

Metallization by plating for high-performance multichip modules

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Electrolytic plating is used to produce the interconnect wiring on the current generation of high-performance multichip modules used in IBM S/390® and AS/400® servers. This paper reviews the material and manufacturing requirements for successful implementation of a multilayer high-density wiring pattern involving electroplated copper metal and polyimide dielectric. Various strategies for the construction of thin-film structures (planarized and nonplanarized) are outlined, and the advantages of electrolytic plating over dry deposition techniques are described.

Introduction

Almost every electronic device is an aggregate of individual chips and discrete components. The ability to effectively package these components often plays a critical role in the ultimate performance of the device. This is especially true for high-end midrange and mainframe computers or servers, which, despite advances in chip design and ultralarge-scale system integration (ULSI) technology, can still consist of hundreds of individual chips.

Packaging in an electronic device serves four major functions. First, it provides the electrical connections (signal and power) among the components in the device. Second, the package provides mechanical protection to the chip die. Third, it acts as a space transformer (fan-out) between the dense chip connections and the less dense connections in subsequent mechanical assemblies. Finally,

the package provides a means to dissipate the heat generated when the chips are powered. For high-end systems the first function, that of electrical connection, is critical to the ultimate performance of the computer. One widely adopted interconnection technique places multiple chips that require interconnections onto a common carrier, referred to as a multichip module (MCM). Depending on the nature of the carrier and the composition of the interlevel dielectric separating the electrical conductors in the package, an MCM can be categorized into one of three types: MCM-L, MCM-C, or MCM-D. For interconnection of the chips, MCM-L [1] uses printed-circuit-board wiring, while MCM-C uses cofired ceramic or glass-ceramic with thick-film metallization. MCM-D uses thin metal films and an organic dielectric over a rigid-base substrate such as silicon or aluminum nitride. This strategy is identical to that used in the fabrication of semiconductor interconnections, and permits MCM-D packages to achieve higher packing density and performance than the other two categories. Not surprisingly, it is also the most costly technology to implement. To reduce cost without a concomitant sacrifice in performance, a hybrid approach is taken by placing less critical wiring in a cofired ceramic base (MCM-C type) while concentrating the critical wiring in the MCM-D upper portion [2-4]. This approach is used in the IBM S/390* and AS/400* high-end servers.

A cross section of a typical MCM-D structure is shown in **Figure 1**. The base substrate is alumina ceramic with multiple levels of cofired molybdenum wiring. The critical

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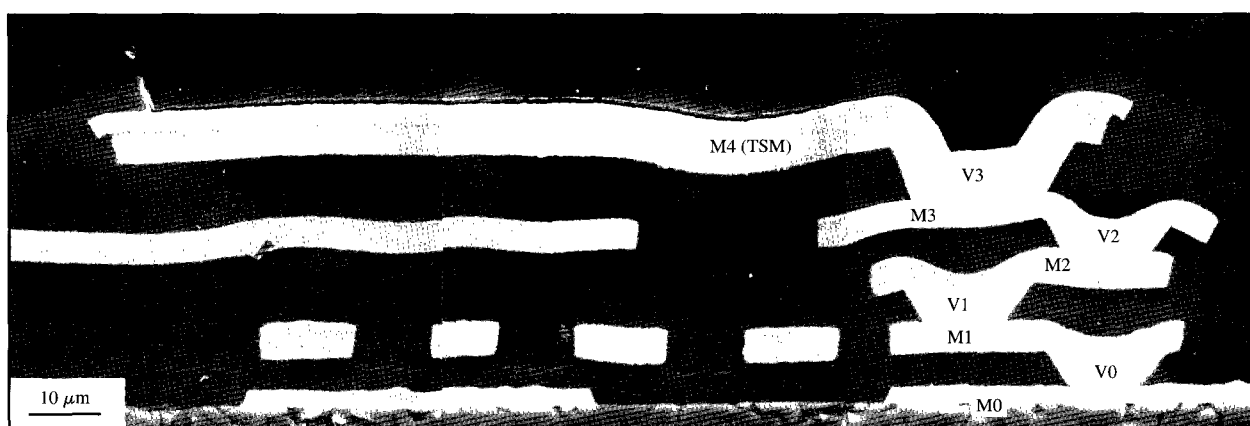


Figure 1
Cross section of a five-level MCM-D substrate showing the individual wiring and via levels from capture pads through terminal surface metallurgy (TSM).

wiring, which consists of five levels of copper lines with a polyimide dielectric, is deposited on top of this base. Metallized capture pads on the top surface of the ceramic connect the internal metallization in the ceramic with the first level of copper wiring (designated as M0). This is followed by a via level, V0, which connects M0 to M1, the second wiring level. Alternating via and wiring levels are then sequentially fabricated, and finally end in a terminal metal layer, also known as the terminal surface metal, or TSM. The structure illustrated in Figure 1 contains five wiring levels (M0 to M4) connected by four via levels (V0 to V3). The narrowest wiring lines are of the order of 13 μm wide, 25 μm apart, and approximately 5 μm thick. Copper is chosen as the conductor line material primarily because of its high electrical conductivity. Polyimides are used as the interlevel dielectric material because they have relatively low dielectric constants and excellent thermal, mechanical, and chemical stability.

There are four common methods of copper film deposition. For features with less demanding ground rules (>25- μm linewidth and 50- μm spacing between lines), a sub-etch process is used [Figure 2(a)]. In this process, a blanket film of copper is deposited by sputtering or evaporation. The film is then photo-patterned with resist, followed by a wet etch to remove the unwanted copper. However, the inherent undercutting associated with wet etching makes this approach unsuitable for defining more aggressive features. Dry-etching techniques such as ion milling alleviate the undercutting, but these techniques are expensive, and minimizing back-sputtering of copper over other areas of the substrate is difficult.

An alternative procedure is metal stencil lift-off [Figure 2(b)]. Here the pattern is first defined by photoresist.

Several metal layers (usually consisting of a diffusion barrier as well as the conductor) are then evaporated over the entire substrate. Because of the line-of-sight deposition during evaporation, there is very little sidewall coverage over the openings of the resist. After metal deposition, the resist is floated away, leaving a clean metal stack over the substrate. Lift-off was successfully used for the terminal metal layer of the IBM S/390 series of computers.

Electroplating metal lines over areas not covered by the photoresist, referred to as "plate-through mask," is the third method. The process, illustrated in Figure 2(c), begins by the blanket deposition of a thin (200 Å) film of chromium, which acts as an adhesion layer between the copper conductor and the dielectric. An electrically conducting copper seed layer is then deposited (usually by sputtering) over the chromium, followed by a photopatterning process using photoresist. In some applications, photosensitive polyimide (PSPI) is used with the photoresist [5] to define the vias which connect the different wiring levels, and remains an integral part of the MCM package.

The fourth method, shown in Figure 2(d), is the damascene process [6, 7]. Here the conductor features are formed by defining openings in the dielectric, backfilling the openings with metal, then removing the excess metal by a planarization step. Metal deposition uses either dry or wet methods, and, as with the other processes, involves multiple layers of different metals.

As currently practiced in the IBM Microelectronics Division, the copper wiring in MCM-D packages is deposited by electroplating using the plate-through-mask

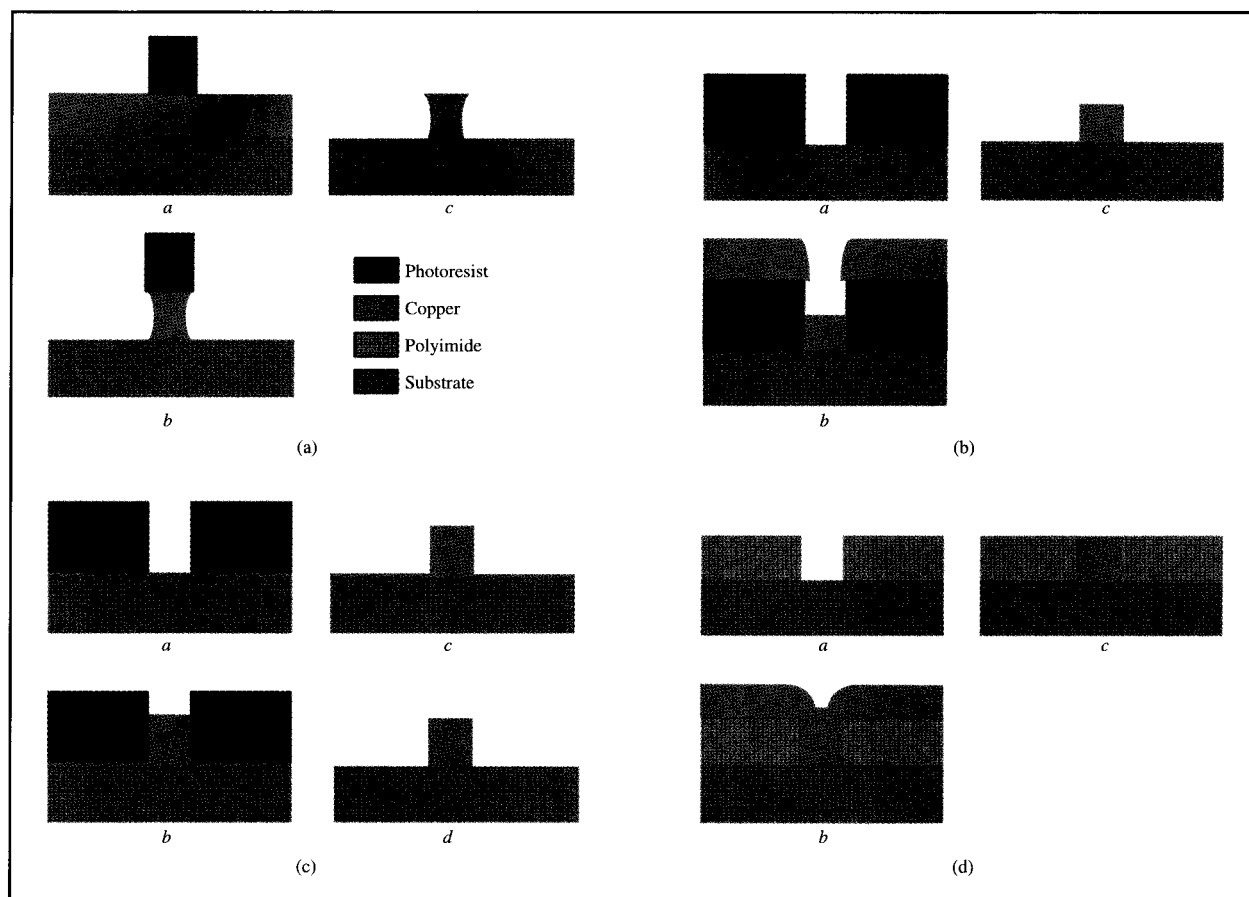


Figure 2

Different metallization schemes for an MCM-D substrate: (a) sub-etch, (b) lift-off, (c) plate-through mask, (d) damascene.

technique. A number of factors led to the selection of plating over a dry process such as sputtering:

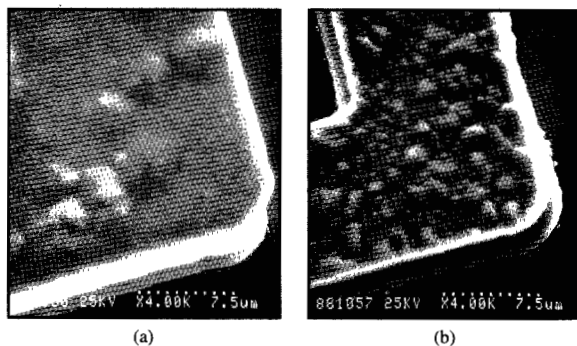
- Plated copper has a more desirable metallurgical structure (low stress, equiaxial, ductile).
- Plating provides improved filling of trenches and vias (less tendency for voids to form).
- The tools and processes used in plating are more scalable to large-format substrates.
- The processing time for plating is faster, thus providing higher throughput.
- Factoring in tooling, raw materials, and maintenance, plating is a relatively low-cost manufacturing process.

The major challenges for plating metal conductors in MCM-D are the relatively small feature size and the correct choice of thin-film materials to ensure the integrity and reliability of the final product. How these and other issues, such as uniformity of thickness, have been

addressed in a manufacturing environment is the focus of this paper. The discussion focuses on electrolytic plating, since electroless copper plating is not widely used in copper/polyimide structures because most commercially available electroless copper chemistries operate at high pH levels, at which many polyimides are unstable. It should be noted that lower-pH formulations based on hypophosphite and dimethylaminoborane have recently been reported [8, 9], and that this may lead to wider use of electroless plating of copper in the future.

Electrolytic plating through resist

Table 1 summarizes the key plating requirements in plating-through masks. To a large extent, metallurgical properties of the plated metal are controlled by the chemistry of the plating bath, followed by the plating parameters (effective current density, temperature, mass-transport condition), the nature of the seed layer, and the postplating processing conditions. While copper metal is



SEM micrographs of copper lines plated in a copper sulphate/sulfuric acid bath: (a) dc plating at 20 mA/cm²; (b) pulse plating at 1.2 A/cm². Paddle speeds are 1 Hz.

Table 1 Key requirements for through-mask plating for MCM-D.

Uniform plating thickness (global and local scale)	±10%
Low electrical resistivity	<1.85 μΩ-cm
Smooth surface	<0.05 μm (peak to peak)
High ductility	>10%
Low residual stress	<200 MPa (copper)
Bath compatible with photoresist	

easily plated from an aqueous solution of its cupric salt, the as-plated copper deposit is usually rough, with large columnar grains and low ductility [10]. The simple salt solution also gives very poor plating thickness uniformity across the substrate. One approach that alleviates these problems is the use of pulse plating. By judicious choice of the pulsing sequence, copper deposits of acceptable quality can be obtained [11, 12]. The optimum pulse sequence is a complex function of the pulse current density, duty cycle, and polarity reversals; a detailed description of the interaction of these three factors is beyond the scope of this paper. **Figure 3** shows SEM micrographs of thin copper lines that were direct-current (dc) and pulse-plated in a sulfuric acid-cupric sulfate solution. The figure shows that pulse plating produces a relatively smooth, fine-grained structure, while dc plating results in a rougher surface composed of large columnar grains. It should be noted that the fine-grained structure is obtained only at pulse-plating current densities higher than 1 A/cm².

Another approach to obtaining fine-grained structures is to incorporate plating additives into the cupric plating bath [10]. A typical commercial plating bath contains several proprietary additives, identified generically as grain refiner, leveler, and ductilizer [13–15]. Experimental evidence exists that some of the additives are not chemically stable, and their breakdown products play a role in the plating process. Routine monitoring of the plating-bath chemistry by chemical and functional analysis is crucial when using plating baths with additives. Commonly used techniques for additive analysis include high-performance liquid chromatography, microcapillary electrophoresis, cyclic voltammetric plating, stripping analysis, and Hull cell analysis [16–22].

For uniformity of thickness, plating is affected not only by the bath chemistry and plating parameters, but also by the geometric arrangement of the features to be plated on the package. Dukovic et al. [23, 24] have extensively studied different attributes of current-distribution effects on the thickness uniformity of plated metals. They found that, in general, global variations in plated metal thickness from the edge to the center of the substrate are due to nonuniformities in the current distribution. These variations can be alleviated during plating by passing cathodic current to a secondary cathode surrounding the substrate. This approach can be extended to minimize the effect of pattern density (where plated features in isolated areas are thicker than those in densely populated regions) by distributing dummy features within the wiring layout.

The thickness of small plated features, such as individual lines, is measured nondestructively with a microprofilometer, preferably after the seed layer is removed. However, a highly irregular surface topography can render this technique ineffective. When line thickness must be determined and profilometry cannot be used, a substrate is cross-sectioned and the line thickness measured by scanning electron microscopy (SEM). Larger metal features are measured with a four-point probe or microbeam X-ray fluorescence spectroscopy (XRF). XRF has advantages over other methods of thickness measurement in that it is a noncontact technique, and, because of its capability for elemental discrimination, can resolve the thickness of individual metal layers in a multilevel metal stack, provided that those layers consist of different metals.

Planar and nonplanar MCM-D

The vias linking two neighboring metal planes can be partially or completely filled, which leads to two different versions of the MCM-D thin films. For the partially filled version, both the vias and the lines in the next thin-film layer are metallized simultaneously, as illustrated in **Figure 4**. After blanket polyimide deposition, vias are opened in the polyimide. Commonly used techniques for

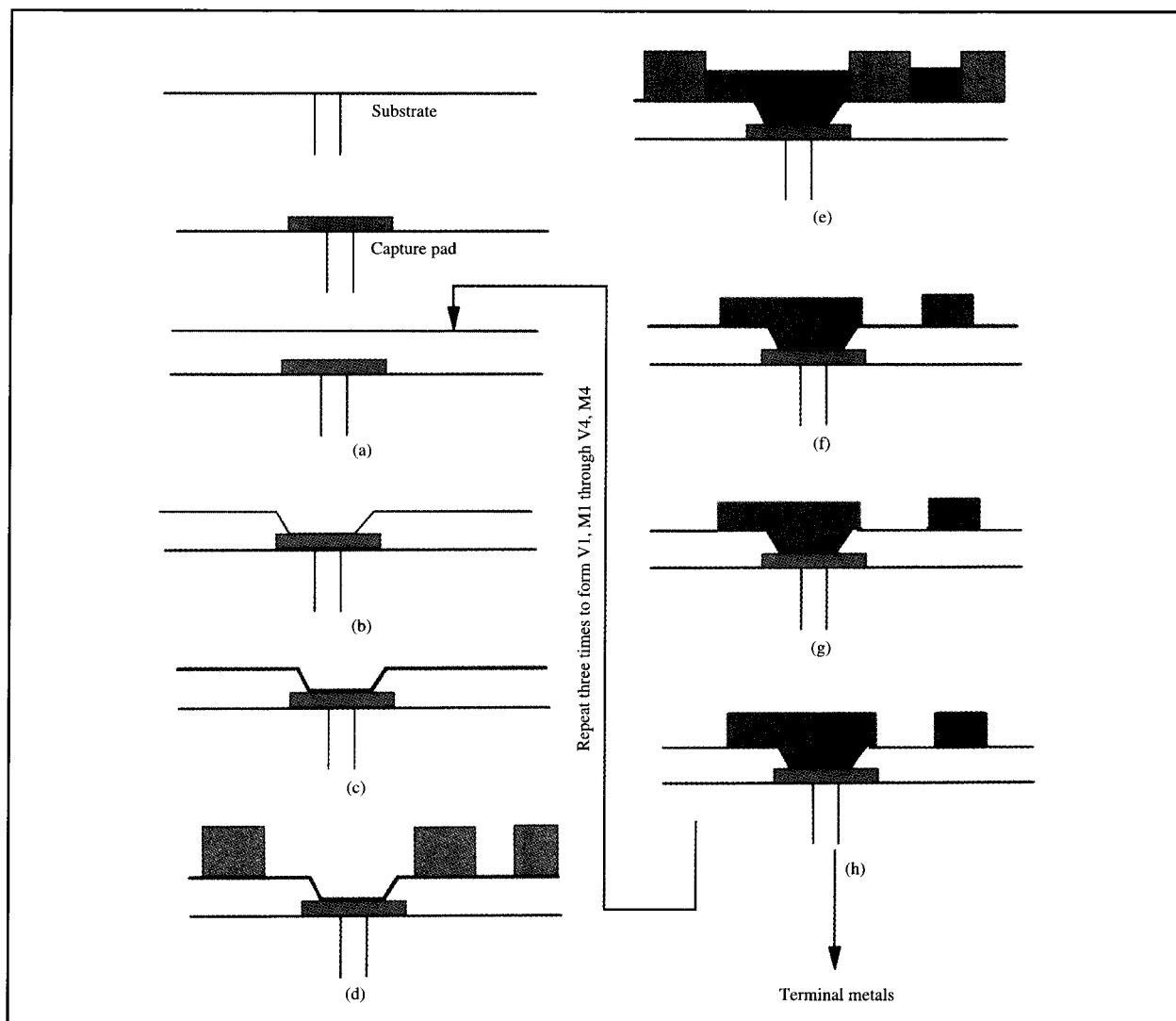


Figure 4

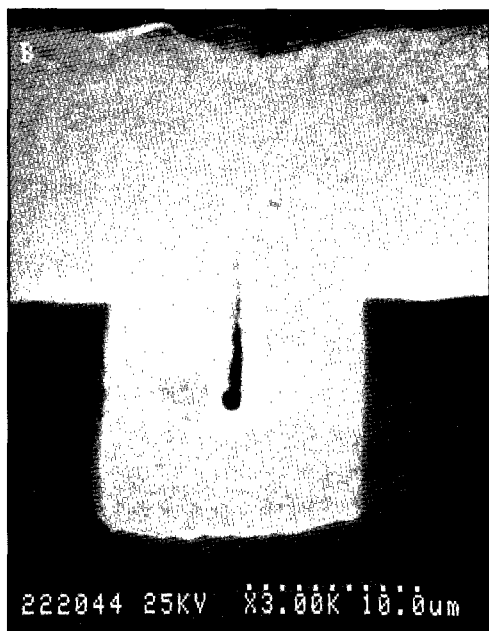
Process flow for building a multilevel MCM-D substrate: On a substrate with a capture pad making contact with the underlying via, (a) deposit polyimide, (b) form a via, (c) deposit a blanket seed layer for plating, (d) lithographically pattern to define plating features, (e) plate Cu, (f) strip photoresist, (g) isolate Cu conductors by removing the seed layer between conductors, (h) deposit layer to enhance polyimide adhesion to Cu. Repeat steps (a) through (g) three more times to form M2, M3, and M4 layers. Proceed to terminal metal deposition steps for formation of the M5 (TSM) layer.

via creation are laser ablation, reactive ion etching, and photolithography using a photosensitive polyimide. A seed layer is deposited, lines and vias defined by a resist, and the metal then deposited via plating. This process fills the vias only partially (see Figure 1), which results in nonplanarity in the subsequent polyimide overcoat. The degree of nonplanarity is a function of the via diameter, as well as the type and thickness of the polyimide dielectric. A thicker polyimide overcoat yields a more planarized structure; however, there are constraints on the thickness

of the polyimide which arise from the electrical and mechanical properties of the package. For designs with less demanding ground rules (linewidths $>8 \mu\text{m}$), the extent of nonplanarity is not too severe, and a planarization step is not required after plating. The ability to build multilevel thin-film structures without a planarization step, as well as the simultaneous plating of lines and vias, significantly reduces the manufacturing cost of an MCM-D substrate. The major drawback of this nonplanarized design is that the vias in the next layer



(a)



(b)

Figure 5

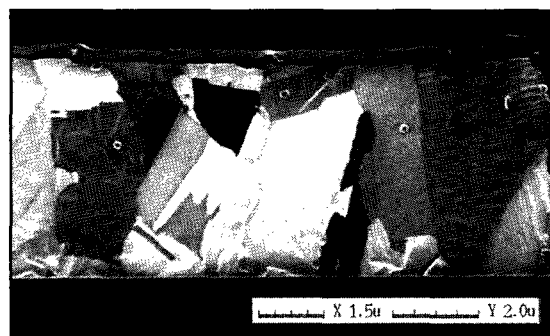
SEM cross sections of (a) multiple partially filled damascene structures; (b) single Cu-filled damascene structure with a void in the center.

must be offset from the underlying layer, which decreases the effective channel width in the wiring layer.

For MCM-D packages with narrow ground rules (plated linewidths $< 8 \mu\text{m}$ and aspect ratios $< 2 \mu\text{m}$), a planarized structure such as that produced by the damascene process [Figure 2(d)] is required. For carriers with large features, the excess copper to be removed after the plating step is beyond the capability of chemical-mechanical polishing and conventional mechanical milling techniques. Trenches with high aspect ratios or with sidewalls having negative angles can lead to void formation in the center of the deposit. These voids can trap liquids such as plating solution or deionized water from a rinsing operation, which can cause corrosion and line fracture during subsequent processing. **Figure 5** shows a partially filled damascene structure with early signs of void formation.



(a)



(b)

Figure 6

Focused ion beam (FIB) cross sections of plated copper lines showing characteristic microstructure: (a) as plated; (b) after two 400°C polyimide cure cycles.

Void formation is prevented by using trench features having a small aspect ratio and vias with a wide opening at the top.

Plated copper metallurgy

The microstructure of as-plated copper from a plating bath with additives is characterized by a low tensile stress ($< 75 \text{ MPa}$), a modest preferred orientation along the Cu(111) planes, and a highly twinned structure, as illustrated by the focused ion beam (FIB) image of an as-plated line shown in **Figure 6(a)**. A low-stress film is critical, as high residual stresses can lead to film delamination. In general, the film texture of plated copper does not appear to affect the electrical or mechanical properties of the lines themselves, but contributes to improvement of the quality of bonding between lines and adjacent vias.

During processing, plated copper is subjected to at least one annealing during polyimide curing at 400°C; recrystallization and significant grain growth, as well as a reduction of twinning, are subsequently observed in the

microstructure [Figure 6(b)]. However, the residual stress remains low and the degree of preferred orientation remains unchanged. The structural changes which occur as a result of the polyimide cure do not appear to affect the electrical properties of the copper. Figure 7 shows the change in resistance of a plated copper film as measured by a four-point probe after the film was subjected to two simulated 400°C cure cycles. The data are presented as a percentage change. As can be seen from the figure, the changes measured are not significant.

Because of their sensitivity to changes in the chemistry of the plating bath, the metallurgical properties of deposited films such as electrical resistivity, grain structure, crystallographic orientation, and residual stress of the deposit should be periodically measured and evaluated.

Surface contamination and resist delamination

The largest defect contributors in plating-through-resist are surface contamination and resist delamination. Surface contamination can be caused by photoresist residues, fingerprints, foreign particles, and metal flakes from the plating fixtures. To minimize foreign-particle contamination, all MCM-D thin-film processing is performed in a class 100 or better clean-room environment. Plating tanks are constructed with inert polymeric materials, and plating solutions are constantly filtered with micron- or submicron-size particle filters. Extraneous plated metal due to resist delamination and cracking is avoided by choosing a proper photoresist and optimizing postdeveloped baking conditions.

Tooling

For adequate fill of narrow lines, such as those shown in Figure 1, the mass-transfer rate of plating chemicals in a conventional open tank with mechanical agitation or jet-stream impingement is not sufficiently uniform to ensure adequate plating over the entire substrate surface [25, 26]. After extensive studies of various mass-transfer mechanisms, a tool with paddle agitation was used [27]. The proper use of a paddle cell can maintain the variation in uniformity of copper thickness across a 125-mm × 125-mm substrate at less than 10%. Plating conditions for each layer require separate optimization. Mathematical modeling [23, 24] is helpful for selecting the initial parameters, but plating and measurements on actual substrates are needed to establish the final conditions.

It has been mentioned previously that one of the major disadvantages in the use of MCM-D packages is their high cost of manufacture. Proposals have been made [28, 29] to reduce this cost by fabricating multiple MCM-D packages on a single large carrier, then dicing them into individual pieces (in a manner similar to that used in the fabrication of semiconductor chips). This would require plating

0.7	0.8	0.9	1.5	0.7
-1.7	-0.5	-1.4	-0.1	-0.7
1.1	0.8	1.2	0.6	-0.2

Figure 7

Percentage change in resistance of a blanket film of plated copper after two 400°C polyimide cure cycles. The initial resistance readings ranged from 0.822 to 0.881 mΩ. Data shown for the top half of the Cu film (similar data on bottom half).

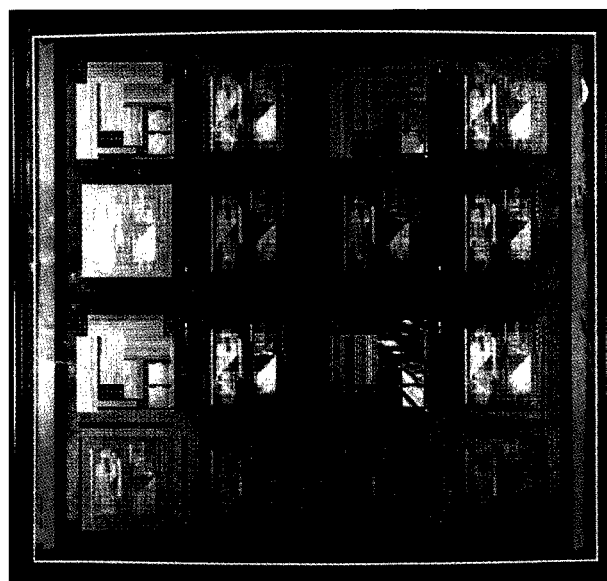


Figure 8

Top view of a 300-mm² panel containing 16 individual 63-mm² MCM-D substrates. Each substrate has five levels of wiring, with 13-μm-wide Cu lines on a 25-μm pitch.

uniformity over very large surface areas. It has been demonstrated [27] that paddle cells can efficiently and uniformly transfer plating chemicals over such large areas; Figure 8 shows a copper-plated 300-mm × 300-mm carrier with sixteen individual MCM-D packages.

Capping of plated copper

For many polyimides, it is desirable to have a layer of adhesion promoter over the plated copper before coating with polymer. Copper can react chemically with these

1.7	-0.7	-0.8	0.2	-1.7
-1.6	-1.7	-2.4	-1.5	0.1
1.5	1.8	2.7	0.6	2.4

Figure 9

Percentage change in resistance of a 5- μm -thick blanket Cu film capped with 0.2 μm of cobalt-phosphorus, subjected to two polyimide cure cycles. The initial resistance readings ranged from 0.846 to 0.885 m Ω . Data shown for the top half of the Cu film (similar data on bottom half).

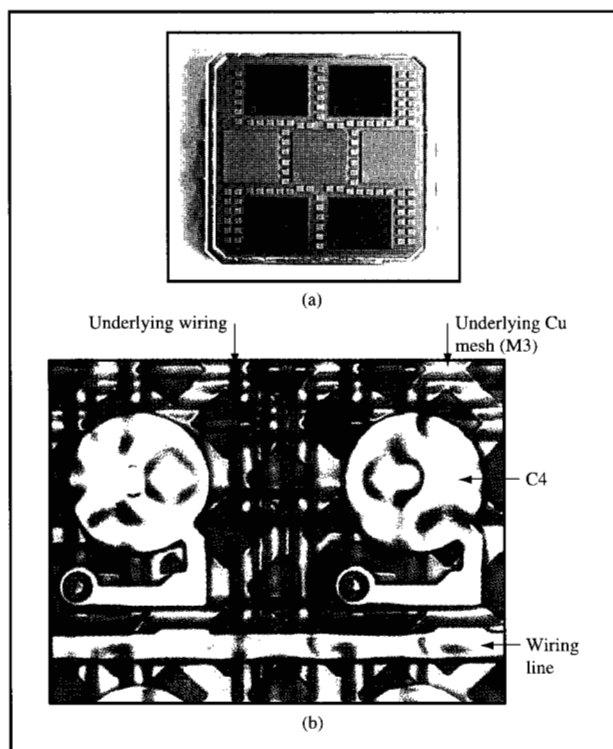


Figure 10

Top views of the terminal metal of an MCM-D substrate: (a) Entire package, showing the terminal metal layer with chips; (b) 400 $\times$ optical micrograph showing the individual C4 pads and underlying metallurgy.

adhesion promoters as well as with polyimide precursors containing free acid groups [30]. Therefore, it is necessary to protect the plated copper with a thin layer of capping material. After testing of different candidate materials,

electrolessly deposited cobalt-phosphorus (CoP) was selected as the capping layer [31]. One concern in using a capping layer is that the copper and the cap will react during subsequent annealing, resulting in degradation of the electrical properties of the copper. **Figure 9** shows the percentage change in the resistance of copper with a CoP layer after simulation of two polyimide cure cycles. The resistance change in the metal stack is negligible; the presence of both positive and negative values suggests that the changes observed are the result of measurement error. The use of less-reactive polyimide dielectrics to make the capping layer unnecessary is currently under development [32].

Terminal metal

All chip carriers require exposed connections, referred to as the terminal metal, to permit the electrical connection of the chip to the carrier. Because exposed copper oxidizes readily in air and makes bonding more difficult, a different metallization deposition scheme consisting of electroplated copper/nickel/gold is used in the terminal metal layer. The gold acts as the oxidation barrier, while the nickel layer serves as a diffusion barrier preventing the interaction of copper with the gold. For most applications, a 2- μm -thick nickel layer is needed. Other barrier metals, including electroplated cobalt and cobalt-nickel, have been used [33]. Nickel and gold are electroplated sequentially after copper from their respective plating baths. The thickness of the gold layer varies with the bonding technology used to join the semiconductor chips and other discrete components to the substrate. Typically, the gold thickness is about 0.5 to 2 μm for wire bonding and a few hundred angstroms for lead-tin solder joining. In applications where more than one terminal bonding technology is used, additional photolithography and gold-plating processes are required. **Figure 10** shows a top view of the terminal metal pads on an MCM-D package. There are approximately 18000 C4¹ pads on the 63-mm $\times$ 63-mm package shown.

Conclusion

For large server systems, multichip modules (MCMs) are commonly used to enhance overall system performance. Current designs utilize a hybrid design, with multiple layers of copper wiring and polyimide dielectric deposited onto a cofired ceramic base containing less critical wiring levels. For modules with lines less than or equal to 15 μm on 25- μm spacing, electroplating through a mask is the preferred metallization technique. The major challenges to electroplating fine copper lines are proper selection of liner and capping metallurgy, control of plated-copper thickness and uniformity, and optimization of plating-bath chemistry. The best results have been obtained using a

¹C4: Controlled Collapse Chip Connection.

paddle cell and the pulse-plating technique. Plating baths must be filtered and changed frequently to eliminate surface contamination and photoresist residues. Development efforts continue to extend electroplating to tighter ground rules by using the damascene process and large plated structures up to 900 cm² in area.

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