

Thin-film multichip module packages for high-end IBM servers

by E. D. Perfecto
A. P. Giri
R. R. Shields
H. P. Longworth
J. R. Pennacchia
M. P. Jeanneret

A new generation of multilevel thin-film packages has been developed for IBM high-end S/390® and AS/400® systems. Thin-film structures in these packages are nonplanar and can be fabricated by either pattern electroplating or subtractive etching. Selection criteria for choice of fabrication methods are discussed in terms of electrical performance requirements, ground rules, manufacturability, and cost issues. Two problems encountered in the development phase of the nonplanar thin-film structures were 1) accelerated etching of plated Cu features during Cu seed etching, and 2) corrosion of the bottom-surface metallurgy during etching of Cr at the top surface. Effective solutions were developed on the basis of underlying electrochemical phenomena. Finally, reliability stress procedures used to qualify these packages and results of these procedures are presented.

Introduction

Multichip modules (MCMs) are used to integrate semiconductor chips into a single package. These structures must meet system-level electrical, thermal, and

reliability requirements. The increased level of semiconductor integration, along with its higher input/output (I/O) density, demands an increase in MCM wiring density [1]. Greater wiring densities are obtained by utilizing cofired multilayer ceramic substrates, where ceramic layers are typically Al_2O_3 and internal wiring is screened on using Mo paste. Thin-film layers on ceramic generally reduce the total number of layers required in the ceramic substrates. Electrical modeling studies have shown that Cu/polyimide multilevel thin-film (MLTF) structures deposited on cofired ceramics provide the required characteristic impedance and shorter signal propagation delays [2-4]. To meet the performance requirements of high-end servers, IBM has developed nonplanar MLTF structures. This paper compares two recent MLTF modules and describes their thin-film fabrication methods, processes, and materials.

Thin-film structures

Since 1989, the IBM Microelectronics Division has manufactured thin-film modules for IBM AS/400* and S/390* systems. From 1994 to the present, thin-film modules have evolved from a two-level planar structure for the IBM ES/9000* system [5] to a five-level nonplanar structure for the AS/400 system [6]. This was primarily

©Copyright 1998 by International Business Machines Corporation. Copying in printed form for private use is permitted without payment of royalty provided that (1) each reproduction is done without alteration and (2) the *Journal* reference and IBM copyright notice are included on the first page. The title and abstract, but no other portions, of this paper may be copied or distributed royalty free without further permission by computer-based and other information-service systems. Permission to *republish* any other portion of this paper must be obtained from the Editor.

Table 1 Thin-film product comparisons.

<i>System name</i>	<i>AS/400</i>	<i>S/390</i>
Announcement date	1995	1997
Ceramic		
Substrate type	Alumina	Alumina
Substrate size (mm)	63 × 63	127.5 × 127.5
No. of layers	30	69
Thin films		
No. of layers	5	4
No. of nets	3600	12,400
No. of vias	18,000	100,000
Wiring length (m)	75.5	65.1
No. of pins	882	3526
System speed (ns)	5.0	5.0
Chip		
Number of chips	7	28
Chip type	bi-CMOS	CMOS
Chip size	14.8–15.8	14.8–17.3
No. of C4s	5600	30,000

Table 2 Comparison of thin-film structures by product.

<i>System name</i>	<i>AS/400</i>	<i>S/390</i>
No. of thin-film layers	5	4
Process type by level	SE/ PE/ PE/ PE/ PE	SE/ SE/ SE/ PE
Wiring pitch (μm)	25	50
Wiring width (μm)	13	25
Min. spacing (μm)	12	15
Min. via diameter (μm)	10	20
Wiring metal	Cr/Cu/Co	Cr/Cu/Cr
Cu metal thickness (μm)	4.5	3.7–5.0
Polyimide dielectric thickness (μm)	6.0–9.0	7.0–9.0
Thin-film capacitance (pF/mm)	0.18	0.17–0.19
Thin-film resistance (Ω/mm)	0.34	0.22
Chip join metal	Ni/Au	Ni/Au

SE: subtractive etching; PE: pattern electroplating.

dictated by the need to provide increased wiring density while meeting cost objectives. Electrical specifications for conductor and interlevel dielectric require that metal and dielectric thicknesses, as well as metal linewidths, must be precisely controlled. Comparisons of the physical attributes of AS/400 and S/390 modules as well as thin-film ground rules and electrical characteristics are shown in **Tables 1** and **2**, respectively.

In 1995, IBM initiated fabrication of thin-film modules for the midrange AS/400 system. The cofired $\text{Al}_2\text{O}_3/\text{Mo}$ substrates had Mo vias on the top surface for thin-film interconnections and screened-on Mo ($\text{Mo}/\text{Al}_2\text{O}_3$

composite) I/O pads on the bottom side. These pads were then electrolessly plated with Ni/Au prior to thin-film processing. The bottom-surface metallurgy is commonly referred to as the BSM. The top surface was planarized utilizing lapping and polishing techniques, and MLTFs were fabricated. After thin-film fabrication, a 127.5-mm^2 substrate was diced into four individual modules. Pins brazed onto the BSM connected the module to a circuit board.

The thin films in the AS/400 module consisted of a capture pad/mesh (power) level, two wiring levels, a second mesh (ground), and a terminal metal layer for chip joining [7]. All seven chips were interconnected with $13\text{-}\mu\text{m}$ linewidths at a $25\text{-}\mu\text{m}$ pitch. The required metal thickness ($4.5\text{ }\mu\text{m}$) necessitated the use of pattern electroplating. **Figure 1** shows a typical cross section of the thin-film portion of the AS/400 substrate. Packaging modules for the S/390 system [8, 9] required thin films on a 127.5-mm^2 substrate for interconnecting up to 34 chips (**Figure 2**).

Thin-film process selection

Processes used for fabricating thin-film multilayers on ceramic or organic carriers are defined by a sequence of steps which are repeatedly used for 1 to n levels of metal. The key to low-cost fabrication is a) minimizing the number of processing steps for wiring and terminal metal layers, and b) selecting robust processes for high yields. Wiring layers can be fabricated in a variety of ways. Nonplanar thin-film structures are more cost-effective than planar structures, since they avoid the extra planarizing steps, and can be fabricated by subtractive etching or pattern electroplating [10, 11]. However, critical process steps must be optimized to effectively control linewidths and spacings between lines for a desired metal thickness. These processes are schematically described in **Figure 3**.

In subtractive etching, a Cr/Cu/Cr sputtered metal is chemically etched through a defined photoresist image. The isotropic nature of chemical etching produces metal undercutting during the image transfer (etching) of the Cr/Cu/Cr features. Subtractive processes for $3\text{--}6\text{-}\mu\text{m}$ -thick Cu layers were optimized to yield an undercut of 1.2 times the thickness of Cu. A $10\text{-}\mu\text{m}$ feature (minimum dimension) can be successfully etched for Cu metal thicknesses of $2\text{ }\mu\text{m}$ or less. Chromium $250\text{ }\text{\AA}$ thick is used to enhance the photoresist and polyimide adhesion. It also provides an optical contrast with the polyimide, facilitating autoinspection. Copper is etched with ammonium persulfate solution in a spin/spray tool. In this system, etch rates show first-order reaction kinetics [12]. An endpoint detector is used to minimize the undercut and to ensure linewidth control. The tolerances associated with the

sputtered metal thickness, resist lithography, and etching contribute to a $\pm 5\text{-}\mu\text{m}$ feature linewidth variation.

In pattern electroplating, linewidths can be controlled to $\pm 3\text{ }\mu\text{m}$, since feature dimensions are defined by photolithographic tolerances. Copper is the material of choice for wiring because of its electrical properties, plating chemistry, and cost [13]. The conductive seed layer, consisting of $250\text{ }\text{\AA}$ Cr and $2500\text{ }\text{\AA}$ Cu sputtered over the entire surface, is etched after electroplating Cu. Thin copper oxides on the seed are etched in the plating solution before Cu plating begins. Good electrical and mechanical connection occurs even when the seed is partially etched. The transmission electron microscope (TEM) photograph in **Figure 4** shows the plated wiring metal and a partially etched Cu seed. After the seed metals are etched, the plated Cu wiring is capped using electroless Co(P) chemistry [13]. Cobalt-phosphorus capping is used for the same reason that the top Cr is used in the subtractive etching process: a) to facilitate autoinspection by enhancing the optical contrast between the Cu wiring and the polyimide background, and b) to provide enhanced polyimide adhesion. Cobalt-phosphorus alloy is commonly utilized to prevent Cu from reacting with and precipitating in polyamic acid [14]. However, in the above application, the polyimide precursor is a polyamic ester without $-\text{COOH}$ acidic end groups; therefore, Cu reaction and diffusion do not occur [15].

There are various factors to consider when choosing between pattern electroplating and subtractive etching. Subtractive etching is a lower-cost process and is therefore the preferred method. Pattern electroplating is used when closely spaced wires are required. **Figure 5** shows the typical linewidths and spacings that can be achieved under optimal etching conditions [11]. Since a $5\text{-}\mu\text{m}$ metal thickness and a $26\text{-}\mu\text{m}$ spacing between wiring lines lie on the boundary of pattern electroplating and subtractive etching, it is questionable whether subtractive etching can provide an equivalent yield under manufacturing conditions. No significant yield differences have been observed after the fabrication of more than 1000 parts utilizing both processes.

Finally, Ni/Au terminal metal pads (**Figure 1**) required for C4¹ chip joining are defined by pattern electroplating. The Ni which acts as a barrier layer is known to prevent the rapid buildup of Cu/Sn intermetallics during multiple reflows typically required for chip reworks, ensuring the reliability of C4 interconnections [16]. A new repair procedure was developed in which the last metal layer not only had C4 joining pads but also a set of lines in X and Y directions that allowed for the rewiring of defective signal interconnections in the ceramic as well as in the thin films [7, 17].

¹ Controlled collapse chip connection.

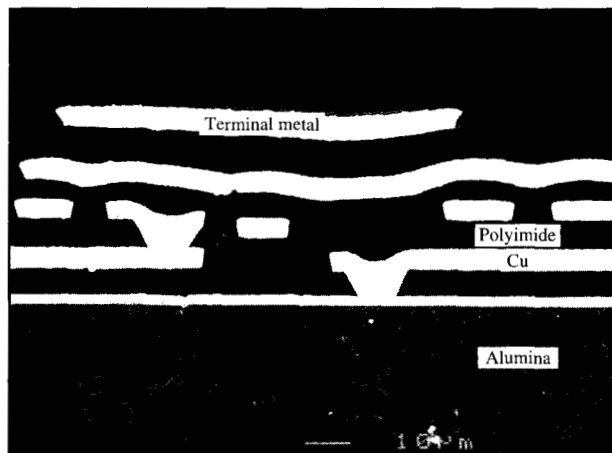


Figure 1

Thin-film SEM cross section of AS/400 module.

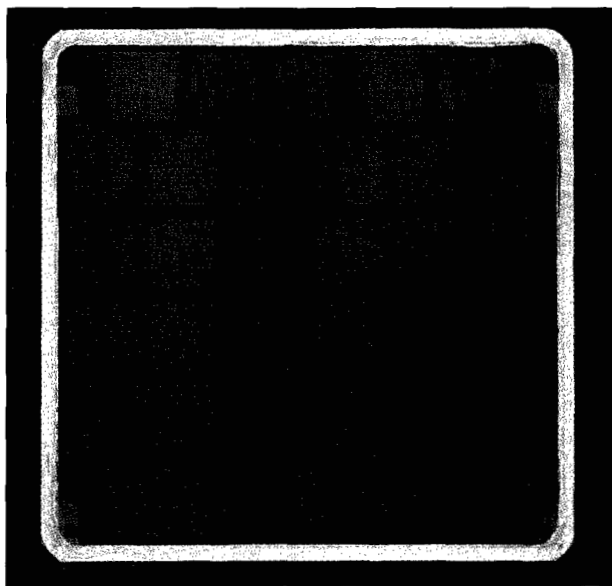


Figure 2

Top view of S/390 high-performance multichip module.

Seed etching process optimization

The etching of the seed layer is one of the most challenging process steps, since etching of the plated features occurs concurrently. Fortunately, the sputtered Cu seed etches at a slightly faster rate than the plated Cu features, which reduces thickness loss of the Cu plated features during the seed etching. The etch-rate differences seen for sputtered films vs. plated films can be explained

Prepare substrate, define first-level metal by subtractive etching of Cr/Cu/Cr



Apply and cure polyimide, laser-ablate the vias



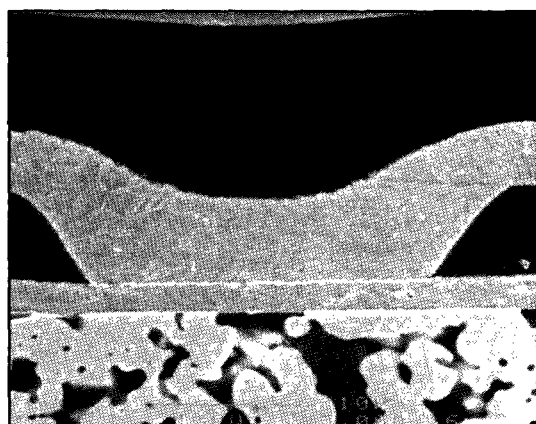
Sputter Cr-Cu seed layer



Apply photoresist and define wiring level



Electroplate Cu, strip photoresist, etch Cu-Cr and electroless Co-P cap



(a)

Prepare substrate, define first-level metal by subtractive etching of Cr/Cu/Cr



Apply and cure polyimide, laser-ablate the vias



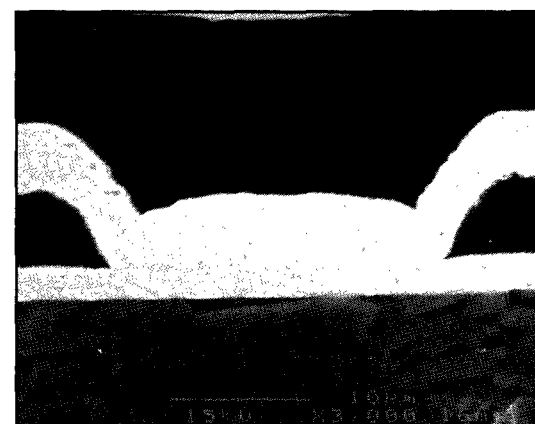
Sputter Cr-Cu-Cr blanket metal



Apply photoresist and define wiring level



Etch Cr-Cu-Cr metal and strip photoresist



(b)

Figure 3

Process flow and SEM cross sections of a via fabricated by (a) pattern electroplating and (b) subtractive etching.

in terms of structural differences (Figure 4). For example, sputtered films prepared under low Cu adatom mobility conditions produce columnar structures [18], while plated films produce equiaxed large-grain structures. Besides structural differences, oxide films formed on the Cu seed delay the onset of seed etching. This increased total

etching time results in increased plated metal roughness which can cause problems in Co(P) capping and layer-to-layer via interconnection. Other factors that influence the etching time are Cu seed thickness, solution pH, and percent of over-etch. **Figure 6** shows atomic force microscope (AFM) measurements of Cu after plating and

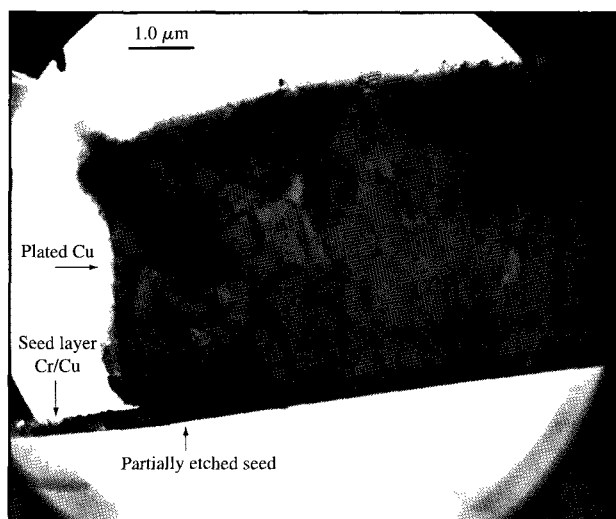


Figure 4

Cross-sectional transmission electron microscopy (X-TEM) of 5- μm -thick electroplated Cu on Cr/Cu sputtered seed.

after seed etching. The AFM measurements after seed etching can vary from ± 20 nm to ± 150 nm. Smoother Cu surfaces also provide for a more efficient autoinspection.

During the etching of the Cu in the seed layer, the endpoint detector is triggered as soon as featureless areas are clear. To ensure that the Cu seed is etched in the high-density feature areas, a 20% over-etch is used. This is referred to as the standard etch process. An accelerated etching of the Cu plated features occurs during the over-etch cycle. Galvanic coupling between the Cr and the Cu etch solution has been suggested as the mechanism for this effect [19]. The effects of accelerated etching are more pronounced with increased numbers of wiring levels and interconnections. For example, accelerated etching is observed at the second wiring level, but is nonexistent on the mesh levels where the pattern is uniformly dense.

An IBM proprietary etching process was developed and optimized to eliminate accelerated etching. **Figure 7** compares the effects of extended Cu seed etching in three cases: 1) isolated and dense wiring areas without thin film or substrate connection etched with the standard process; 2) isolated features with via and substrate connection etched with the standard process; and 3) isolated and dense wiring areas with substrate and via connection etched with the optimized process. As **Figure 7** shows, interconnected Cu features (16 μm wide, 45 μm long, and 4.5 μm thick) which are isolated can be completely removed by etching during the standard over-etch cycle. The optimized etching process not only prevents removal of the interconnection, but also decreases

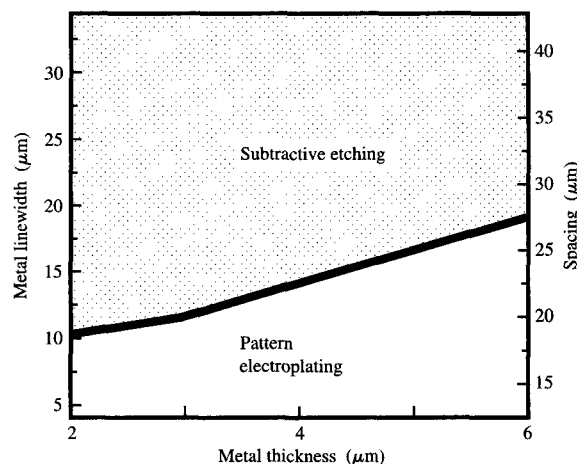


Figure 5

Parameters controlling subtractive etch vs. pattern electroplating selection. Beyond 10- μm linewidth, spacing requirements will control process selection. Spacing = (etch factor $\times$ metal thickness $\times$ 2) + 13. (13 μm represents 10 μm of minimum mask feature spacing plus 3 μm develop process bias.) Etch factor = 1.5 for metal thickness < 3 μm and 1.2 for metal thickness > 3 μm .

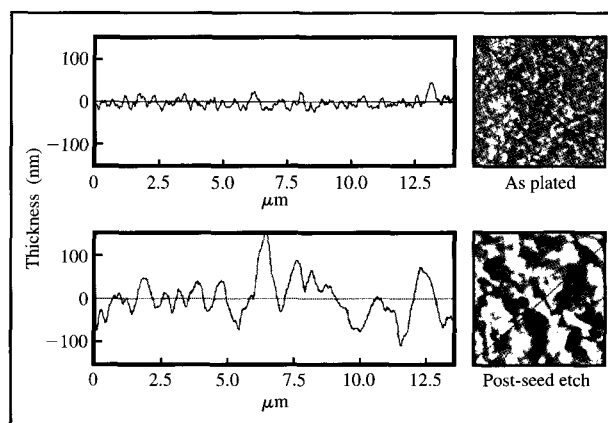


Figure 6

Comparison of AFM surface roughness of Cu as plated and after seed etching.

the difference in etch rate between isolated and dense lines. Since no accelerated etching occurs in the optimized etching process, the percent of over-etch can be increased, thus decreasing the chance of feature-to-feature shorting while maintaining good feature integrity.

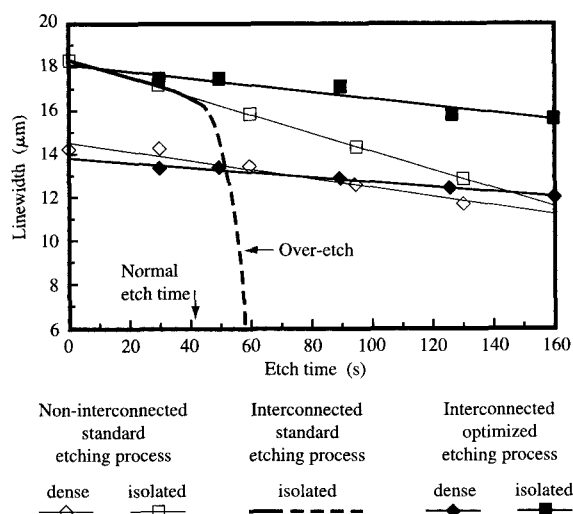


Figure 7

Effect of interconnection and wiring density on electroplated Cu during seed etching.

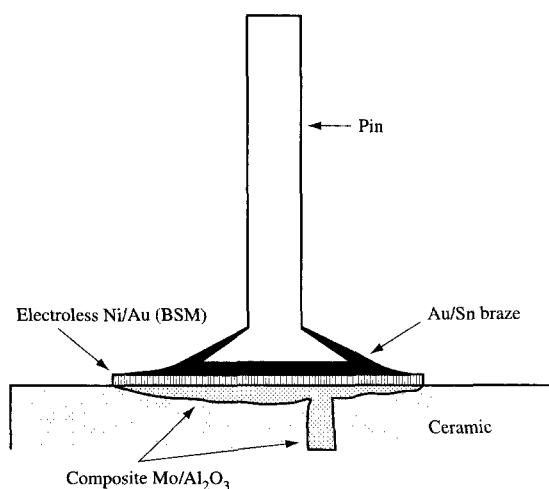


Figure 8

Schematic diagram of the BSM pad and brazed pin.

Effect of wet processes on integrity of BSM pads

BSM features on alumina substrates are deposited by electroless Ni and Au plating on sintered Mo pads (Figure 8). Four to six levels of thin-film wiring are subsequently built on the top surface of the substrate. During early

development of the MLTF process, a closer examination revealed that wet processes, and their specific sequence, could significantly affect the integrity and reliability of thin-film structures. This section briefly discusses the observed effects of wet processes on the BSM structures, the underlying electrochemical phenomena associated with wet processes, and the elimination of undesirable effects.

Multilevel thin-film processing on alumina substrates exposes metal features on top and bottom surfaces to various acids and alkaline etchants more than ten times during normal processing. The typical Cr etchant is an alkaline KMnO_4 solution followed by an oxalic acid rinse. This process was found to cause corrosion of BSM pads, which affected the reliability of brazed pins. However, at the final stage of MCM processing, the extent of the BSM pad corrosion could not be readily detected.

Cross-sectional analysis of a Ni/Au-plated Mo pad (Figure 9) and tape adhesion testing (Figure 10) of the same structure revealed that under the Ni/Au surface Mo corrosion can be extensive. Since different metals on the top and bottom surfaces are exposed in both high- and low-pH solutions, localized galvanic cells may be established. The electromotive force may vary from region to region because of varying metal interconnection lengths between top- and bottom-surface features. For example, pinholes in Ni and Au films on BSM pads cause Mo, Ni, and Au to come into contact with wet etchants, and in these regions one would expect different galvanic reactions. Predicting the steady-state electromotive potentials and currents of such cells and their effect on BSM corrosion is nontrivial. One can use Pourbaix diagrams [20] for various metals to qualitatively examine the processing conditions and their effect on corrosion. For example, Pourbaix diagrams show that Mo exposed to pH 7 solutions and Ni exposed to solutions with pH below 8 and above 12 can lead to corrosion reactions. Since the alkaline KMnO_4 solutions have a pH greater than 10, and other photolithography processing solutions have a pH range of 10 to 14, observed effects can be eliminated if metal features are protected from exposure to such high-pH solutions. Of the various methods evaluated for protecting the BSM features during Cr etching, vacuum-assisted mechanical protection has proved to be most effective. MCM substrates etched using such an approach show no corrosion of BSM features. Additionally, to reduce the possibility of pinholes in the Ni layer, the electroless Ni film thickness on BSM features was increased. The results of extensive reliability testing of MCMs, discussed below, support the effectiveness of these actions.

Reliability assessment/qualification

The three stages of reliability assessment are 1) feasibility assessment, in which specially designed test vehicles with

ground rules tighter than those of product are used; 2) prototype evaluation on modules similar to product; and 3) product qualification, in which modules are built with the plan-of-record process under strict quality-assurance and engineering-change (QA/EC) controls. The development of nonplanar multilevel thin films and their subsequent use in several generations of IBM high-end servers followed the same qualification process.

- *Reliability concerns*

Nonplanar structures can create localized variations in polyimide thicknesses. Tight ground rules and high wiring density allow limited tolerance for contamination and process variation; both can affect yield and long-term reliability. The complex processing steps associated with MLTFs require an evaluation of both BSM features and pin integrity, since multiple thermal excursions can cause cracking or delamination of the metallurgy. If the BSM features are not well protected during Cr etch processing, the underlying metals, Ni and Mo, can be corroded, leading to voids or delamination (Figure 9). Contamination and impurities trapped either within or on the surface of the wiring metal can lead to corrosion and migration-induced shorts.

- *Reliability assessment*

Table 3 is a summary of the reliability stress conditions utilized to qualify MLTF modules. This includes accelerated stressing and integrity assessments through mechanical strength measurements and visual inspections. The first four cells in Table 3, thermal cycling (T/C), thermal shock (T/S), temperature age (T/A), and electromigration (E/M), are designed to monitor potential via or line opens due to metal fatigue, poor via formation, or Cu electromigration. Modules in T/C and E/M cells also contain special repair wires which are stressed to evaluate the integrity and reliability of line open repair bonds [21]. The next three stress cells, temperature/humidity/bias (T/H/B), highly accelerated stress test (HAST), and temperature/bias (T/B), are designed to monitor intralevel or interlevel shorts due to wet or dry metal migration, corrosion, or contamination. All test modules are electrically tested before and after stressing, and are monitored for shifts in electrical measurements either *in situ* or at certain stress intervals.

The integrity of the BSM pads and pins is determined by visual inspection and mechanical stressing (pin-bending test, flexing, and pin tensile pull). These tests are carried out periodically during multiple temperature excursions to simulate chip joining, T/S, T/H/B, and HAST stressing, with visual inspections and pin pull-strength evaluations performed at each step.

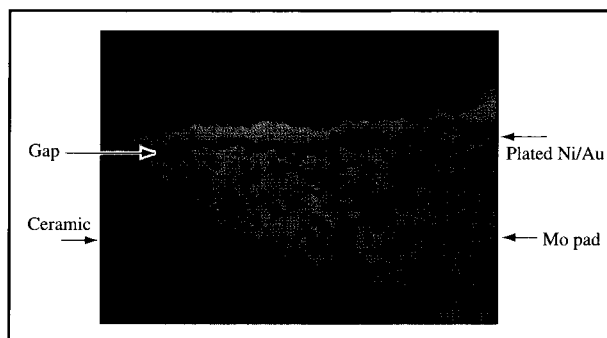


Figure 9

Cross-sectional optical micrograph of delamination at the Mo/Ni diffusion zone due to chemical attack.

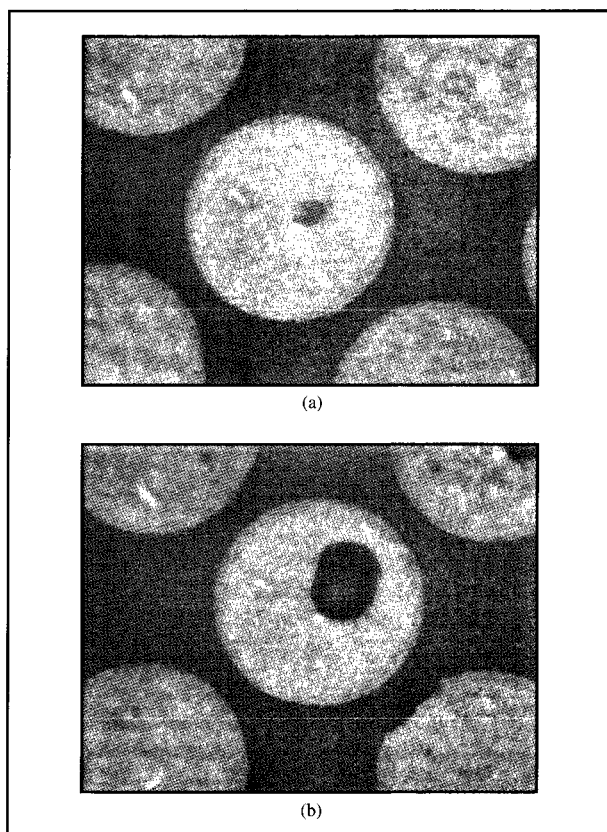


Figure 10

Optical micrographs of Ni/Au on Mo pad after thin-film processing: (a) before and (b) after tape adhesion test.

- *Reliability results and discussion*

Of the two types of thin-film metal shorts, intralevel and interlevel, the latter are very difficult to detect by visual

Table 3 Description of accelerated test conditions of thin-film modules following IBM and military specifications

Stress	Conditions
1. Thin-film opens and latent opens	
Thermal cycling	0/100°C, 3–5 kc (IBM) –25/125°C, 3–5 kc (IBM) –55/125°C, 1 kc (Mil-Std 883)
Thermal shock	–65/150°C, 1–3 kc (Mil-Std 883)
Temperature age	150–200°C/1–2 khr (Mil-Std 883)
Electromigration	150°C/300 mA, 1–3 khr (IBM)
2. Thin-film shorts and latent shorts	
Temperature/humidity/bias	85°C/85%RH/5–15 V, 1–4 khr (IBM)
Temperature bias	130–150°C/35–75 V, 1–2 khr (IBM)
Highly accelerated stress test	140°C/85%RH, 100–500 hr (IBM)
3. Bottom-surface metal and pin integrity	
Reflows	13× reflows
Thermal shock	–65/150°C, 1 kc (Mil Std 883)
Temperature/humidity/bias	85°C/85%RH/5 V, 2 khr (IBM)
Highly accelerated stress test	140°C/85%RH, 100–500 hr (IBM)
Mechanical stressing	Pin flexing/bending (1–5 lb forces)

inspection. Two potential sources for high-resistance or latent interlevel shorts were identified in the early evaluation stage. First, irregular topography due to contaminant particles or plating nodules can cause polyimide thinning, increasing the probability of interlevel shorts. Impurities in the plating baths occasionally produce plating nodules which can extend up to 5 μm above the metal layer, resulting in subsequent thinning of the overlying polyimide layer. Optimum controls of the plating bath chemistry minimized this problem. Second, it was found that the potassium borate step [used during Co(P) plating] followed by NaOH treatment (used for polyimide adhesion promotion) degraded the polyimide along the metal edge. The depth of the affected areas could be as much as half of the polyimide thickness. To correct the problem, the NaOH was replaced by an aminopropylsilane treatment for polyimide adhesion enhancement.

The extensive BSM feature corrosion, as discussed previously, resulted from the cumulative effect of multiple Cr etching steps. Parts which had not gone through rework showed only mildly damaged BSM pads. This posed more reliability risk, since the defects could not be detected but could decrease the pin pull strength significantly after thermal fatigue. The problem was

resolved by the implementation of BSM mechanical protection during Cr etching, as described earlier.

Successful results were obtained in all stress cells. More than 400 modules have been successfully tested, including the test vehicles and high-end server modules [6, 8, 22]. No fails were observed in thin films and BSM stress cells, as outlined in Table 3. The accelerated test results showed that the reliability of these modules far exceeded typical product lifetime requirements.

Summary

High-performance nonplanar thin-film structures have been successfully built for several generations of high-end systems. The criteria to select a wiring fabrication process, i.e., either subtractive etching or pattern electroplating, was defined in terms of metal linewidth and spacing, and metal thickness (Figure 5). The product yields from both processes were shown to be equivalent under manufacturing conditions; however, subtractive etching is preferred because of its lower cost.

Two processing concerns encountered during development of the processing for nonplanar thin-film structures were the accelerated etching of top-surface electroplated Cu lines during etching of a Cu seed layer, and galvanic etching of a Mo/Ni diffusion zone on the bottom-surface metallurgy during etching of thin Cr in the structure. A proprietary Cu seed-etch process was developed that eliminated the accelerated etching of isolated Cu features and also decreased etch differences between isolated and closely spaced pattern features. Corrosion at the bottom-surface metallurgy was eliminated by preventing contact between etchant and metallurgy with a vacuum-assisted mechanical protection fixture during all top-surface-metallurgy Cr etch steps. These actions ensured the manufacturability and reliability of nonplanar thin-film products.

Acknowledgments

There are many individuals to thank for the development and manufacturing efforts that allowed reliable, low-cost thin-film nonplanar fabrication, particularly the members of the thin-film development, thin-film manufacturing, and East Fishkill analytical teams.

*Trademark or registered trademark of International Business Machines Corporation.

References

1. R. R. Tummala and E. J. Rymaszewski, Eds., *Microelectronics Packaging Handbook*, Van Nostrand Reinhold, New York, 1989.
2. C. W. Ho, D. A. Chance, C. H. Bajorek, and R. E. Acosta, "The Thin-Film Module as a High-Performance Semiconductor Package," *IBM J. Res. Develop.* **26**, No. 3, 286–296 (May 1982).

3. M. Swaminathan, E. Perfecto, and K. Prasad, "Thin Film Multichip Module Technology at IBM—Design and Electrical," *Proceedings of the IEPS International Electronics Packaging Conference and Exhibition*, San Diego, September 12–15, 1993, pp. 10–17.
4. A. Iqbal, M. Swaminathan, M. Nealon, and A. Omer, "Design Trade-offs Among MCM-C, MCM-D and MCM-D/C Technologies," *IEEE Trans. Components Packag. & Manuf. Technol. B* **17**, No. 1, 22–29 (1994).
5. T. F. Redmond, C. Prasad, and G. Walker, "Polyimide–Copper Thin Film Redistribution on Glass Ceramic/Copper Multilevel Substrates," *Proceedings of the IEEE 41st Electronic Components and Technology Conference*, Atlanta, May 13–15, 1991, pp. 689–693.
6. E. D. Perfecto, K. Kelly, K. Lidestri, H. Longworth, T. Wassick, J. Pennacchia, M. Ellsworth, and A. Merryman, "MCM-D/C Application for a High Performance Module," *Proceedings of the ISHM/IEPS 5th International Conference on Multichip Modules*, Denver, April 17–19, 1996, pp. 69–74.
7. M. Ellsworth, H. Hammel, E. Perfecto, and T. Wassick, "A High Density, High Performance MCM-D/C Package: A Design, Electrical and Process Perspective," *Proceedings of the IEEE 46th Electronic Components and Technology Conference*, Orlando, May 28–31, 1996, pp. 821–828.
8. W. Shutler, H. Longworth, J. Pennacchia, E. Perfecto, and R. Shields, "A Family of High Performance MCM-C/D Packages Utilizing Cofired Alumina Multilayer Ceramic and Shielded Thin Film Redistribution Structure," *Inter. J. Microcirc. & Electron. Packag.* **20**, No. 3, 289–296 (1997).
9. G. Katopis, D. Becker, H. Smith, and H. Stoller, "MCM-C/D Design for the CMOS Implementation of the S/390 System," *Proceedings of the IEEE 47th Electronic Components and Technology Conference*, San Jose, May 18–21, 1997, pp. 479–485.
10. E. D. Perfecto, K. Prasad, C. Osborn, M. Swaminathan, G. White, and C. Prasad, "Comparison of Planar and Non-Planar Multi-Level Cu–Polyimide Interconnect," *Proceedings of the IEEE 43rd Electronic Components and Technology Conference*, Orlando, June 1–4, 1993.
11. K. Prasad and E. D. Perfecto, "Multilevel Thin Film Applications and Processes for High End Systems," *IEEE Trans. Components Packag. & Manuf. Technol. B* **17**, No. 1, 38–49 (February 1994).
12. T. E. Dinan and M. Datta, "Kinetics of Copper Etching in Acid Ammonium Persulfate Solutions," *Proceedings of the Symposium on High Rate Metal Dissolution Processes*, PV 95-19, The Electrochemical Society, Pennington, NJ, 1995, pp. 189–201.
13. K. K. H. Wong, S. Kaja, and P. W. DeHaven, "Metallization by Plating for High-Performance Multichip Modules," *IBM J. Res. Develop.* **42**, No. 5, 587–596 (1998, this issue).
14. Y.-H. Kim, G. F. Walker, J. Kim, and J. Park, "Adhesion and Interface Studies Between Copper and Polyimide," *J. Adhes. Sci. Technol.* **1**, No. 4, 331–339 (1987).
15. Y.-H. Kim, J. Kim, G. F. Walker, C. Feger, and S. P. Kowalczyk, "Adhesion and Interface Investigation of Polyimide on Metals," *J. Adhes. Sci. Technol.* **2**, No. 2, 95–105 (1987).
16. S. K. Ray, K. Beckham, and R. Master, "Flip Chip Interconnection Technology for Advance Thermal Conduction Modules," *Proceedings of the IEEE 41st Electronic Components and Technology Conference*, Atlanta, May 11–16, 1991, pp. 772–778.
17. E. D. Perfecto, S. Ray, T. A. Wassick, and H. Stroller, "Evolution of EC and Repair Technology in High Performance Multi-Chip Modules at IBM," presented at the IEEE 48th Electronic Components and Technology Conference, Seattle, May 26–28, 1998.
18. R. Messier, A. P. Giri, and R. A. Roy, "Revised Structure-Zone Model for Thin Film Physical Structure," *J. Vac. Sci. Technol. A* **2**, No. 2, 500 (1984).
19. L. T. Romankiw, "Pattern Generation in Metal Films Using Wet Chemical Techniques: A Review," *Proceedings of the Symposium on Etching for Pattern Definition*, H. G. Hughes and M. Rand, Eds., The Electrochemical Society, Pennington, NJ, 1976, pp. 161–193.
20. M. Pourbaix, *The Thermodynamics of Aqueous Solutions* (Translation), Edward Arnold Publishers, London, 1949.
21. T. A. Wassick and L. Economikos, "Open Repair Technologies for MDM-D," *IEEE Trans. Components Packag. & Manuf. Technol. B* **18**, No. 1, 154–162 (February 1995).
22. H. P. Longworth, E. D. Perfecto, and P. V. McLaughlin, "Reliability Evaluation of Multilevel Thin Film Structures," *Proceedings of the IEEE 44th Electronic Components and Technology Conference*, Washington, DC, May 1–4, 1994, pp. 482–486.

Received November 3, 1997; accepted for publication June 4, 1998

Eric D. Perfecto *IBM Microelectronics Division, East Fishkill facility, Route 52, Hopewell Junction, New York 12533 (perfecto@us.ibm.com).* Mr. Perfecto is a Senior Engineer in the IBM Microelectronics Thin Film Packaging Development group, East Fishkill, New York. He received his B.S. degree in chemical engineering from the University of Puerto Rico; he also received an M.S. degree (1982) in chemical engineering from the University of Illinois at Urbana-Champaign and an M.S. degree (1987) in operations research from Union College, New York. Mr. Perfecto joined IBM in 1982 at the East Fishkill facility, where he has worked on a number of thin-film technologies including photolithography, subtractive etching, lift-off processes, and joining metallurgy. He holds nine U.S. patents and has published more than 35 papers. He is a member of the IMAPS and IEEE, and a senior member and past President of the Mid-Hudson Chapter of the Society of Plastics Engineers.

Ajay P. Giri *IBM Microelectronics Division, East Fishkill facility, Route 52, Hopewell Junction, New York 12533 (giri@us.ibm.com).* Dr. Giri is a Senior Engineer in the IBM Microelectronics Interconnect Products group, East Fishkill, New York. He received his Ph.D. in solid state science from Pennsylvania State University in 1985, joining IBM that year. He received his B.Sc.(Hons.) in chemistry and M.Sc. in physical chemistry from the University of Poona, India. Dr. Giri has worked on a number of thin-film projects and has led process development in the areas of plasma processes, metal depositions, and materials. He received an IBM Outstanding Technical Achievement Award in 1990 for his contributions in thin-film development for ES/9000 systems. He has published numerous papers on thin-film microstructure vs. properties, thin-film packaging, electrochromic films, photogalvanics, and conservation of daguerreotypes, and he holds many patents.

Ronald R. Shields *IBM Microelectronics Division, East Fishkill facility, Route 52, Hopewell Junction, New York 12533 (shields@us.ibm.com).* Mr. Shields joined IBM as an engineer in 1974 after receiving his M.S. degree from the University of Maryland in chemistry. He is a Senior Engineer in the IBM Microelectronics Thin Film Packaging Development group, East Fishkill, New York, and is responsible for the S/390 thin-film program. He has worked in the Thin Film Packaging Development area for the past eight years; before that, he managed an engineering department in Substrate Packaging. Mr. Shields is co-author of several papers related to thin-film packaging technology; he holds several U.S. patents and is a member of the American Chemical Society and IMAPS.

Hai P. Longworth *IBM Microelectronics Division, East Fishkill facility, Route 52, Hopewell Junction, New York 12533 (longworth@us.ibm.com).* Dr. Longworth is an Advisory Engineer in the IBM Microelectronics Ceramic Packaging group and is responsible for reliability assurance and product qualification of mostly high-end products. She joined IBM in 1992 after receiving an Sc.D. in electronic materials engineering from the Massachusetts Institute of Technology. She received an M.S. in metallurgical engineering from Michigan Technological University, a B.S. in physics, and a B.S. in chemistry from Saigon University. Dr. Longworth had worked as an analytical chemist and supervisor at Howmet Corporation Technical Center in Michigan. She has published 14 papers on microstructures vs. properties, electromigration, thin film, and packaging reliability evaluation.

John R. Pennacchia *IBM Microelectronics Division, East Fishkill facility, Route 52, Hopewell Junction, New York 12533 (pennacch@us.ibm.com).* Dr. Pennacchia received his Ph.D. in polymer chemistry from Polytechnic University in Brooklyn, New York, in 1986. He joined the IBM General Technology Packaging Development Division in 1986 as an engineer working on thin-film technology and process development in the areas of polymer and photoresist process development. From 1986 to 1989, he was responsible for process development, coordination, and program integration for IBM's thin-film efforts for the ES/9000 mainframe computer. In 1989, Dr. Pennacchia became a Development Engineering Manager in the Thin Film Development area; he is currently the Thin Film project manager in the IBM Microelectronics Ceramic Packaging group.

Mathias P. Jeanneret *IBM Microelectronics Division, East Fishkill facility, Route 52, Hopewell Junction, New York 12533 (jeannm@us.ibm.com).* Mr. Jeanneret is a Staff Engineer at the IBM Microelectronics Packaging Laboratory, East Fishkill, New York. He received an M.S. degree in physics from the Universidad de Chile, Santiago, in 1985 and an M.S. degree in metallurgical engineering from the University of Illinois at Urbana-Champaign in 1988. Since joining the East Fishkill facility in 1988, he has worked on a number of projects related to thin-film technologies, particularly in the area of photolithography.