

Electrochemical process for advanced package fabrication

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Interconnections for high-end applications are essentially low-resistance transmission-line structures with precisely controlled cross-sectional shapes and dimensions. The relatively thick copper conductors—typically 6 μm or more—combined with the stringent control required on the 10–20- μm -wide cross sections stretches the capabilities of the subtractive etch and lift-off processes that are typically used in semiconductor fabrication to pattern evaporated and sputtered metal films. Electroplating through a photoresist mask, which has proven itself to be a highly effective, precision manufacturing process for thin-film magnetic recording heads, is, however, capable of meeting and far exceeding the requirements of package fabrication. This paper describes the fabrication of a package structure that integrates traditional dry-process technologies with electrolytic copper plating to form the conductors, polyimide backfill and planarization steps to form the dielectric, and electroless deposition to selectively clad the copper lines to prevent adverse reaction of the copper with water generated during the polyimide cure. The discussion highlights salient issues which are

pertinent to the compatibility of the individual process steps and to the extension of the technology to more demanding packaging structures and to other applications.

Introduction

The interconnections which carry the pulses between chips in a high-performance multichip module are essentially low-loss transmission lines with precisely controlled propagation characteristics. These lines are typically part of a thin-film multilevel structure containing two ground plane levels, x and y wiring levels (some advanced designs may contain two x – y wiring pairs), and, usually, capture pad and chip-joining top-surface metallurgy levels [1]. Performance requirements dictate that these structures have precisely controlled electrical characteristics to minimize pulse distortion. Today's multichip package designs call for individual lines and vias with dimensions in the 10–20- μm range to allow high wiring densities and to minimize pulse propagation time. While thin-film multilevel interconnections have been built using lift-off and subtractive etch processes [2], the fabrication requirements of the more advanced structures are most advantageously met by the appropriate use of electroplating operations. This paper describes the dual-layer polyimide (DLP) process, in which an integrated

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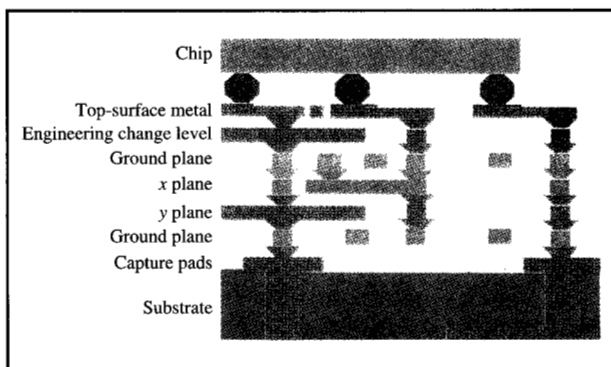


Figure 1

Schematic cross section of the multilevel, thin-film wiring on a high-performance multichip module.

combination of appropriate electrochemical and traditional wet and dry technologies has been used to advantage to fabricate an advanced multilevel interconnection structure. The name DLP highlights the fact that insulation layers for a wiring level and its associated via level are formed concurrently in a single operation, thus simplifying the dielectric application and planarization operations. The discussion highlights salient issues which are pertinent to the compatibility of the individual process steps and to the extension of the technology to more demanding packaging structures and to other applications.

• Structure

A schematic cross section of the multilevel interconnection wiring structure is shown in **Figure 1**. The wiring structure consists of a ground plane, two planes with orthogonal conductors referred to as *x* and *y* planes, respectively, a second ground plane, a level of wiring for engineering changes (EC), and a top layer which provides test pads and chip attachment metallurgy. The thin-film wiring structure is built on top of a ceramic substrate which contains the power distribution wiring and an associated array of pads. Since a slight distortion of the pad array inevitably occurs during firing of the ceramic, an additional level of capture pads is included in the multilevel structure to ensure registration to the studs in the cofired ceramic. Vias interconnect the various levels according to the needs of the circuit design. Many of these interlevel connections, such as those in Figure 1 which connect the top-surface metallurgy to the *y* plane or to the substrate wiring, entail stacks of vias.

The structures described in this paper were designed as test vehicles to assess the electrical performance of multilevel interconnect structures. The electrical tests did

not require the presence of powered chips, and so it was sufficient to use planarized glass rather than a ceramic brick as the substrate with power distribution wiring. Using a glass substrate obviated the need for the capture pad level. Since the EC level was not required for the electrical tests, it was omitted in many of the fabricated structures.

Each conductor layer and each insulator layer in the multilevel interconnection wiring is 6 μm thick. The test vehicle design includes transmission-line patterns with nominally 9-, 12-, and 15- μm linewidths, all on a 45- μm pitch, and via chain structures with 15-, 18-, and 23- μm -diameter vias. This design is intended to produce a characteristic impedance of 30 to 40 Ω for the 15- μm -wide lines when the dielectric constant of the insulator is 3.5. (Since there is no ground plane separating the *x* and *y* levels, the actual characteristic impedance depends on the degree of fill in the adjacent wiring level.) The overall substrate dimensions are those of a standard 127-mm $\times$ 127-mm module.

From a fabrication point of view, meeting the performance requirements for the interconnect structure translates into a) maintaining precise spacing between conductor planes, b) fabricating conductors with precisely defined cross-sectional shape and dimensions, and c) incorporating a low-loss insulator with appropriate dielectric constant. Selection of the dielectric and details of dielectric processing are beyond the scope of the paper. In this particular case, polyimide was chosen for its relatively low dielectric constant and for its ability to withstand a 400°C temperature during C4¹ solder joining of the chips. The choice of polyimide leads to the potential of an adverse interaction between copper and H₂O, which is a by-product of the polyimide cure, to form Cu₂O at the Cu-polyimide interfaces. In time, the Cu₂O will migrate into the polyimide, resulting in Cu₂O particles in the dielectric near the Cu interface which will degrade the dielectric properties of the polyimide [3]. This effect was prevented by introducing an electroless deposition step to create a Ni(P) or Co(P) barrier layer on the copper prior to forming the polyimide insulation [4].

• Electroplating for conductor fabrication

The process of choice to meet the requirement of precise shape and dimension, particularly for thick conductors, is electroplating through a lithographically defined mask. In contrast to subtractive etching or lift-off, which are alternative approaches to forming multilevel interconnect wiring, through-mask plating is an atom-by-atom molding process which precisely replicates the cross section of the lithographic stencil down to atomic dimensions [5, 6]. The viability of through-mask plating as a precise

¹ Controlled collapse chip connection.

manufacturing process has been proven by nearly twenty years of use in thin-film head manufacture and by the fact that virtually all of the inductive thin-film heads today are produced by this process. Since packaging and thin-film heads have comparably demanding fabrication requirements [7-9], the experience that was gained and the extensive scientific understanding of electrochemical processes that was developed in the thin-film head work has direct bearing on the application of electrochemical technology to package fabrication.

Precise control of the thickness of the conductors must be maintained across the entire substrate at each level, since the height of the plated copper influences the characteristic impedance of the transmission lines and, thus, the electrical behavior of the structure. This requirement dictated that the plating system be designed to achieve uniform mass transfer and uniform secondary current distribution across the entire substrate. Tool design concepts and the in-depth understanding of electrochemical processes that had been developed to address the uniformity requirements of the thin-film head industry were carried over into the plating processes for the multilevel package.

The paddle cell [10], which is the proven workhorse of the thin-film head industry, was chosen to do the copper plating in the package. The parallel-plate electrode configuration of this cell and the insulating sidewalls which are perpendicular to the electrodes promoted straight field lines and uniform current density. The paddle, which moves in close proximity to the workpiece, provided the controlled, uniform agitation necessary for uniform mass transfer right at the surface where the agitation was needed. The extensive modeling on processes in this type of cell provided the understanding necessary to achieve optimum uniformity in the multilevel package described here [11-13]. In particular, the models showed how current distribution could be optimized by the use of auxiliary electrodes and by the design of the pattern being plated.

The need for an auxiliary electrode to optimize uniform current distribution across the surface of the workpiece stems from the fact that the paddle must travel beyond the edge of the substrate to ensure uniform agitation across the active substrate area. However, moving the insulating sidewalls of the cell back from the substrate edges to make room for the paddle creates a nonuniform potential field which causes the current lines in the electrolyte beyond the edge of the substrate to crowd in toward the substrate. By adding an independently powered electrode to the cathode assembly beyond the substrate, a controlled portion of the current can be diverted from the substrate to avoid the increase in current density at its outside edge. The work of Mehdizadeh et al. [11], which shows how the current distribution across the substrate

can be predicted quantitatively in the presence of an auxiliary electrode, provided valuable guidance in optimizing plating uniformity.

Current distribution is also affected by the lithographic pattern. The density of the resist pattern (i.e., the fraction of the surface covered by resist) and variations in this density from point to point across the substrate determine the uniformity that can be achieved in the plating process. Mehdizadeh et al. [12] have considered these effects by describing the lithographic pattern as a continuous distribution of "active-area density" and developing a model to predict the current to individual features as a function of the active-area density of the surrounding region. Factors which minimize pattern-driven nonuniformities include a low plating rate, high bath conductivity, and mild variations in the active-area density across the substrate. It is important to examine the lithographic pattern in the context of the work of Mehdizadeh et al. for any through-mask plating application where plating uniformity is important. Fortunately, the conductor patterns in the typical wiring level of the packaging structure show little variation in active-area density across the wafer. This characteristic, in combination with the high conductivity of the acid copper bath and a low plating current density, facilitates excellent thickness control across the substrate.

Fabrication process

The fabrication process for any given level entails forming a conductor pattern for that level on a planar surface, forming via studs on the conductors as required, filling the structure with a dielectric, and planarizing the surface. (The ground plane is actually a patterned mesh; from the fabrication point of view, the operations to build a ground plane or a wiring plane are identical.) Building the structure of Figure 1 can then be regarded as a repetition of these process steps for each desired level.

Figure 2 shows the process sequence used to build one level of conductors and vias. For all levels except the first, the starting surface was the planarized polyimide surface of the preceding level with flush, exposed vias. The first level was also built on planarized polyimide, but there were no vias present, since the underlying substrates for the test vehicle described in this work were blank glass plates. This initial polyimide layer was applied and planarized using steps similar to that described below to form the insulation for each conductor level. The unstructured polyimide layer was included to improve the planarity of the glass and ensure that the starting surface was flat to better than 0.5 $\mu\text{m/in.}$ across the entire plane.

Formation of the wiring pattern for any given level began by sputter-depositing a Cr-Cu seed layer on the planarized surface of the preceding level [Figure 2(a)].

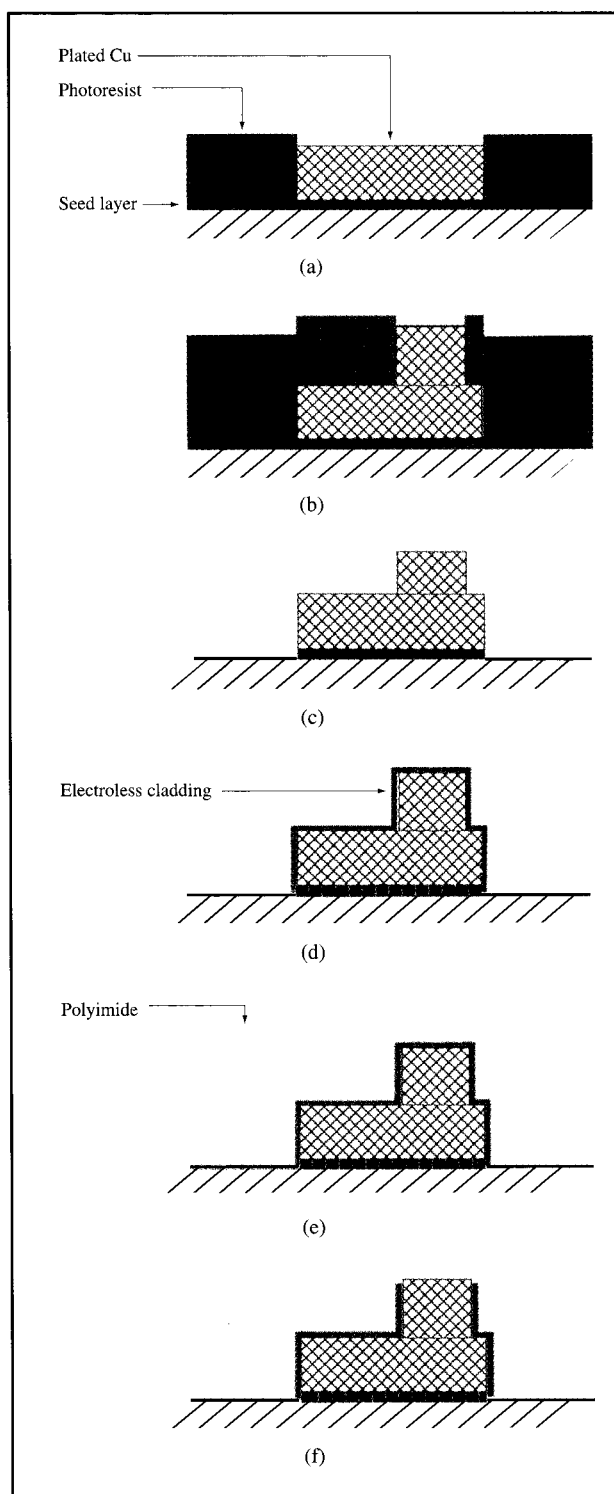


Figure 2

Drawings (a) through (f) represent the process sequence used to fabricate one conductor and via level by the DLP process. This sequence of steps is repeatedly carried out on top of the previously completed level until the multilevel structure is completed.

A 20-nm Cr layer was used to promote adhesion of the Cu to the polyimide. Copper thickness of 300 nm was more than enough to ensure negligible ohmic drop across the typical-size packaging substrate during plating. The Cu was next given a one-minute etch in 10% sulfuric acid to create a clean, standardized surface. A layer of Shipley SJR 1440 photoresist² was then spun on, exposed, and developed to form openings for the wiring pattern. The thickness of the photoresist was slightly greater than the thickness of the wiring to ensure that the plating did not mushroom above the top of the resist. After development, the pattern was ashed in an argon-5% oxygen plasma at 50 W in an LFE 301C asher for three minutes to ensure that there was no residual photoresist in the openings which would interfere with uniform initiation of plating.

Electroplating of copper was done in a paddle cell [10] using Sel-Rex CuBath-M³ copper plating solution, a commercial acid copper sulfate bath which produced deposits with near-bulk resistivity. The paddle cell was the tool of choice for this work because, as indicated above, it has proven itself in providing the uniform agitation which is one of the necessary conditions for achieving uniform plating across large substrates. With proper tool design to ensure uniform current density across the substrate, the thickness of the copper wiring was determined by the deposition time and current.

Vias to the next level were formed after plating the wiring pattern by removing the wiring conductor lithography, applying a new layer of photoresist with sufficient thickness to provide at least 6 μm of resist on top of the copper, and exposing and developing the stud pattern. Development was again followed by a three-minute ash in an argon-5% oxygen plasma to ensure that there was no residual resist on the Cu. The studs were then plated using the same plating process as for the wiring [Figure 2(b)].

The next operation, removal of the seed layer, entailed separate steps to first etch the Cu and then the Cr. After the resist was stripped, the copper layer was spray-etched with an etchant containing 10 g/l ferric ammonium sulfate and 10 cc/l sulfuric acid. The Cr adhesion layer was spray-etched at 60°C with a solution containing 60 g/l of potassium permanganate and 200 g/l of tribasic sodium phosphate. This etch was followed by a spray rinse in 10 g/l oxalic acid to remove solid residue from the KMnO_4 process. The wiring pattern was not masked for this etch step, since even with a factor of 2 over-etch to ensure complete removal of the copper seed, only about 0.5 μm of copper was lost from the lines. Adequate control of the final line thickness was maintained by depositing sufficient additional Cu during the plating operation to compensate

² Shipley Company, Marlborough, MA.

³ Trade name of Sel-Rex, a division of Enthone-Omni, New Haven, CT.

for the Cu lost during seed-layer removal. Figure 2(c) represents the structure after seed-layer removal.

As indicated earlier, a Co(P) barrier layer must be deposited on the Cu metallization to prevent the reaction of the Cu with H₂O produced during the polyimide cure cycle and the consequent formation of Cu₂O particles in the polyimide dielectric. A properly oxidized Co(P) deposit, in addition to forming a barrier layer, will also enhance the adhesion between the copper and the polyimide which is applied in the next step. Details of the electroless deposition process used to form the Co(P) layer and of the oxidation step to improve adhesion to the polyimide are described in another paper in this journal [4]. As depicted in Figure 2(d), the cladding process provides a Co(P) barrier on the tops and sides of all conductors and studs.

A dual layer of insulation to concurrently form the dielectric in the via and stud levels was provided by spinning on and curing a version of Du Pont PI-2611 biphenylene dianhydride-phenylenediamine (BPDA-PDA) polyimide⁴ formulated to IBM specifications. Before applying the polyimide, the part was subjected to a water plasma treatment to enhance the adhesion of the applied polyimide to the cured polyimide of the previous layer.⁵ The polyimide was spun on in three layers to ensure complete filling of all the crevices in the wiring structure and to achieve partial planarization of the cured polyimide surface. The first layer, a 10% solution of PI-2611 in *n*-methylpyrrolidone (NMP) followed by a 95°C bake, provided initial wetting of all surfaces of the structure. This layer was followed by application of a 50% solution of polyimide in NMP using a slow ramp-up of the spin speed to achieve complete filling of the narrow spaces of the pattern. Following a second 95°C bake, full-strength BPDA-PDA was applied and cured according to the manufacturer's recommended cure cycle. Applying the polyimide in the manner just described resulted in a partially planarized surface in the cured polyimide, as depicted in Figure 2(e). The spin speeds were adjusted so that the thinnest portions of the cured polyimide were 1 to 2 μm above the final polished thickness.

The final planarization and polishing were done mechanically using an 0.05- μm alumina slurry. Table rotation speed and quill rotation speed and pressure were optimized for uniform polishing across the part. The topography in the polyimide above the metal features was removed in the initial stages of polishing. Continued polishing then brought the dielectric to its final thickness. Since the polyimide application was controlled so that the prepoly thickness was within 1 to 2 μm of the final

value, very little polyimide had to be removed, contributing to tight control of the final thickness. The completed level with planarized surface is shown in Figure 2(f). From this point, fabrication continued with the next level by depositing a new seed layer on the planarized surface and repeating the sequence of steps in Figures 2(a) through 2(f).

Results

The fabrication of the multilevel structure was assessed by SEM examination of the structure; by measuring the resistivity of the deposited copper, the resistance of vias which interconnect conductors on different levels, and the isolation resistance between adjacent conductors; and by determining the pulse-propagation characteristics of transmission lines which were designed into the structure for this purpose.

• SEM observations

The SEM work was carried out on a sample in which the polyimide in a region of the structure was completely removed by extended ashing in an oxygen plasma. This ashing stripped away the exposed polyimide down to the substrate and allowed SEM images of all conductor levels to be obtained. The SEM in Figure 3 shows contact pads, which are part of the top-surface wiring, and the upper mesh ground plane. Two rows of via chains can also be seen in the foreground. Figure 4 shows the stacked vias with 11 layers of metallurgy in one of these chains. This SEM was taken at a shallow angle and shows all of the levels of the structure below the top-surface wiring. The well-defined edges of the conductors, their highly vertical profiles, and the good alignment of the via stacks seen in these figures are characteristic of plated-through-mask structures and are typical of all of the parts which were examined during the course of this work.

• Copper resistivity

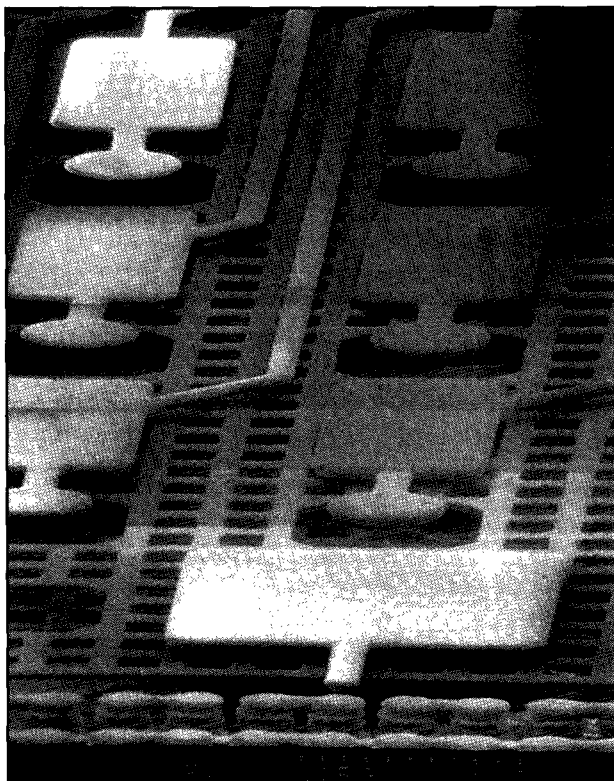
Conductor patterns designed for four-point probe measurements were used to determine the resistivity of the plated copper. Resistivity was calculated from the dimensions of the pattern and the measured resistance. The effects of slight uncertainties in the dimensions of these patterns stemming from variations in the fabrication process were minimized by individually measuring the line width and thickness for each of the structures used for the resistivity determination. The calculated resistivity for all samples on which these measurements were made fell between 1.6 and 1.7 $\mu\Omega\text{-cm}$, showing that the resistivity of the plated conductors was essentially that of bulk copper.

• Via resistance

The resistance associated with the vias which interconnect different levels of the structure was determined by

⁴ E. I. du Pont de Nemours & Co., Wilmington, DE.

⁵ R. D. Goldblatt, L. M. Ferreira, S. L. Nunes, R. R. Thomas, N. J. Chou, L. P. Buckwalter, J. E. Heidenreich, and T. H. Chao, "Characterization of Water Vapor Plasma Modified Polyimide," IBM internal publication, November 19, 1991.



SEM photograph of completed structure showing top-surface metallurgy and top side of upper ground plane. Polyimide has been ashed away to allow the copper structure to be seen in the SEM.



SEM photograph showing a via stack with 11 levels of metallurgy. (Polyimide has been ashed away as in Figure 3.)

measuring the total resistance of a chain of 3000 vias joined together by links which alternate between the x and y planes. A portion of such a chain is shown in **Figure 5**. The pattern contained chains with nominally 15-, 18.4-, and 23- μm vias. Resistance measurements for these via chains on ten different samples are shown in the bar chart in **Figure 6**. The relatively large spread among the via-chain resistances for the first three samples is attributed to the fact that these parts were among the first ones fabricated; it reflects the variability in conductor dimensions associated with early learning and refining of the process. The seven later samples showed excellent consistency among the measurements on different parts and demonstrated the high degree of control that can be attained in this process.

The total chain resistance was also calculated using the measured resistivity of the electroplated copper and the dimensions of the structure. Taking into account the expected dimensional variations in the structure as actually fabricated and approximations made in calculating the resistance of the chain, the total resistance for the

chain with 18.4- μm vias was predicted to be between 20 and 24 Ω . The average measured total resistance of the chains with 18.4- μm vias for the parts in **Figure 6** that were built after the initial learning period was 20.6 Ω , which is within the expected range. Furthermore, the fact that the resistance is at the low end of this range supports the belief that the interfaces between the various processing levels in a plated structure do not make an excess contribution to the interlevel resistance. (Processing issues leading to excess interlevel resistance are considered in the discussion below.)

• Isolation resistance

Isolation resistance measured between closely spaced adjacent conductors gives an indication of such processing deficiencies as incomplete removal of the seed layer, spurious electroless deposition of the Co(P) capping material on the polyimide, underplating due to lifting of the resist during electrodeposition, gross lithography problems which create unwanted openings in the plating mask, and process-induced changes in the polyimide which

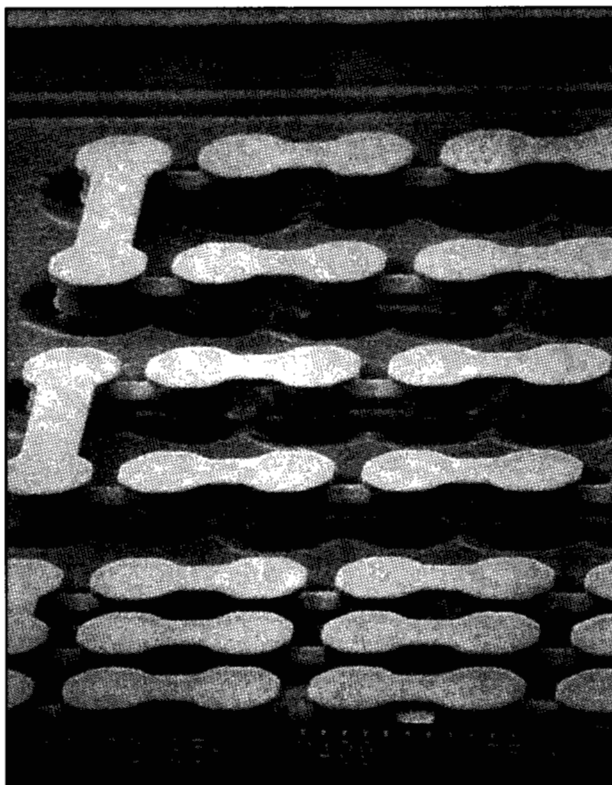


Figure 5

SEM photograph of a section of the via chain structure used for via resistance measurements.

alter its insulating qualities. Each of the fabricated structures included isolation test sites on both the x and y levels containing electrically isolated, parallel conductors on a $45\text{-}\mu\text{m}$ pitch. The conductor patterns had an effective length of 6 cm and were folded into a serpentine pattern to fit the allotted space on the test vehicle. The folding also created corners, which tend to be more vulnerable to some of the processing problems mentioned above. Nominal conductor widths of the respective test patterns were 9, 12, or $16\text{ }\mu\text{m}$, thus providing the ability to evaluate isolation at conductor separations of 36, 33, and $29\text{ }\mu\text{m}$. **Figure 7** summarizes the measurements made at such test sites on four different samples. Isolation resistance on all of the test sites was in the gigaohm range, thereby demonstrating that processing issues were sufficiently well understood and controlled to avoid the potential problems mentioned above.

• Pulse propagation

The ultimate electrical test of the structure is, of course, the ability to faithfully propagate a data pulse. A

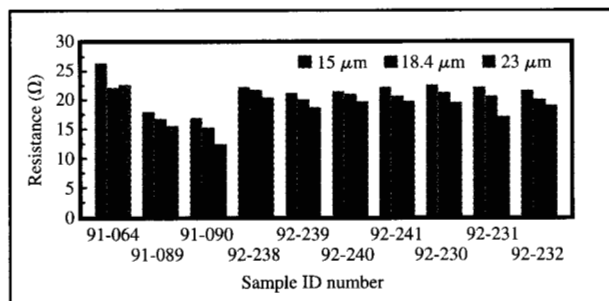


Figure 6

Total chain resistance for 3000 y - x vias as measured on ten different samples. Each sample had three different sizes of vias, as indicated in the figure.

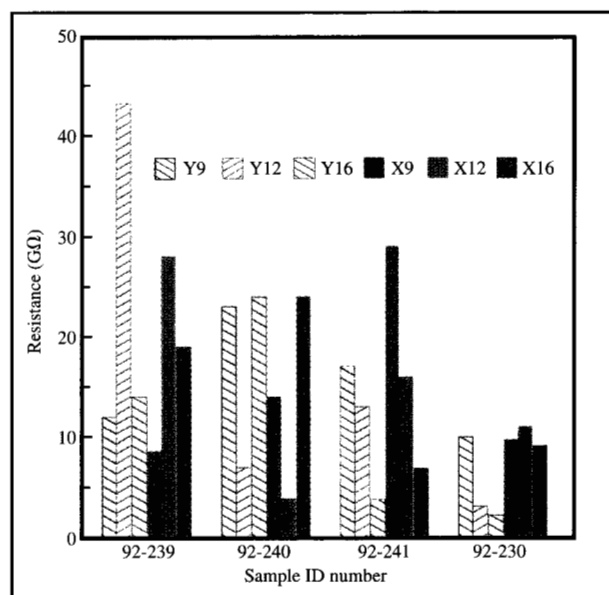


Figure 7

Leakage resistance as measured on four different samples between adjacent serpentine lines of test sites containing 9-, 12-, and $16\text{-}\mu\text{m}$ lines on a $45\text{-}\mu\text{m}$ pitch. Measurements were made at sites on both the x and y levels. The various shadings on the bars are defined in the legend and indicate the linewidth and test site location for each measurement.

perspective of the functional characterization of packaging structures has been presented by Ellsworth et al. [14].

Table 1 shows a typical set of measured and predicted values of characteristic impedance and of pulse-propagation behavior on transmission lines of different length which were built into the structure to evaluate

Table 1 Electrical performance of transmission lines in test vehicle.

	Characteristic impedance (Ω)	Propagation delay (ps)	Rise time (35 ps at input) (ps)
3.12-cm line			
Measured	34.3	74.6	82.6
Predicted	30.8	70.5	—
5.29-cm line			
Measured	33.8	75.9	136
Predicted	30.8	70.5	—

these properties. The predicted values were based on the geometric dimensions of the transmission-line structure and the dielectric constant of the polyimide. Pulse-propagation behavior was assessed by sending a pulse with a 35-ps rise time down the respective line and measuring the delay and rise time at the far end. The measured impedance and propagation delay showed good agreement with the design values, and the rise times of the transmitted pulses were well within the requirements of the intended packaging application. Since these parameters are dependent on precise control of the geometric dimensions and material properties during fabrication, the observed pulse-propagation behavior confirmed the precision with which the fabrication process replicated the design. The fact that the rise time for the propagated pulse was within the expected range is a good indication that the various steps and thermal cycles used in the process did not adversely affect the properties of the dielectric and, in particular, confirms the effectiveness of the Co(P) capping layer in preventing formation of Cu_2O particles in the dielectric.

Discussion

• Via resistance

The multilevel package is effectively a three-dimensional structure, so that the vias which interconnect the different levels are a critical factor in determining its performance. There has always been the concern in building multilayer structures that residues and oxidation or other tarnishing layers from previous process steps would contribute to excess resistance between levels. The photolithography steps used to define the pattern openings for both the via and the conductor levels are particularly likely sources of residue, and care had to be taken to ensure complete removal of all traces of resist at the bottom of the pattern openings. This requirement was met by optimizing the exposure and development parameters to favor complete development (sometimes at a slight sacrifice in replicating

the lateral dimensions of the mask) and by introducing an ashing step before plating. The plating electrolyte, in combination with the pre-plating etch step, was sufficiently aggressive to remove any slight oxidation on the underlying copper including that caused by the ashing process.

The through-mask plating process offers the advantage that the effects of any residue are visibly apparent as soon as the part is removed from the plating bath. If any residue is present, plating may not take place in the affected regions of the pattern; if plating does occur, the deposit will be rough, with a cauliflowerlike structure. In either case, the defect can be seen under visual inspection. In a lift-off process, on the other hand, the metallization would appear to be normal, although the interface could have a very high contact resistance which would not be detected until the completed structure was tested electrically.

• Seed-layer removal

The use of wet spray etching rather than ion milling or sputter etching to remove the seed layer deserves special mention because it illustrates how the side effects of a particular fabrication operation can adversely affect a subsequent processing step. Ion milling and sputter etching have generally been used in preference to wet etching to remove the seed layer in previously reported applications of through-mask plating [7, 8]. Among the factors prompting this choice were the absence of electrochemically driven modifications of etch rate, a general preference for dry process technology, and the belief that better resolution and control can be achieved with ion milling than with wet etching. However, physical sputtering processes, including ion milling, suffer from redeposition of the etched material onto other parts of the structure, particularly the vertical walls of the conductors. This redeposition adversely affected the initiation of the electroless Co(P) plating and the adhesion of the Co(P) to the sidewalls of the conductors. Spurious Co(P) was also deposited on the insulator surface wherever there were high levels of redeposited Cu. Thus, in spite of the usefulness of ion milling and sputter etching in other applications of through-mask plating, the wet spray etching process for seed-layer removal as described earlier was chosen in this work to achieve compatibility with the electroless Co(P) cladding operation.

• Package fabrication and MEMS technology

The basic processes described in this paper for multilevel packaging have also been used to fabricate an operating variable-reluctance minimotor [15, 16] which is believed to be the first reported multilevel MEMS structure to be formed using batch-fabrication technology. A close connection between the DLP process described in this

paper and MEMS fabrication should not be surprising in light of the observation by Frazier et al. [17] that the thin-film head plate-through technology, which provided the groundwork for the DLP process, was the forerunner of LIGA fabrication. (LIGA is an acronym coined from the German words Lithographie, Galvanoformung, Abformung (lithography, electroplating, and molding) to describe a fabrication process for MEMS structures based on through-mask electroplating [18].) The motor fabrication involved forming a 60- μm -thick copper conductor layer, a second magnetic layer with comparably thick patterned magnetic poles, and another copper conductor layer which was interconnected by vias to the first copper layer to form a coil wound around the magnetic poles. Each layer was made by a sequence of process steps similar to that used in the multilayer package work which included lithography, through-mask plating, seed-layer removal, dielectric backfill, and planarization. The motor fabrication process, which drew extensively on the DLP work, is just one example of the extension of the package fabrication technology to the thicker dimensions of MEMS structures; other applications can be found in recent review papers dealing with plating technology in electronic applications [19, 20].

The package fabrication work was cited above as a precursor to building the motor, but advances in MEMS technology are equally important to packaging fabrication. The process issues encountered in both applications are similar. However, because MEMS structures are usually more than an order of magnitude thicker than packaging structures, processing difficulties are exacerbated. Consequently, state-of-the-art advances in MEMS processing can usually be practiced with greater ease when applied to package structures and thus can enhance the robustness of a package fabrication process. The recent work of Lochel et al. [21], who have shown patterns up to 100 μm thick which were plated through optically exposed novolak-type resists, illustrates an advance in high-aspect-ratio lithography that is relevant to package fabrication.

Conclusions

A complete fabrication process in which all conductors and vias were formed by through-mask plating has been developed to fabricate the thin-film interconnection wiring in a high-performance, multilevel chip carrier. Electrical measurements on the completed structure demonstrated that the through-mask plating process provides the precision necessary to meet the performance requirements of the package. The process described here is based to a large extent on the through-mask plating process originally developed to fabricate thin-film magnetic recording heads. The successful extension of the latter technology to multilevel packaging structures was aided significantly by the in-depth understanding of electroplating science that

grew out of the thin-film head program. Continued work on the underlying science throughout the packaging program contributed to the precision and control of the process for the packaging application. The technology described here for multilevel package fabrication is also finding application in the fabrication of MEMS structures. In turn, advances in MEMS technology can contribute to improvements in multilevel package fabrication.

Acknowledgments

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