# Applications of electrochemical microfabrication: An introduction

by M. Datta
*Guest Editor*

Global competitive pressures and the ever-increasing demand for faster, smaller, less expensive electronic systems have produced fundamental changes in processing technologies. A variety of microelectronic components are manufactured with high-yield, cost-effective electrochemical processing. Electrochemical microfabrication uses electrochemical methods to create thin- and thick-film-patterned microstructures.

Electrochemical deposition (plating) is the oldest industrial application of an electrochemical reaction. Both electroplating and electroless plating processes deposit pure metals or alloys from metallic ions in solution. Plating also enables tailoring of the deposit's electrical, mechanical, and magnetic properties, brightness, color, and resistance to corrosion. Electrochemical metal-removal processes include electrochemical machining, electropolishing, chemical etching, and electroetching.

Electrochemical processing through polymeric photoresist masks is a primary technique for microfabrication of high-density patterned structures [1]. Photolithography is the exposure of photosensitive resist to ultraviolet light to transfer an original image. Advances in optical lithography have continued to meet increasing demands for high-resolution patterning [2]. Using X-ray lithography, it is possible to pattern advanced three-dimensional structures in which high-aspect-ratio profiles with minimal distortion are required.

Storage, packaging, device fabrication, and several other aspects of microelectronics have been affected by electrochemical processing. This topical issue on electrochemical microfabrication contains ten papers from IBM and one from the Georgia Institute of Technology that are associated with applications of "wet" electrochemical processing in microelectronics. This introduction outlines aspects of microelectronic devices and packaging technology to illustrate the role of electrochemical microfabrication and provide a framework for the included papers. This issue may be considered a follow-on to a previous issue of the *Journal* which focused on fundamental aspects of electrochemical science [3].

## Microelectronic devices and packaging

At the heart of every microelectronics system is an integrated circuit (IC) chip that becomes part of the functioning system via a packaging hierarchy. The package enables the distribution of power and signals as well as heat dissipation and package protection. In addition to electronic ICs, the chip or device level of a computer can be composed of discrete or integrated devices such as detectors, diode lasers, and photonic or optoelectronic ICs. These devices communicate through electrical or optical pathways in the form of, e.g., thin-film wiring and metal or organometallic bonding residing within the packaging hardware. Chips, with transistors, have layers of wiring stacked above to interconnect the transistors to one another and ultimately to the rest of the computer. As the number and diversity of devices increase, communication between the devices and the packaging hierarchy becomes increasingly complex. The number of levels within a hierarchy varies with the degree



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of integration and the packaging needs. A typical electronic package hierarchy for a high-performance computer consists of chips, chip carriers or modules, printed-circuit cards, printed-circuit boards, and gates [4]. Electrochemical microfabrication has advanced each level of microelectronic packaging.

Copper wiring on IC chips, introduced by IBM in September 1997 [5], uses low-cost electrolytic plating [6]. Copper wires conduct electricity with about 40 percent less resistance than traditional aluminum wires, leading to faster microprocessors, and are less vulnerable to electromigration, which ultimately induces wiring failures. In this issue, Andricacos, Uzoh, et al. describe the damascene process for fabrication of copper chip interconnections. By selecting appropriate conditions, electroplating within trenches can be made to occur preferentially at the bottom of the trenches, leading to void-free deposits. This paper presents experimental results and mathematical modeling of Cu profile evolution in trenches during damascene plating.

An important packaging application, not discussed in this issue, is the extendability of the controlled collapse chip connection (C4) process by electrochemical microfabrication. A chip is attached to a substrate that contains the wiring structure for the power and signal connections. Compared with other methods of interconnecting chips to a substrate, such as tape automated bonding (TAB) and wire bonding, the C4 process provides the following advantages [4]: short interconnection distances, which allow fast signal responses and low inductances, and area array bonding pads, which provide uniform power and heat distribution. The fabrication of PbSn C4 interconnections by evaporation through a metal mask, pioneered by IBM [7] in the 1960s, provides a highly reliable high-density process. However, the more than 95% of the material that is deposited on the evaporator wall and on the metal mask must be cleaned and the waste disposed of by an expensive, regulated procedure. The evaporation process is further limited by thermal mismatch between mask and wafer and the inability to produce high-aspect-ratio metal masks. The electrochemical fabrication of C4s, which is a highly selective and efficient process [8], is extendable to larger wafers, a wider range of alloys, and finer C4 dimensions than are possible by evaporation; it has thus become the process of choice for various applications.

To reduce package size and weight and achieve high performance and reliability, the electronics industry is moving from single-chip to multichip module (MCM) packages [9, 10]. A multilevel package structure contains a repetition of several conductor and via levels. As package designs become more aggressive, the internal wiring dimensions approach those of the thin-film wiring on the chip. To maintain a low resistance in package wiring, a reduced lateral wiring dimension requires conductor film thickness to increase. Dry chip metallization processes must be pushed to their limits to achieve the 5–10-$\mu$m conductor film thickness needed for packaging. In conjunction with high-aspect-ratio lithography, electrochemical microfabrication offers the possibility of readily producing thick conductors with lateral dimensions in the submicrometer range if required [11].

Four papers in this issue discuss the fabrication of thin-film multichip modules. Krongelb et al. and Wong et al. describe the use of through-mask electroplating in the development of IBM's advanced packages. Krongelb et al. discuss the dual-layer polyimide process, in which electrochemical and dry processing have been integrated to fabricate an advanced multilevel interconnection structure. Issues related to the compatibility of individual process steps and the extension of the technology to more demanding packaging structures are also discussed. Wong et al. review the material and manufacturing requirements for implementation of a multilayer high-density wiring pattern involving electroplated copper. Planarized and nonplanarized options for the construction of thin-film structures are described, and the advantages of electrochemical processing over dry processing such as evaporation are discussed. Perfecto et al. review development efforts to fabricate high-performance nonplanar thin-film structures for several generations of high-end systems. The criteria for choosing electroplating or subtractive etching are discussed in terms of ground rules, cost-effectiveness, and manufacturing robustness. This paper presents reliability test procedures used to qualify MCM packages.

Wiring in multichip modules must be prevented from corroding and interdiffusing. To accomplish this, barrier layers are deposited on Cu wires. A major advantage of electroless barrier deposition is that it is a self-aligning process that selectively clads the copper conductors. The paper by O'Sullivan, Schrott, et al. evaluates electrolessly deposited materials, focusing on barrier and adhesion properties. The investigated barrier materials include pure Co and Ni and alloys such as Co(P), Ni(P), and NiCo(P). The authors also describe a newly developed method of measuring the thickness of thin Co(P) layers using low-energy-beam SEM/EDX.

At the next level of packaging, chip carriers are connected to printed-circuit boards (PCBs). Present-day multilayered boards are produced by the plated-through-hole (PTH) process involving electroplating, electroless plating, and etching. A fundamental understanding of through-hole electroplating [12] and fine-line etching processes with closely controlled feature tolerances [13] was critical for the development of advanced PCBs and their integration for high-performance chips.

The next four papers discuss efforts in the development of monitoring methods and novel electrochemical etching and plating processes applicable in device fabrication and microelectronic packaging. Horkans presents an electrochemical method to monitor additives which affect the kinetics and quality of electroplated Sn–Pb solders. A polarographic technique with a renewable Hg drop electrode is used for the quantitative analysis of addition agents in the solder plating solutions. Kohl describes photoelectrochemical etching of III–V semiconductors to fabricate structures in electronic and photonic devices, such as lenses integrated onto light-emitting diodes, gratings on laser structures, and through-wafer via connections in field-effect transistors. His paper also addresses the extension of photoelectrochemical etching to silicon. The paper by Von Gutfeld and Sheppard deals with maskless electrochemical microfabrication by laser-enhanced processing, focusing on localized heating effects. This paper reviews theoretical and experimental aspects of laser-enhanced plating and etching for a variety of materials. Though the laser processes handle materials in a serial manner, the extremely high rates of localized plating and etching make the approach an interesting alternative for some specialized applications such as circuit repairs. Datta reviews work at IBM on the development of novel electrochemical metal-removal processes for microfabrication and compares dry and wet metal-removal processes. This paper highlights the features that make electroetching a cost-effective, environmentally friendly processing technology for microfabrication.

## Magnetic recording devices

The application of through-mask electroplating in the fabrication of thin-film magnetic heads created a revolution in the storage industry [1, 11]. This technology dates back to the 1960s, when Romankiw and his co-workers fabricated fine copper lines for coupled film memory devices, a process which was subsequently extended to thin-film heads [1]. The first experimental version of a coupled magnetic memory by these authors required the development of plating tools, such as paddle cells [14], and Permalloy plating to produce a magnetic-flux closed structure around the copper wires. On the basis of this early work, IBM pioneered the use of thin-film inductive heads for disk-drive products in 1979. The development of newer magnetic materials and on-wafer processing of thin-film heads led to the availability in 1991 of the first disk drive using magnetoresistive (MR) heads. The industry's continued demand for increased storage density has increased the importance of the plating of magnetic materials [15, 16]. The paper by Andricacos and Robertson reviews electroplated magnetic materials that are used in storage technology. The addition of impurities to nickel–iron alloys in a controlled manner and the fabrication of laminated materials by electroplating have led to improved magnetic and related properties.

## Microelectromechanical systems

Microelectromechanical systems (MEMS) are miniaturized machines that include sensors and actuators [17–19]. Microfabrication of these components with silicon employs basic integrated circuit processes that incorporate special etching and bonding techniques to create three-dimensional structures with micrometer resolution. Anisotropic etching (bulk micromachining) of silicon removes material at different rates along different crystal planes to produce characteristic pyramidal pits and sloped sidewalls. In surface micromachining, freestanding mechanical devices are formed by successive deposition, photopatterning, and etching of thin films at a substrate surface [19]. The development of high-aspect-ratio processing, in which the vertical dimensions are larger than the lateral dimensions, has made it possible to move from planar to three-dimensional micromechanical structures with dimensions ranging from millimeters to submicrometers. High-aspect-ratio microelectromechanical systems (Hi-MEMS) with vertical walls are generally formed using X-ray lithography in conjunction with electroplating and IC manufacturing techniques [20]. The paper by O'Sullivan, Cooper, et al. reviews a recently concluded ARPA-supported alliance project to build a Hi-MEMS minimotor. Optical and X-ray lithography were employed in the fabrication of the minimotor, which consists of a stator and a rotor. Tall structures with vertical walls were formed with X-ray lithography, while optical lithography was used for less critical layers in the stator structure. This paper describes processing involved in the minimotor fabrication.

## Concluding remarks

Electrochemical technology, which entered the electronics industry as a manufacturing process for low-end printed-circuit boards, is now employed for advanced processing to fabricate complex components, such as MEMS, high-end packages and storage systems, and high-performance chip interconnections. This has required an understanding of electrochemical transport, current distribution, process monitoring and control, as well as the ability to develop environmentally friendly processes. The development of nanoprocessing for further MEMS miniaturization and fabrication of giant magnetoresistance materials by lamination of a sandwich of nanometer-thick electroplated layers are among the emerging applications of electrochemical microfabrication that may have an impact on the performance of future microelectronic devices [18, 21]. Continued research and development efforts at both the industrial and academic levels are essential for

electrochemical processing to meet the challenges of the next millennium.


## Acknowledgment

I would like to thank the authors for their enthusiastic response, and the many internal and external referees who were involved in the reviewing process.


## References


1. L. T. Romankiw, I. Croll, and M. Hatzakis, *IEEE Trans. Magn.* **6**, 729 (1970); L. T. Romankiw, U.S. Patent 3,853,715, December 10, 1974.
2. *IBM J. Res. Develop.* **41**, No. 1/2 (January/March 1997).
3. *IBM J. Res. Develop.* **37**, No. 2 (March 1993).
4. R. R. Tummala and E. J. Rymaszewski, Eds., *Microelectronics Packaging Handbook*, Van Nostrand Reinhold, New York, 1989.
5. *The Wall Street Journal*, September 22, 1997.
6. *IBM Research* magazine, No. 4, 16–21 (1997).
7. P. A. Totta and R. P. Sopher, *IBM J. Res. Develop.* **13**, No. 3, 226 (1969).
8. M. Datta, R. V. Shenoy, C. Jahnes, P. C. Andricacos, J. Horkans, J. O. Dukovic, L. T. Romankiw, J. Roeder, H. Deligianni, H. Nye, B. Agarwalla, H. M. Tong, and P. A. Totta, *J. Electrochem. Soc.* **142**, 3779 (1995).
9. J. H. Lau, *Flip Chip Technologies*, McGraw-Hill Book Co., Inc., New York, 1996.
10. M. L. Minges, Ed., *Electronic Materials Handbook, Vol. 1, Packaging*, ASM International, Materials Park, OH, 1989.
11. L. T. Romankiw, *Electrochim. Acta* **42**, 2985 (1997).
12. E. K. Yung, L. T. Romankiw, and R. C. Alkire, *J. Electrochem. Soc.* **136**, 206 (1989).
13. A. H. Sweet, N. J. Nelson, and J. F. Battey, *Print. Circ. Fabr.* **10**, 20 (1987).
14. E. E. Castellini, J. V. Powers, and L. T. Romankiw, U.S. Patent 4,102,756, July 25, 1978.
15. P. C. Andricacos and L. T. Romankiw, in *Advances in Electrochemical Science and Engineering*, Vol. 3, H. Gerischer and C. W. Tobias, Eds., VCH Publishers, Inc., New York, 1994, p. 230.
16. T. Osaka, *Electrochim. Acta* **42**, 3015 (1997).
17. R. L. Smith, D. J. Fulmer, and S. D. Collins, in *Electrochemical Microfabrication*, M. Datta, K. Sheppard, and D. Snyder, Eds., PV 92-3, The Electrochemical Society, Pennington, NJ, 1992, p. 203.
18. N. F. de Rooij, in *Micromachining and Microfabrication Process Technology III*, S.-C. Chang and S. W. Pang, Eds., Society of Photo-Optical Instrumentation Engineers, Bellingham, WA, 1997, pp. 2–9.
19. P. J. McWhorter, A. B. Frazier, and P. Rai-Choudhury, in *Handbook of Microlithography, Micromachining and Microfabrication*, Vol. 2, P. Rai-Choudhury, Ed., Society of Photo-Optical Instrumentation Engineers, Bellingham, WA, 1997, pp. 3–40.
20. W. Bacher, K. Bade, K. Leyendecker, W. Menz, W. Stark, and A. Thommes, in *Electrochemical Technology*, N. Masuko, T. Osaka, and Y. Ito, Eds., Kodansha Ltd., Tokyo, 1996, p. 159.
21. E. Chassaing, P. Nallet, M. Walls, and M. J. Hytch, in *Magnetic Materials, Processes and Devices IV*, L. T. Romankiw and D. Herman, Eds., PV 95-18, The Electrochemical Society, Pennington, NJ, 1996, p. 125.



*Received June 10, 1998; accepted for publication June 25, 1998*



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