

Active line repair for thin-film-transistor liquid crystal displays

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A new method for repairing line defects during panel fabrication is described for high-resolution thin-film-transistor liquid crystal displays (TFT/LCDs). This approach uses electronic means in conjunction with physical rewiring to supply the appropriate data signal to the undriven segment of an open data line. Active line repair is simple and inexpensive, with the capacity for repairing numerous line defects. We have successfully implemented this repair approach on 10.4-in.-diagonal, 157-dpi prototype TFT/LCDs. This method is particularly suited for lower-volume, large-area, high-resolution TFT/LCDs, which are difficult to produce with high yield.

Introduction

Manufacturing yields of thin-film-transistor liquid crystal displays (TFT/LCDs) have increased steadily over the past several years. Manufacturing capacity has also increased, approximately doubling over the past two years, and many companies are planning fourth-generation plants which will use glass substrates approaching one meter on a side. At the same time, there are efforts to expand the LCD market to include desktop and other high-performance

applications. Very large-area or high-resolution displays are difficult to produce with high yield and acceptable cost, particularly during the startup phase, when production quantities are small. It is critical to any successful business plan to be able to recoup startup costs, especially at a time when the demand for and price of a new product are high, before the arrival of competitive products in volume.

If we consider the manufacturing process to consist of array process, cell assembly, and module assembly, the yield of the array process is comparable to the yield of the other portions of the process. For low-resolution VGA or SVGA panels, the usual yield inhibitor for the array is pixel defects, but it is common to have several percent of the array plates rejected because of line defects. For development laboratories or manufacturing lines working in the startup phase of high-resolution arrays, array-line defects are a major problem. In this paper, we describe a cost-effective method of line repair which can be implemented during the panel process, either before or after the attachment of driver chips. This approach can be used to salvage panels which have gone through most of the manufacturing process. Alternatively, this repair strategy can be used to remove or relax constraints placed on current array-process steps, thereby lowering manufacturing cost.

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Repair concept

In-process testing and optical inspection of array plates are essential to efficiently identify defective panels and to understand and improve process steps [1]. After completion of the active-matrix TFTs, an array test can be performed which sensitively and accurately measures a variety of electrical characteristics, including the precise location of line defects [2, 3]. Other types of tests, including electro-optic and conventional open and short testing, can also be used at various stages in the process to determine line defects [1].

A number of possible types of line defects can occur in TFT/LCDs, and these are discussed below. Some types of shorting defects can be repaired by laser cutting of the conducting material [4]. Unfortunately, even careful cutting within an array can result in one or more pixel (point) defects. For low-resolution displays, pixel defects are unacceptable. However, for high-resolution displays, individual pixel defects are less noticeable, and this may be an acceptable tradeoff in the correction of shorting defects. Repair of line opens within the array is much more difficult. In principle, this could be done by a combination of selective laser ablation of the topmost passivation layer and laser-induced chemical vapor deposition of a metal layer to bridge the gap at the open defect [5]. This process has been applied with some success in the repair of integrated-circuit packaging, where the feature size is fairly large [6]. However, past attempts in our laboratory to apply this process to high-resolution flat-panel displays have been only moderately successful. As practiced, the technology required precise control of the metal deposition, utilizing an organometallic precursor gas, in a vacuum chamber. The deposition of very narrow lines, less than 10 μm in width, was found to be difficult to control. It is likely that the vacuum environment, combined with variations in the local structure on the glass near defects, contributed to the difficulty of controlling the local heating that determines the deposition characteristics. Recent developments in laser technology and controlled nitrogen environments may greatly improve this technology. One very important limitation to this overall repair approach is that it cannot be implemented after the top color-filter plate has been attached to the array glass plate.

The repair of line opens is best done with an aggressive approach, such as that described by Castleberry and Possin [7], involving wiring changes at the periphery of the array that depend upon the detailed driver arrangement. Most smaller, low-resolution arrays used in notebook computers use *single-sided* drive for both data (signal) lines and gate (select) lines. The data lines are arranged in vertical columns and the gate lines are arranged in horizontal rows. One end of each line (the driven side) is connected to a driver chip output. Usually the driver chips

are attached to KAPTON** tape by tape-automated bonding (TAB), and the driver-chip outputs are metal traces on the KAPTON tape. Connection is made from data-line metal pads formed lithographically on the glass, through an anisotropic conductive film (ACF), to the driver-chip outputs. The driver-chip inputs are soldered to a printed-circuit board. The opposite end of each line in the array (the undriven side) is unconnected. In the case of a line-open defect, we call the portion of the line between the open and the undriven end of the line the *broken segment*, and the functioning segment, which is connected to the driver-chip output, the *driven segment*. In high-resolution arrays, the column driver chips are often arranged so that one set of drivers is attached to the glass at the top of the array and another set is attached at the bottom, and alternate lines are driven from opposite ends. For example, odd-numbered lines could be driven from the top and even-numbered lines from the bottom, or groups of lines could be driven alternatively from the top or bottom. We call this arrangement a *dual-bank* drive scheme. Dual-bank drive is necessary for fine-pitch arrays because of fan-out space limitations on the glass, driver bonding pitch limitations on the TAB, driver-chip size, and also by limitations on the maximum allowable clock frequency. The clock frequency is reduced by splitting the data input to the panel into several parallel signal paths. It is also common for high-end applications to drive gate lines from both ends (*double-sided* drive). This reduces the gate-line delay by more than a factor of 4 over single-sided drive and provides built-in redundancy. For an open line, double-sided drive becomes two single-sided drives, allowing nearly perfect drive for an open data line and adequate drive for an open gate line.

To repair an open data line, the data signal must be rerouted to the broken segment via a connection to the undriven side. Once this is done, we refer to this segment as the *repaired segment*. One way to do this is to make a jumper connection to the appropriate driver-output pin, which is connected to the open line, and route the repair signal to the undriven side by means of a metal jumper ring created by photolithography on the periphery of the glass substrate, or by means of a copper trace in the printed-circuit-board "picture frame" for the display, or with an insulated wire. We call this a *yellow-wire* approach to repair of line opens, and it has numerous disadvantages. First, the packaging requirements are extreme. Jumper connections must be made both to the driver output and to the undriven end of the open line. If the repair-signal line is on glass, some way must be found to route the line from the selected driver output, in the midst of the other outputs, around the periphery of the array, through the line connections on the other side to connect to the broken segment. The peripheral glass "real estate" is at a premium for most flat-panel displays

in order to keep the bezel area of the plastic frame to a minimum. The fan-out and TAB pitch also leave no room to introduce additional signal lines. If the repair-signal line were to be placed on the printed-circuit board, the additional on-and-off glass interconnections would require custom TAB packages at a minimum. A second disadvantage of a yellow-wire repair is that it is difficult to achieve acceptable electrical loading requirements. Typical data-driver specifications allow a maximum load capacitance not much larger than that of the array. This prohibits running a repair-signal bus line through the fan-out regions, because the crossovers with data and gate lines would increase the load capacitance by nearly a factor of 3, with an accompanying increase in line resistance. A third major disadvantage of yellow-wire repair is extremely limited capacity. The busing and connection requirements for running extra signal lines around the array make it difficult to accommodate more than a few repairs for the entire array.

Many of the problems of yellow-wire approaches to data-line repair arise from the need to run a signal line directly from one side of the array to the other. These problems can be greatly alleviated by providing an *electronic* means to supply the appropriate data signal to the broken segment of the line, as shown in **Figure 1**. We call this approach *active line repair (ALR)*. If the data for the defective line can be stored in a buffer, retrieved at a later time, and supplied to the broken side of the array, nearly all loading, layout, and interconnect problems are avoided. In this way, the repair-signal path between the top and bottom of the array is placed largely in a digital portion of the drive electronics. Only one connection is required on the glass to complete the circuit, and the arrangement is ideal for dual-bank drive.

It is possible to implement the same ALR approach for lower-resolution, smaller-area, single-sided drive panels for notebook displays. For these panels, the bezel area is especially critical, and is forced to an absolute minimum. A typical panel layout is shown in **Figure 2**, where data-driver chips are located at the top of the panel and gate-driver chips on the left. To implement ALR, several extra outputs on the last driver are routed around the periphery of the panel. On the right side, the metal bus lines can be placed under the black-matrix or glue-seal region of the top plate, and there are no crossovers with any gate lines. On the bottom of the panel, the repair-bus lines must extend below the edge of the array, with suitable connection pads. Depending upon the total number of repair-bus lines required, the width of the extended area below the array can be less than a few tenths of a millimeter. Since there are no crossovers, the load capacitance of the repair line is dominated by the capacitance between the line and the top plate, which can probably be made acceptably small. For small panels, the

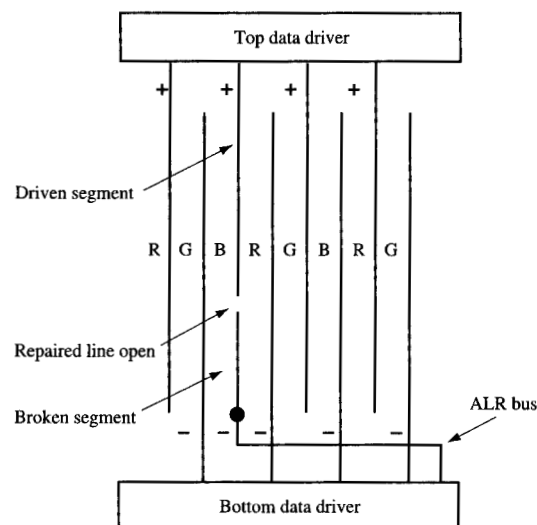


Figure 1

Dual-bank data-driver arrangement for a portion of the panel which has an open data line. A repair connection is shown between the broken segment and a bus line which runs from an extra driver output.

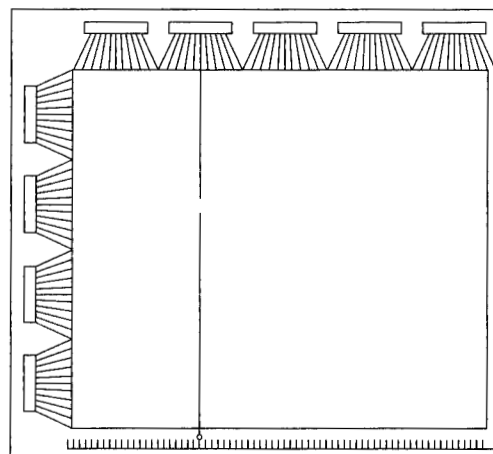


Figure 2

Overview of an ALR implementation for single-sided drive panels. For clarity, only one open data line is shown. Shown at the bottom is a single repair bus line, which runs along the panel periphery and is connected to an extra output on the last column-driver chip at the top of the panel.

resistance of the repair line should not be a limitation, but if space constraints allow, the repair lines may be made

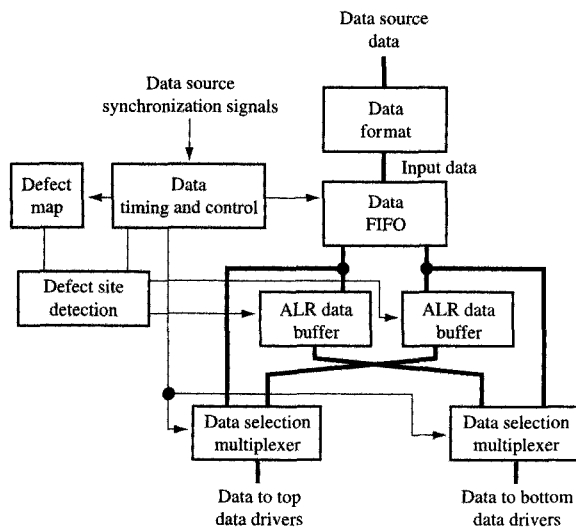


Figure 3

Block diagram of an ALR circuit.

slightly wider to offset the effects of increased average line length on resistance. For a limited number of repairs on a single-sided drive panel, an ALR approach such as this still maintains advantages over a simple jumper-connection approach. ALR avoids the layout constraints of a direct-connection bus within each driver-chip region and the associated crossover capacitance.

Thus far we have considered the repair of defective open lines; we now discuss the repair of line shorts. Shorts can occur between lines of the same type (data or gate), between a data line and a gate line (crossover short), or between a line (usually a data line) and the top plate. Another, unusual, type of short defect is a short between a line and the shorting ring, often as a result of a defective electrostatic-discharge protection device. Finding the location of a shorting line defect, in contrast to an open, can often be difficult. Various electrical tests typically reveal only the rough location of the defect, and it is usually necessary to optically inspect a large region of the defective line to determine the exact location of the short. Once this is done, line-to-line shorting defects can usually be removed with careful laser cutting. Crossover and top-plate shorts usually cannot be fixed with a laser. The strategy to repair crossover and top-plate shorts is to cut nearby regions in order to convert the shorting defect into an open defect. The detailed approach depends upon the nature of the drive circuit. For example, if the gate lines are driven double-sided and there is adequate margin for gate delay, the simplest approach is to convert a

crossover short into an open gate line by cutting the gate line to the left and right of the offending short. In this case, the repair is now complete, because the gate line is still adequately driven in a single-sided fashion from both sides. Alternatively, for either a crossover short or a short between a data line and the top plate, the data line could be cut above and below the short. The resulting data-line open could then be repaired with ALR. It is a challenge, however, to avoid forming one or more pixel defects during the cutting process. Array unit cells which are designed specifically for repair of crossover shorts may be necessary. This combination of laser cutting and ALR may be important, because crossover-short defects remain an ongoing problem even for mature array processes. For some processes and conditions, crossover shorts occur more frequently than line opens.

Fortunately, the dual-bank driver arrangement in many high-resolution display designs allows easy implementation of active line repair, since data signals are supplied to both the top and bottom of the array. It is relatively easy to incorporate driver chips which have extra, unused outputs available to provide ALR signals to the broken segments of defective lines. An ALR controller circuit is required, along with a suitable ALR bus arrangement on the glass. Finally, an on-glass connection technology is needed. These components are discussed in the following sections.

Active line repair circuit

A separate ALR circuit is required to intercept and process data for defective lines differently from the rest of the data. Its primary function is to count incoming pixel data and compare this count with a control reference to determine the locations of defective columns on the specific display. When a defect data site is detected, the ALR circuit saves the data in a buffer for later use. **Figure 3** shows a simplified block circuit diagram for ALR. The details of how and when the ALR data are used, as well as details for several blocks in Figure 3, are dependent upon the display design. Some assumptions can be made, however, about the handling of the source data in the ALR circuit, and also the operation of the devices that will accept the data from the ALR circuit.

The data source is assumed to be organized in a raster-scan arrangement in which the data are provided continuously during the active horizontal scan time. At the end of each horizontal-line scan time, before the next line begins, there is a period of time when no data are provided. Since the ALR circuit works identically on each horizontal line, there is no concern with vertical synchronization. A signal is generally provided by the data source that can be used as a flag by the ALR circuit to identify when a new horizontal line is beginning.

The output of the ALR circuit goes to the data drivers, which are attached to the display panel itself. The data

drivers convert a serial digital data stream into a parallel analog data stream. Here we are concerned with serial-to-parallel conversion, not digital-to-analog conversion. After the data for an entire row on the display are loaded into the drivers, the data are then latched to the columns. The data drivers can be considered to be a serial shift register followed by a parallel latch. The direction of shift can usually be controlled by an input on the driver chip. Typically, one pixel (three subpixels) is loaded into the shift register each clock cycle.

We now describe the operation of the ALR circuit for the case in which columns on the panel are alternatively driven from the top and the bottom, with the leftmost column 0 driven from the top. Each data-driver chip is assumed to have extra ALR outputs.

The data path through the ALR circuit is shown in bold in Figure 3. The first block encountered by the data is called *data format*. This block takes care of splitting the source data appropriately for the top- and bottom-panel data paths, which is an implementation-specific task. For this case, if the first-pixel data comprise (R0, G0, B0) and the second-pixel data comprise (R1, G1, B1), the data format block splits the data into (R0, B0, G1) for the top path and (G0, R1, B1) for the bottom path. This pattern repeats every two pixels, so that minimal circuitry is required for this block. It can be more complicated, depending upon the way in which the data drivers are interleaved from top to bottom.

The next block is *data FIFO*. Since each data driver has an ALR section of outputs, the normal flow of data must be interrupted in every data driver to load the ALR data. However, the data-source rate must be maintained at its normal data rate. The FIFO (first-in first-out) circuit serves to buffer the input data while the ALR data are loaded into the drivers. In our example, the depth of the FIFO is minimally equal to the number of ALR pixels supported in the entire data path. However, it can be made deeper if asynchronous operation is desired. For example, it may be desirable to minimize the clock rate to the display, independent of the data-source clock rate, since TFT/LCDs do not require horizontal retrace (flyback) time as do CRTs. The FIFO can be adjusted to accommodate this type of operation.

The normal data path from the FIFO runs directly to the *data selection multiplexer* via the connections shown in bold. The multiplexer is set to select the normal data, which pass on to the display data drivers.

The *data timing and control* block in Figure 3 controls the ALR circuit, including the FIFOs. It watches the input data source and directs the loading of data into the FIFOs. It also counts the pixel data coming out of the FIFOs and passes this count to the *defect site detection* circuit. The defect site detection circuit uses this count to

compare to a number received from the *defect map* block. This number from the defect map represents the pixel count of the next defective column on the display. The defect map also contains information about the ALR data driver to which specific data should be routed. The defective line locations could be stored automatically in the PROM from array test data on the panel prior to driver chip attachment, or the PROM could be set following a front-of-screen test. The size of the PROM can be quite small, about 2 Kb for an SXGA display. When a defect site is detected in the defect-site-detection circuit, both the data to be saved and the location at which the data should be saved are sent to the *ALR data buffer* block.

Assume a data driver with N normal outputs and E extra outputs used for ALR, where the driver-chip circuitry is exactly the same for the N and E outputs. After every N data shifts into the data driver, the normal data stream must be interrupted, and E ALR data shifts are performed. At this time, the multiplexer is switched to the ALR data buffer block, and the previously saved data are loaded into the ALR section of the data driver. After E shifts, the multiplexer is switched back to the normal data stream from the FIFOs, and the process continues. Note that the data paths out of the ALR data buffer blocks are crossed. This is the process of taking data that are normally used on one side of the display and routing them as ALR data to the other side of the display. This is the basic operation of the ALR circuit, where extra driver outputs on the opposite side of the display are used to drive the broken data-line segments which are not normally driven.

The details of how the ALR function is implemented on the display panel determine how complex the circuitry becomes. For example, it is possible to distribute the ALR section within the data driver, instead of clumping all ALR outputs at the end. To handle this, it would be desirable to embed some general information into the defect map that is loaded for a given display. For example, the N and E counts could be made programmable and entered as part of the defect map, making the circuitry more general. For development purposes, the entire ALR circuit function can be implemented with a single field-programmable gate array (FPGA).

Bus arrangement and disk-bond repair connections

The bus design employed for active line repair of SXGA prototype displays described in this issue is shown in **Figure 4**. In this display, the data lines are driven in a dual-bank fashion, with even-numbered lines driven from the top and odd-numbered lines driven from the bottom. The gate lines have double-sided drive. Each data driver has 192 outputs, with six extra outputs available for repair.

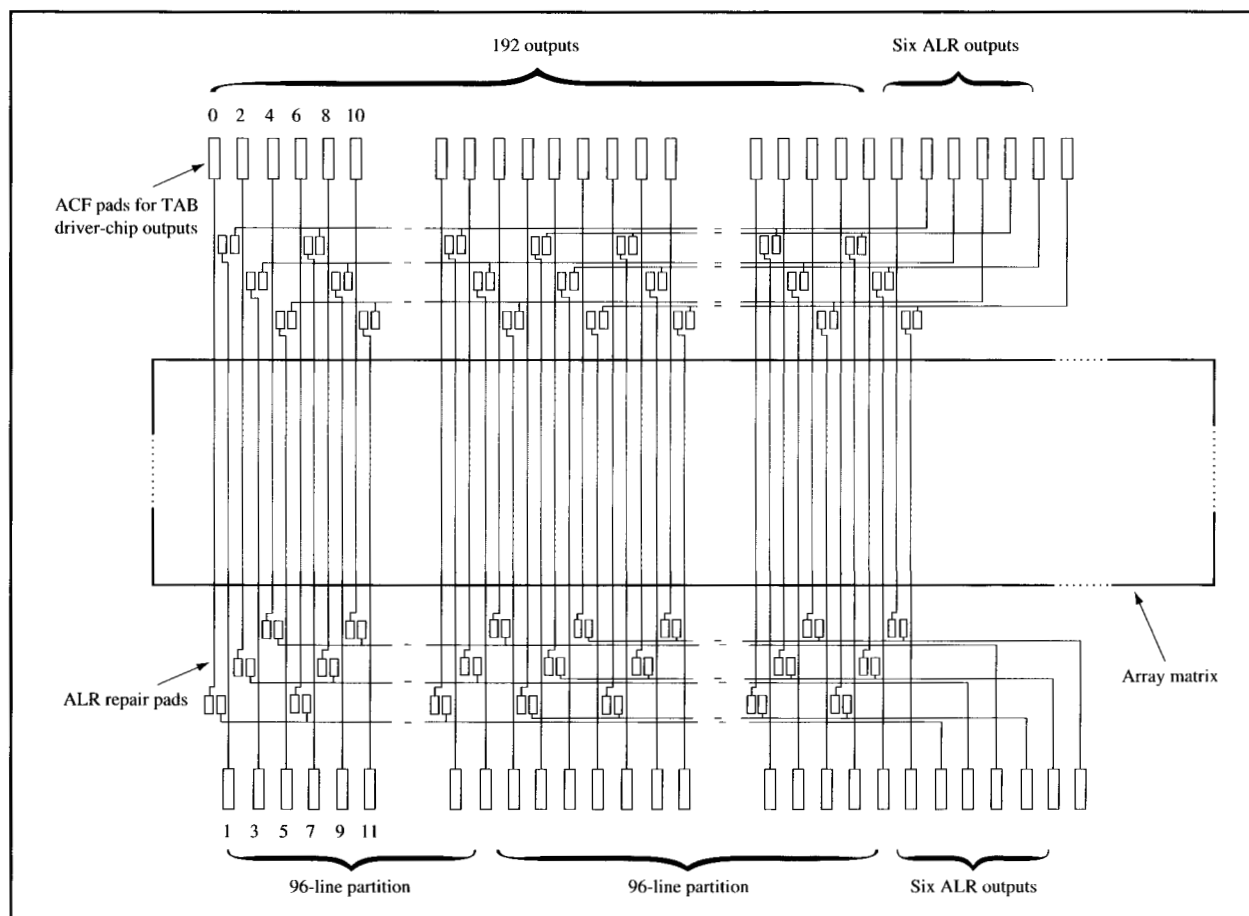


Figure 4

Active line repair bus layout for the prototype SXGA display. An exploded view of 384 lines driven by a top and bottom driver pair is shown. Each driver has 192 normal outputs, with six extra ALR outputs. A driver group has two 96-line partitions, each of which is serviced by three ALR bus lines. The TAB driver-chip outputs are connected to the pads on the glass with ACF.

Each pair of data drivers (top and bottom) addresses a total of 384 lines in the array. To reduce the wiring complexity, the outputs for each driver were divided into two driver partitions. Three bus lines are provided for each driver partition of 96 lines. The design requires two separate metal levels, but with a relatively small number of crossovers. In this way, capacitive loading and crosstalk are kept to a minimum, and the yield loss due to crossover shorts is also kept small. In our experience thus far, the repair bus itself was defective in only one case, preventing the array from being repaired. Provisions also have to be made for interconnections between metal levels, using either a direct via or a strap connection with indium-tin oxide (ITO). The repair-pad configuration is particularly simple, requiring only a single bond per repair.

For an SXGA array with 3840 data lines, this bus design allows a theoretical maximum of 120 lines to be repaired

in the display. However, it is highly unlikely that the detailed location and distribution of a large number of defective lines will allow accommodation by the repair bus. It is more appropriate to discuss the degree to which a more local distribution of line defects can be accommodated. Although each driver partition allows a theoretical maximum of three out of 96 lines (3.1%), the bus arrangement will not allow repair of any two lines within a partition which differ by a multiple of 3. For the RGB arrangement in this display, this means that no two lines of the same color within the same half of the same driver can be repaired. However, if we consider the dual-bank driver arrangement, this bus design allows a cluster of up to six consecutive line opens to be repaired. The implications of these constraints as well as those of the drive circuit are discussed in the following section.

A range of technologies were considered for the on-glass connections required for repair, such as wire bonding, laser welding, and anisotropic conductive film. Of these, laser welding is the most elegant, but the present technology is not particularly mature. The quality of laser welding is highly dependent upon welding conditions, connection-pad layout design, layer structure, and materials. With enough development, this may be the preferred approach. Although anisotropic conductive film allows very fine-pitch tabbing (down to $50\text{ }\mu\text{m}$), it is difficult to develop a small-area connection technology. TAB pad areas are typically in the range of $10^5\text{ }\mu\text{m}^2$ and larger, but required ALR connection areas are closer to $10^4\text{ }\mu\text{m}^2$ or less. Wire bonding is a very well established and automated technology, routinely used in integrated-circuit packaging. Basic types include ball and wedge bonding using either ultrasonic energy or thermal compression. Conventional wire-bonding technology is not appropriate for active line repair, because the wire loops left after bonding present additional packaging and reliability problems. Conventional wire bonding was developed to make connections between points separated by relatively large distances. With a suitable ALR bus design, there is no need for a long-distance jumper connection to be made. The distance between connection points can be made quite short, of the order of $10\text{ }\mu\text{m}$, which is safe with regard to both photolithographic and crosstalk considerations. A reliable low-profile, short-distance connection technology is required.

A proprietary bond technique was developed which uses ultrasonic energy at room temperature, applied to a small aluminum metal disk about $125\text{ }\mu\text{m}$ in diameter. A schematic drawing of a disk-bond and repair-pad pair is shown in **Figure 5**. One of the pads is a *line-extension* pad, which is connected to the undriven side of a data line. The other pad in the pair is a *repair* pad, which is connected to one of the bus lines running to the extra outputs from the driver chip. The bonding-process window and contact reliability were studied, and it was found that good bonds could be formed over a moderately wide range of bond conditions, provided that the bonding surfaces were clean. The bonding process also worked well for a variety of repair-pad layer structures, where the top layer of metallization was either molybdenum or aluminum and the underlying structure consisted of several layers. At low ultrasonic energies, unacceptably low bond adhesion was obtained, and at high energy there was unacceptable smearing of the disk bond. Typical pad-to-pad resistances were a few tenths of an ohm, and they remained low after temperature and humidity stressing. This bonding technology should have application not only for line repair of displays, but also for any packaging repair or engineering change which can be accomplished with a short-distance connection.

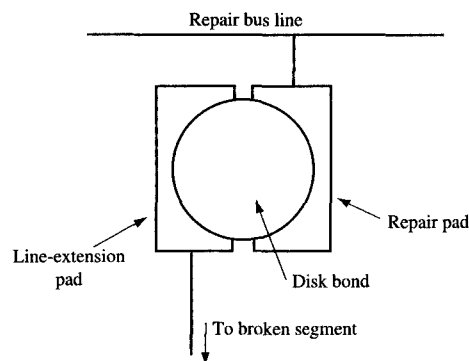


Figure 5

Drawing of a disk-bond and repair-pad pair. The line-extension pad is connected to the undriven side of a data line. The repair pad is connected to one of the bus lines running to the extra outputs on the driver chip. Each pad is typically $70 \times 150\text{ }\mu\text{m}$, with approximately $10\text{-}\mu\text{m}$ separation between pads.

Visual characteristics and crosstalk

The visual characteristics of a repaired line in display operation depend on the quality of the data voltage waveform supplied to the repaired segment, and on parasitic elements inherent in the array or repair connection circuit. Once the bond connection is made, and the ALR EPROM programming is completed, the correct data are supplied to the broken segment of the open line. Direct probing of repaired lines suggests that there is no signal degradation of the data waveform supplied to the broken segments: Timing, level, and noise are all the same as the waveforms applied to the normal lines. However, the data voltage polarities applied to the broken and normally driven segments of a defective line depend upon the polarity-inversion conditions used to drive the panel.

Some form of polarity inversion is necessary to avoid the presence of a dc voltage across the liquid crystal cell. Frame inversion consists of alternating the polarity of all data voltages every frame, which can be designated as positive and negative frames. Frame inversion is always present for LCDs. While this largely prevents the formation of dc pixel voltage, even optimal adjustment of the front-plate voltage may result in substantial flicker and unacceptable crosstalk. Additional inversion must be applied for acceptable performance. Row inversion (horizontal inversion) corresponds to alternating the polarity of data voltages as each row is addressed. Column inversion (vertical inversion) alternates the polarity of data voltages for every other column. Each of these inversion conditions suppresses vertical crosstalk, and if

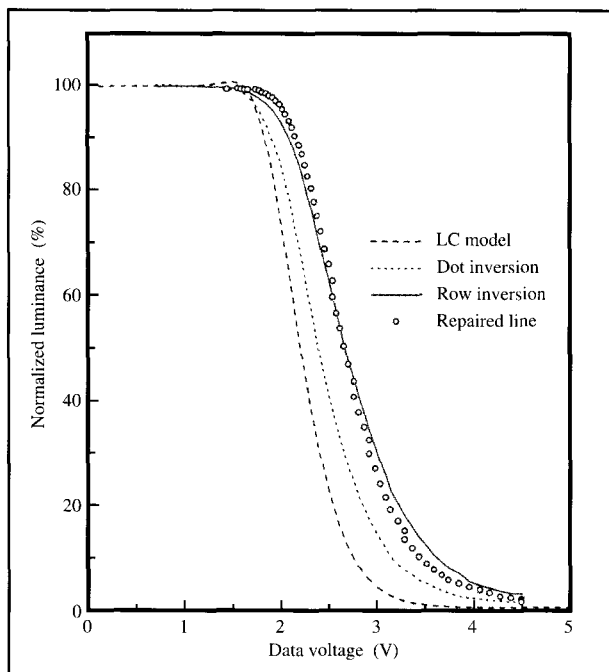


Figure 6

Transmission vs. voltage characteristics of a typical prototype display panel for different drive conditions. The characteristic for dot inversion is shown as a dotted line, the characteristic for row inversion as a solid line. The dashed line is a calculated curve for an ideal liquid crystal cell with the same cell gap as the prototype display. The points are for a repaired line segment, inferred from a separate front-of-screen measurement, which estimated the drive voltage difference required to match the luminance of the repaired line to the background, with the panel driven in dot inversion. The exact T-V characteristics of the repaired line fall exactly on the row-inversion curve, because no brightening effect is observed for the repaired line when the panel is driven in row inversion.

both conditions are applied together, the inversion condition is known as dot (or pixel) inversion.

When the prototype panel was driven with frame or row inversion, no visual artifacts were observed anywhere on or near the repaired lines. This was true not only at normal incidence, but also at viewing angles far away from normal, where contrast conditions become quite sensitive. However, when column or dot inversion is applied, there is a visual artifact which appears along the entire length of the repaired segment. The repaired segment appears slightly brighter than the surrounding (normal) lines, and this brightness is uniform everywhere on the segment.

It might be expected that a local visual defect could also occur at the location of the open. Under some conditions, the local electric fields could be high enough to affect the operation of the liquid crystal cells close to the open, perhaps resulting in some sort of circular defect. However,

no local visual defects were observed to occur at the locations of the opens under any drive condition.

In frame or row inversion, top and bottom data signals applied to the columns have the same polarity during the same frame time, so the polarity applied to the repaired segment is the same as that applied to the driven segment. In column or dot inversion, where top and bottom data drivers have opposite polarities, the polarity applied to the repaired segment is opposite to that applied to the normally driven segment, as shown in Figure 1.

The increased luminance of the repaired line segment is a consequence of an average pixel voltage on that segment which is smaller than that on the rest of the array, but the cause of the pixel voltage shift has to be understood. To rule out any possibility that the visual artifact is related to a problem with the ALR signal integrity, a "yellow-wire" experiment was done. An open line in the array of a prototype display panel was left unbonded, so that the broken segment remained isolated. A probe was placed on an ALR output of a drive chip on the same side of the panel as the normally driven side of the open line. A second probe was placed on the repair pad of the broken segment, and the two probes were electrically connected. In this way, the same polarity signal is provided to both ends of the open line under all inversion conditions. No visual artifacts were observed for the broken segment of the open line which was "repaired" in this fashion, under all inversion conditions. This experiment shows that the brightening effect is unrelated to the ALR circuit.

The shift in luminance of a repaired segment under column or dot inversion was first translated into an equivalent shift in data gray level by noting the difference in data gray levels required to match the brightness of the repaired segment with the background. This was done by using a number of different methods, involving only the subpixels of the same color as the defective line, or involving more than one subpixel field. One method involved reprogramming the EPROM so that the data supplied to the repaired segment of an open line were actually the data supplied to a nearby line. By this means, the gray level applied to the repaired segment could be changed within a small patch on the line, to accurately determine the matching gray-level condition. From a knowledge of the reference voltages supplied to the data driver and the 6-bit interpolation scheme, the difference in data gray levels required to match the repaired segment to the background can then be translated to differences in data voltage. Under these conditions, the differences in pixel voltage should be very nearly the same as the differences in data voltage.

Typical transmission versus voltage (T-V) characteristics of normal lines in a panel driven under different inversion conditions are shown in Figure 6. The luminance is measured with a photometer at normal incidence, near

the center of the display, with a uniform gray level applied to the panel. The photometer spot size includes approximately 25 full-RGB pixels, with no pixel or line defects contained within the spot. These curves have been normalized for 100% transmission at an applied voltage of 1 V. Typical luminance for a panel driven to a fully bright state is about 120 cd/m², with contrast ratios between fully bright and fully dark between 100 and 300. No normalization or offset of the transmission is done here for the dark state.

Included in Figure 6 is the T-V curve calculated from a liquid crystal cell model [8] for the same cell gap as that for the panel. We have obtained good agreement between predicted T-V curves from this model and actual test cells. The test cells use blanket films of ITO deposited on glass to define large-area electrodes, with no TFTs, with an applied ac voltage. Here we use the theoretical cell model curve, because for the same cell-fill process it is difficult to obtain the same cell gap for both a blanket test cell and the processed array. In Figure 6, different T-V characteristics are obtained for dot- and row-inversion conditions. The curves are shifted laterally from one another and also have different slopes. The T-V curve under dot inversion falls closest to the ideal, theoretical curve. These differences are due to the different drive-condition polarities and not to distortions of data or gate signals.

The RMS voltage which appears on the pixel flag determines the transmission through the liquid crystal. Although the pixel voltage is largely determined by the data voltage present while the addressed TFT is turned on, it also depends on several other factors. These include liquid crystal leakage, TFT charge-up characteristics, and parasitic capacitance. For our prototype display, the most important factor is crosstalk due to parasitic capacitances [9, 10]. Owing to the close proximity of array elements, capacitive coupling is present between the pixels and signal lines. Each pixel is coupled to its data line and also to the adjacent data line. Factors which influence this coupling include ITO pixel-to-data-line spacing, distance to the ITO top plate, layer thicknesses, and dielectric constants.

The differences between these curves can be analyzed to estimate the capacitive crosstalk between a pixel and the data lines to the left and right of the pixel. The points on the curves which have equal transmission values correspond to drive conditions which result in the same RMS pixel voltage. The pixel voltage is affected by capacitive feedthrough from the address-gate voltage pulse as well as from the data voltages on the adjacent left and right lines. The row-inversion curve is shifted to higher applied voltages than the dot-inversion curve. This is because, in dot inversion, the alternation of data-voltage polarity between the left and right data lines effectively

cancels the capacitive coupling from these two lines to the pixel, assuming the two values of parasitic coupling capacitance are the same. The dot-inversion T-V curve is also shifted to higher data voltage than the test cell. This is due both to the coupling from the gate pulse and to other drive-circuit waveform features which are not present in the test-cell case. The coupling capacitance values can be estimated by calculating the percentage of voltage shift between row and column inversion. In Figure 6, the row-inversion curve is shifted to the right of the column-inversion curve by about 12% of the applied data voltage, corresponding to an average coupling for this particular panel of about 6% to the left and right of each pixel. The values of coupling capacitance obtained from this analysis are in rough agreement with that expected from the pixel-cell geometry and array process for this panel. This estimate of crosstalk also agrees with separate front-of-screen measurements of crosstalk on test patterns.

Also shown in Figure 6 is a typical T-V curve for a repaired segment as inferred from matching experiments, with the same panel driven under dot inversion. The transmission values in this curve are those of the background pixels under dot inversion, but the data-voltage values are those required to match gray level for the repaired line segment. For typical prototype displays driven in dot inversion, the brightness increase of repaired line segments corresponded to pixel voltage shifts as large as about 200 mV for the mid-gray state. It is seen that the T-V curve for the repaired segment, as derived from the matching experiment, is close to that for normal lines driven in row inversion. This agreement is a consequence of the polarity of data voltages applied to the repaired segment and the presence of capacitive crosstalk in the array. As shown in Figure 1, the local inversion conditions applied to the repaired segment and its nearest neighbors are actually row inversion, regardless of whether the panel is driven in column or row inversion. Ideally, the inferred T-V curve for the repaired segment and the T-V curve for normal lines under row inversion should coincide exactly, because the brightening effect is not observed under row inversion. The discrepancy is believed to be an artifact of the measurement technique used, where one or more color subfields were varied, and where the crosstalk conditions are not exactly the same as for the rest of the array.

We also note two other characteristics which indicate that crosstalk causes the effect. The first is that, with column or dot inversion, the visual artifact is very weak if subpixels the same as those on the repaired line are driven dark and subpixels to the right are driven bright. In this case, the crosstalk on the line to the right is the same as for the rest of the panel, and the voltage feedthrough on the repaired line is minimized by minimizing the voltage on the line to the right. For all other combinations of energized subfields, the visual effect is seen. The second

is that the ALR visual artifact is reduced somewhat in panels which have a smaller cell gap. The smaller cell gap brings the ITO layer on the top plate closer to the array, increasing the pixel capacitance and ground-plane shielding. Both of these factors decrease capacitive crosstalk.

The visual artifact is easily removed once the effect is understood. The best approach uses data drivers which provide bipolar output [11]. In this way, the polarity of the ALR data provided to the broken segment can be arranged so that the local inversion conditions and crosstalk are the same as in the rest of the array.

Repair utility

A number of factors contribute to an understanding of the utility of this repair approach. An estimate of the repair effectiveness can be done by calculating the size of the repair "net," that is, the range of possible defect configurations which are suitable for repair. To do this, we must assume something about the probability distribution of line defects. If the line-defect density is extremely low, we may safely assume that the defects are independent of one another, such as those due to particulates, for example. A reticle defect, for example, would result in a very high array-defect density, and the defects would be correlated because of the repeated exposure pattern of the stepper. Another way in which the defect density becomes higher and correlated is when the size of the particle, defective area, or scratch becomes large compared to the line-to-line spacing. In this way, groups of adjacent line opens could occur in clusters. Generally, the vast majority of line defects are uncorrelated even when there are many defects. This analysis assumes that the line opens are completely independent, treating the formation of each line as an independent trial in which the occurrence of a line open does not depend on location on the glass, run, or lot number, etc. This allows us to break up the analysis on the glass in any way we choose—odd or even lines, driver-chip outputs, data path, or any other order. Events which are independent follow a binomial distribution. For a moderate number of trials with a low probability of occurrence for any single line open, this distribution is well approximated by the Poisson distribution,

$$P_n(k) = \frac{\lambda^k}{k!} \cdot e^{-\lambda},$$

where $P_n(k)$ is the probability of k occurrences in n trials, and λ is the most probable number of occurrences, given by $\lambda = n \cdot p$, where p is the probability of a single event.

The probability of any single line open is simply the total number of line opens divided by the total number of lines fabricated in a large number of displays. In manufacture, a typical display yield loss due to line defects

might be in the range of a few percent, where the total number of line opens in any single defective array hardly ever exceeds 1. For an 800×600 SVGA array with 2400 column signal lines (n), a 2% display yield loss [$P_{2400}(1)$] corresponds to a probability of any specific line being defective (p) of about 0.0008%. It is difficult to create prototype displays in a research environment that are totally free of line defects. For our high-resolution SXGA prototype panels, typical single-line-defect probabilities are in the range 0.02–0.5%, corresponding to about 1–20 line defects per panel.

We wish to estimate the probability that a defective panel will be suitable for repair. It is assumed that a panel will be suitable for repair if the distribution of line opens is compatible with the limitations of the ALR wiring and also the ALR circuit design. We assume that the additional yield loss in the repair process itself is negligible. Examples of this additional yield loss might be disk-bond failure, incorrect repair connections, or display damage due to handling. There are two areas which can be considered separately: the on-glass repair bus wiring connecting the extra driver outputs, and the ALR active circuit.

For the on-glass wiring, we first break up the display into odd and even lines and consider them independently of each other. In the actual display, each driver chip drives either even-numbered lines (from the top), or odd-numbered lines (from the bottom). However, with the assumptions discussed above, we can "re-map" the display, and imagine that all of the odd lines are lumped together (for example, on the left), and all of the even lines are lumped together (for example, on the right). For our prototype display, each driver addresses a group of 192 lines, further divided by the repair bus into two driver partitions of 96 lines, so that the display contains a total of 20 driver chips (10 driver pairs) and 40 driver partitions. Six extra outputs were used in each driver chip, so that three extra outputs are available to repair each partition. From the bus arrangement shown in Figure 4, there are two conditions which cause failure. First, if more than three line opens occur within a driver partition of 96 lines, the capacity of the extra ALR outputs is exceeded. Second, if two or more opens occur within a partition, and they differ by a multiple of 3, the capacity of the bus lines is exceeded. For a stripe RGB arrangement, bus capacity is exceeded if two or more lines of the same color are open within a partition.

Repair is suitable in any single partition if either no line opens occur, or one, two, or three occur. The probability of success (that is, that the line-defect configuration is suited for repair) is given by

$$P_{\text{bus}} = P_{96}(0) + P_{96}(1) + (2/3) \cdot P_{96}(2) + (2/9) \cdot P_{96}(3),$$

where the individual P terms are defined from the Poisson distribution function. The last two individual terms are modified to take into account the probability that the lines may differ by a multiple of 3, which would cause a conflict. Consider the $P_{96}(2)$ term, corresponding to two open lines within a partition. There are two chances in three that the second open line does not conflict with the first open line, so the prefactor for this term is $(2/3)$. For the case of three open lines, the probability that the second open line does not conflict with the first is $(2/3)$, and the probability that the third open line does not conflict with either the first or the second line is $(1/3)$. To avoid conflict, both of these conditions must be met, so the individual probabilities should be multiplied. The probability that there is no conflict with three open lines is $(2/9)$, which is the prefactor in the last term.

To successfully repair a display panel, *all* partitions must be suitable for repair. One way to estimate the probability of success for a panel is to treat all 40 driver partitions as independent trials. In this case, the exact binomial probability distribution can be used. The panel success probability becomes

$$P_{\text{display}}(\text{bus}) = P_{40}(0) = (P_{\text{bus}})^{40}.$$

We turn next to the ALR circuit limitations for our prototype display. The data path is split into four, so that at any instant in time, four driver chips are being loaded with data. The ALR control circuit RAM allows seven defect locations to be stored for appropriate loading into these data drivers. This loading process is repeated five times before all of the data can be latched into the array, so that a total of 35 lines can be accommodated by the ALR circuit. We define an array partition as the lines addressed by a single data path, corresponding to four drivers for a total of 768 lines. Again we treat all partitions as being independent. There are five partitions in the display, all which must be free of overload. The probability of success for the ALR circuit is given by

$$P_{\text{display}}(\text{circuit}) = (P_{\text{circuit}})^5 = \left[\sum_{j=0}^7 P_{768}(j) \right]^5.$$

The constraints of bus and circuit are independent, and they must both be satisfied. We multiply these two probabilities to get an overall estimate,

$$P_{\text{display}}(\text{overall}) = P_{\text{display}}(\text{circuit}) \cdot P_{\text{display}}(\text{bus}).$$

The results of these calculations are shown in **Figure 7**. The abscissa is the most probable number of opens for the display, $\lambda_{\text{display}} = n_{\text{display}} \cdot p$, the product of the total number of lines in the display (3840) and the probability of a single-line open. It is desirable to balance the limitations due to the bus and circuit portions of the repair design to achieve an optimum. For the partitions,

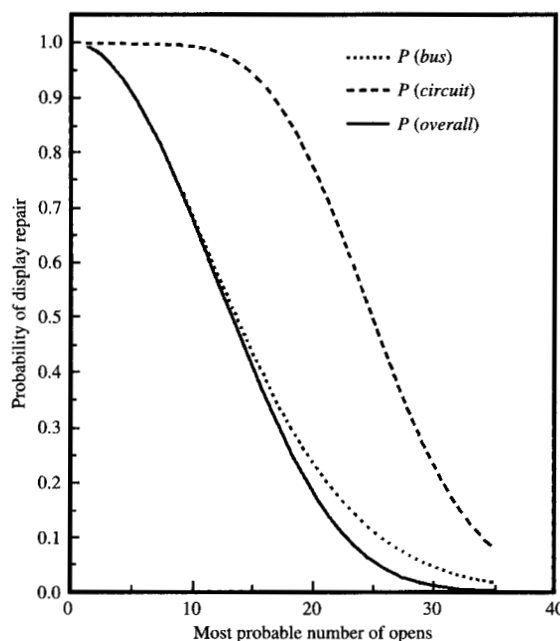


Figure 7

Success probability for repair of a display panel. A Poisson distribution is assumed for line opens. The overall probability is the product of probabilities for the on-glass wiring and the ALR circuit.

the success probability for the bus wiring is much higher than for the repair circuit. However, the bus partition size is 96 lines, much less than the ALR circuit partition, 768 lines. When the success probability for the display is calculated, as shown in Figure 7, it is seen that the bus wiring is clearly the limiting factor. The overall probability of repair success falls steadily from 100% for a single open to nearly zero for 35 opens. The probability of success is 90% for five line opens, 67% for ten line opens, and 18% for 20 line opens.

Improvements can be made to increase the capability of both the bus and drive circuit, with only a small increase in complexity. One possible improvement to the bus requires the occasional use of more than one disk bond per line repair, combined with laser cutting. Although this makes the repair process slightly more difficult, the probability of repair success can be greatly increased. One design has been built which increases the repair capability by more than a factor of 10 over the design described in this paper, with no significant increase in glass area devoted to the repair bus. While designs such as these are clearly excessive for typical manufacturing yields, for an immature array process it provides an appropriately large safety net.

The main consideration of this analysis has been for line opens. As discussed earlier, other line defects, such as crossover shorts or top-plate shorts, can be repaired with this technique. Assuming that all defects are uncorrelated, the analysis is the same as for opens alone, since all defects would be converted to opens in the course of the procedure. The abscissa in Figure 7 can then be viewed as being the most probable total number of line defects of any type.

These calculations can be directly applied in an analysis of cost versus benefit where array yield loss due to line defects may be quite large. The analysis should include the cost of the ALR circuit on every panel, the fixed capital equipment cost to implement ALR, the cost to implement ALR on a panel, and any additional yield loss due to plate handling, etc. during repair. The ALR circuit includes a PROM for the defect map, FIFOs, and controller circuits, which could all be included as part of a reduced-chip-set panel module. Altogether, the additional cost to implement ALR is estimated to be quite small, no more than about 1% of the panel manufacturing cost, with minor capital equipment outlay. The cost of ALR depends only slightly on the size of repair capability. Although the detailed cost-versus-benefit analysis can be complicated, one general relationship holds: If the percentage of panels lost to line defects exceeds the ratio of ALR cost to panel manufacturing cost, ALR will be cost-effective. This is especially important for those cases in which insufficient production-run volume can be allocated to gain the experience necessary to improve the yield. By increasing the yield, ALR has the potential to both reduce manufacturing cost per part and increase throughput.

Summary

We have developed a new approach to repair defective lines in TFT/LCDs. This inexpensive method is straightforward and can be highly automated. Nevertheless, it is natural for developers of manufacturing processes to explore all possible process yield inhibitors, and to exhaust all potential process improvements before resorting to a repair strategy, however modest. Attempts to provide built-in redundancy in the array have thus far focused on point-defect TFT failures. These approaches generally compromise display performance, and have been relatively unsuccessful. Line defects present a different and simpler kind of challenge, and active line repair offers a solution which is nearly equivalent to built-in redundancy. Given the rapid pace of new product introductions and the desire to penetrate the desktop CRT market, it is worthwhile to consider the potential advantages of active line repair for high-performance and high-resolution TFT/LCDs, which have high manufacturing cost. Much of the challenge of fabricating an array is to produce several kilometers of flawless wiring on a large

piece of glass. As a display technology, TFT/LCDs must move beyond the point where a single line open distinguishes the difference between manufacturing success and failure.

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