A 10.5-in.-diagonal SXGA active-matrix display

by E. G. Colgan
P. M. Alt
R. L. Wisnieff
P. M. Fryer
E. A. Galligan
W. S. Graham
P. F. Greier
R. R. Horton
H. Ifill
L. C. Jenkins
R. A. John
R. I. Kaufman
Y. Kuo
A. P. Lanzetta
K. F. Latzko
F. R. Libsch
S.-C. A. Lien
S. E. Millman
R. W. Nywening
R. J. Polastre
C. G. Powell
R. A. Rand
J. J. Ritsko
M. B. Rothwell
J. L. Staples
K. W. Warren
J. S. Wilson
S. L. Wright

A 157-dot-per-inch, 262K-color, 10.5-in.-diagonal, 1280 × 1024 (SXGA) display has been fabricated using a six-mask process with Cu or Al-alloy thin-film gates. The combination of high resolution and gray-scale accuracy has been shown to render color images and text with paperlike legibility. The low-resistivity gate metallization and trilayer-type TFTs with a channel length of 6–8 μm were fabricated with a six-mask process which is extendible to larger, higher-resolution displays. A combination of double-sided driving and active line repair was used so that open gate lines or data lines did not result in visible line defects. A flexible drive-electronics system was developed to address the display and characterize its performance under different drive conditions.

Introduction

To evaluate the ergonomic advantages of high-resolution active-matrix liquid crystal displays (AMLCDs), we have constructed a 157-dot-per-inch (dpi), 262K-color, 10.5-in.-diagonal, 1280 × 1024 (SXGA) display. The advantage of such a display is that it encompasses a combination of high information content, high spatial resolution, and high gray-scale accuracy, permitting it to render color imagery with high fidelity and provide text with paperlike legibility. (The term *paperlike* is of course used subjectively to indicate that the display approaches laser print quality; this term has been used by a number of first-time observers of the display.) Laser printers typically use resolutions of 300 to 600 dots per inch (dpi) with no gray scale. The tradeoff between gray scale and resolution has been explored experimentally [1], and 13-in. SXGA displays have been fabricated with self-aligned TFTs having a channel length of 6 μm. [2]. That work indicates that the use of gray scale can be traded off with spatial resolution. Color images in magazines are typically screened (the process of pixellating an image for printing) at a resolution of 150 dpi. The above results led us to believe that improved image and text quality could be achieved on an AMLCD with approximately 150 dpi and good gray-scale accuracy. Cathode-ray-tube-based displays provide a technology which is capable of 110-dpi color pixels with a full gray scale. For the first time, AMLCDs provide a means of obtaining higher resolution with full color on a direct-view flat-panel display. AMLCDs have been commercially produced with resolutions of 77 dpi to 106 dpi [3]. The process technology underlying AMLCD production permits even higher resolutions to be achieved.

0018-8646/98/$5.00 © 1998 IBM

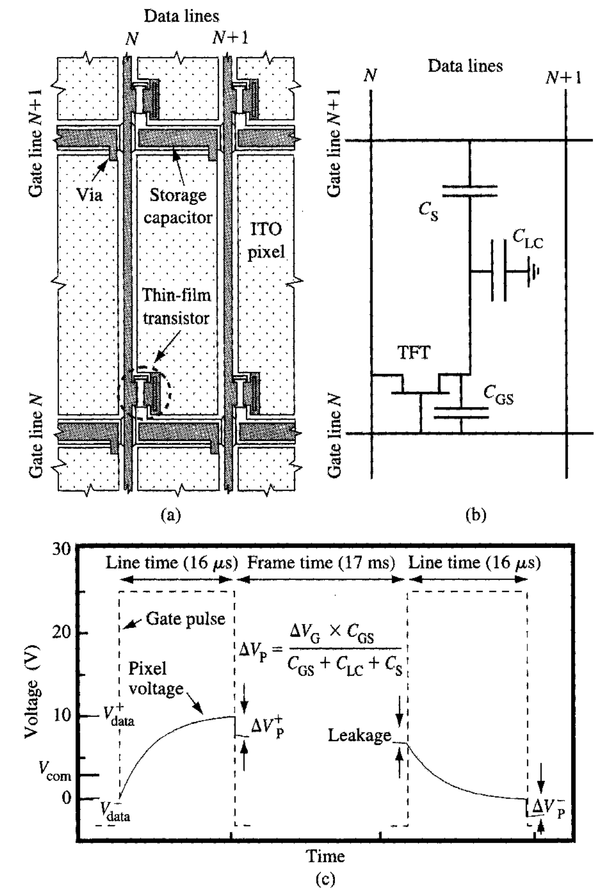


Figure 1

Schematic drawing of AMLCD (a) subpixel, (b) equivalent circuit, and (c) pixel voltage vs. time.

Key technical issues in fabricating the display described here included minimizing the gate delay, achieving adequate charging performance, obtaining an acceptable aperture ratio (the fraction of the subpixel area through which light can pass), and developing suitable processes for achieving an adequate thin-film-transistor (TFT) array yield. In the present work, we have used low-resistivity gate metallizations such as Cu and Al-alloy films. In previous work, we fabricated 146-dpi VGA Cu-gate AMLCD displays [4]. Key challenges in using Cu and Al-alloy films were the development of processes which were compatible with the chemical properties of Cu films and the prevention of hillock formation during the thermal processing of the Al-alloy films. The available charging time for such a high-resolution display and the charging accuracy for 6-bit gray-scale operation required the development of a TFT with a channel length of 8 μm or less. To obtain an adequate aperture ratio, a storage capacitor on the previous gate-line (C_S-on-gate) design was used. In this prototype design, we explored methods for repairing line open defects in both the gate lines and data buses. By driving the gate lines from both sides and using active line repair (ALR), described below, open gate or data lines did not result in visible line defects. A flexible drive-electronics system was developed to help characterize display performance, explore different inversion methods, and provide 6-bit gray-level accuracy at a refresh rate of 60 Hz.

Array design and fabrication

- *Available gate-line time*

A frame rate of 60 Hz with progressive scan was chosen as the starting point. This results in a gate-line time of approximately 16 μs during which the TFT has to charge the pixel with sufficient accuracy and then be turned off to hold the charge. Liquid crystal operation requires a near-zero average dc voltage for long-term, stable operation. This is achieved by alternately addressing a pixel with a positive and a negative voltage. For 6-bit gray-level drivers, the charging accuracy should be approximately 50 mV (1%). The pixels were precharged to meet the charging precision requirements within the available time. Precharging consists of activating or "turning on" a gate line prior to its normal excitation time. For example, pixels in line N might be precharged by turning on gate line N while addressing line $N - 1$ or $N - 2$. This momentarily charges the pixels on line N to values that are incorrect but of the correct polarity. Precharging thus reduces the charging that must take place during the line time. During the gate-line time, the gate voltage must also be brought well below the threshold voltage of the transistors in order to turn off the transistors and hold the charge on the liquid crystal and storage capacitor. **Figure 1** shows a schematic drawing of a subpixel (a), the equivalent circuit (b), and the pixel voltage as a function of time (c). The gate-line time is subdivided into a charging period (up to 12.3 μs), a period for gate voltage decay (>1.2 μs), and a period for the rail switching of the data drivers (>2.4 μs). The resistance and capacitance (RC) delay of the gate line retards the turnoff of the transistor at the far end of the gate line. This display is driven from both ends of the gate line, thus reducing the gate-line delay by a factor of 4.

- *Aperture ratio*

The required subpixel size for a 10.5-in.-diagonal vertical-stripe SXGA (1280 × 1024) display is 54 μm × 162 μm. This subpixel area is about 1/4 the area of a typical subpixel. For a conventional 12.1-in.-diagonal SVGA display, a subpixel with dimensions of approximately

103 μm × 309 μm is used. Obtaining good aperture ratio in this size required the use of a C_S-on-gate design which avoids the area lost to a separate storage capacitor line. The aperture ratio is primarily dependent on the width of the data line, the space between the indium–tin oxide (ITO) pixel electrode and the data line, and the overlap of the black matrix over the edge of the ITO pixel. Typical values for data-line width are 8 μm with a 4-μm space to the ITO pixel. As the pixel resolution is increased, the fraction of the pixel consumed by these spaces increases. The schematic in **Figure 2(a)** shows a cross-sectional view through the subpixel; **Figure 2(b)** shows the calculated aperture ratio values as a function of the black-matrix-to-ITO overlap, assuming that the effective gate width (including the TFT area) is 35 μm. A minimum spacing of about 4 μm is required between the ITO and the data line to avoid excessive capacitive crosstalk. The black matrix must overlap portions of the ITO pixel in order to mask regions of liquid crystal which were responding to fringe fields; a typical overlap is 4 μm. A 12.1-in.-diagonal SVGA display has an aperture ratio of approximately 65%. When the same design rules are applied to a 157-dpi SXGA display, the aperture ratio is 33%. An aperture ratio over 35% was achieved for the present display, and the optical transmission of the complete display module was 4%.

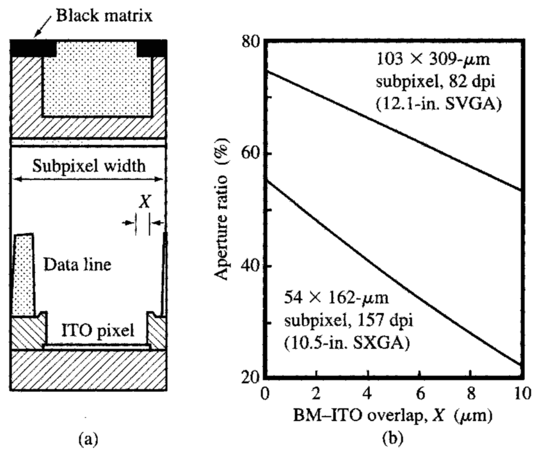


Figure 2

Schematic drawing of (a) subpixel cross section and (b) calculated aperture ratio as a function of the black-matrix–ITO overlap distance.

- *Gate-line delay*

The gate-line delay can be estimated by using the product of the total gate-line resistance and the total gate-line capacitance to ground. This results in a conservative estimate of the RC delay compared to the actual distributed RC delay. The total capacitance is the sum of the capacitance of the crossover capacitor, the capacitance of the transistor, and the series combination of capacitances of the liquid crystal and storage capacitor. The crossover capacitance is due to the overlap of the gate and data lines [Figure 1(a)]. The total capacitance is approximately 0.5 nF. The total resistance in the gate line is about 1500 Ω. (The Al-alloy gate lines were thicker to compensate for their higher resistivity compared to copper.) Driving a gate line from one end gives a lumped RC estimate of 0.75 μs; driving the gate line from both ends gives an estimate of 0.19 μs, both of which easily meet the specification discussed earlier. **Figure 3** shows the required gate resistivity versus the number of gate lines for a range of display diagonals for both the separate C_S line and C_S-on-gate cases [5]. This scaling analysis was based on a lumped RC delay, single-sided driving, and a gate thickness of 250 nm. The design point of the 10.5-in.-diagonal SXGA display is indicated by a solid circle and corresponds to a maximum resistivity of 7 $\mu\Omega$-cm for single-sided driving. For a MoW-alloy gate metallurgy (resistivity 15 $\mu\Omega$-cm versus about 5 $\mu\Omega$-cm for Al alloy

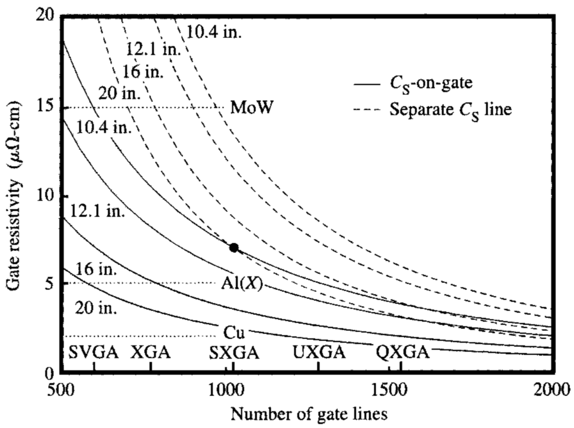


Figure 3

Required gate resistivity vs. number of gate lines for C_S-on-gate and separate C_S line designs for the indicated diagonals. Typical resistivities for MoW films, Al-alloy films, Al(X), and Cu films are indicated.

or about 2 $\mu\Omega$-cm for Cu), the thickness needed for acceptably low resistance is not practical. It therefore follows that an Al-alloy or Cu gate metallization is required for significantly larger displays with higher information content. Although the gate lines were driven from both sides, the array was designed to operate with single-sided driving so that an open gate-line defect would

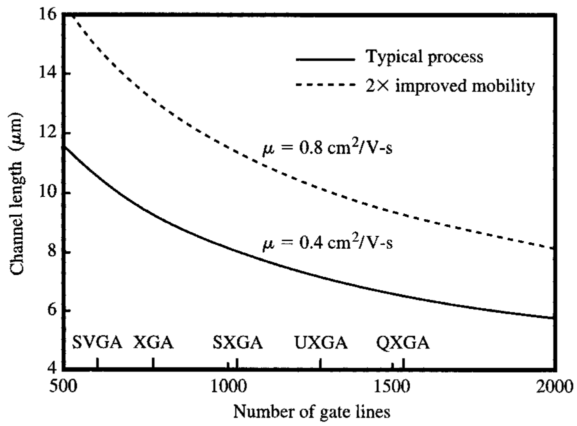


Figure 4

Required channel length vs. number of gate lines for a typical TFT process and an improved process.

not result in a visible line defect. This also permitted repair of "crossover" shorts between data and gate lines by laser-cutting a gate line on both sides of the short, and prevented the very rare gate-line defect from being visible. The single-sided operation was verified by the uniform image which resulted when driver chips were attached to only one end of the gate line. Note, however, that this repair technique has the disadvantage of requiring double-sided driving.

- *TFT channel length*

The transistor used to address an individual subpixel must be able to charge the subpixel to the required accuracy in the time allowed (<12.3 μs), limit the size of the pixel voltage drop (ΔV_P) when the transistor is shut off [Figure 1(c)], and prevent charge from leaking off during the frame time [Figure 1(c)]. The charging accuracy is determined by the time constant, τ_{chg}, the product of the resistance of the TFT and the sum of the liquid crystal capacitance [C_{LC}, between the ITO pixel and top plate, Figures 1(a) and 1(b)] and the storage capacitance [C_S, between the data line and the previous gate line, Figures 1(a) and 1(b)]. A simplified model of the transistor [6] approximates the charging behavior as that of a fixed RC circuit and requires that the RC delay be small enough to allow the charging period to have a duration of several τ_{chg}. The achievement of a 6-bit gray scale requires a charging accuracy of approximately 1% (allowing some error budget for the rest of the system), which corresponds to a charging time of 4.6 τ_{chg}. Therefore, with a charging time of 12.3 μs, an *RC* delay of 2.7 μs is needed. This approximation has been used to estimate the transistor channel length required as a function of the number of gate lines, shown in **Figure 4** for both a typical TFT process (mobility of 0.4 cm^2/V-s) and one with increased mobility (0.8 cm^2/V-s). For an SXGA display with a typical process, a TFT channel length of 8 μm or less is needed. TFT arrays for the SXGA display have typically been fabricated with channel lengths of 8 μm, and recently, arrays have been fabricated with channel lengths of 6 μm. The on-current of the transistor is proportional to the mobility and the width, and inversely proportional to the channel length. It is clear that a wider transistor provides a smaller charging τ_{chg}. However, this has to be balanced against an increase in the size of its capacitance [C_{GS} in Figure 1(c)], to the extent that too large a pixel voltage drop may occur at the trailing edge of the gate pulse. Experience has shown that a ΔV_P of approximately 1.5 V can be tolerated. This drop can be estimated as a capacitive voltage divider between the transistor capacitance and the storage and liquid crystal capacitance [Figures 1(b) and 1(c)]. Minimizing the capacitance of the transistor per unit width is highly desirable. The design assumed a TFT threshold voltage of less than 5 V and an off-current of less than 1 pA. The off-current of the transistor must be low enough to maintain gray-scale accuracy during the frame time and to avoid flicker. Transistor channel lengths smaller than 8 μm or transistors having increased mobility are needed for display formats with higher resolution than SXGA.

- *Six-mask Al-alloy thin-film-transistor process*

Thin-film-transistor arrays were fabricated using a six-mask process and either Cu or Al-alloy gate metallizations. The Cu gate process was previously described [5, 7]. The use of Cu required a number of design changes and novel processing steps to passivate the Cu films against oxidation, provide sufficient adhesion to the substrate, and prevent adverse reactions with other materials. The process integration is easier with an Al-alloy film, but the resistivity is higher, and the formation of hillocks during thermal processing must be avoided. Hillocks result from the thermal expansion mismatch between the substrate and the Al or Al-alloy film. Typical approaches to avoiding hillock formation are the addition of alloying elements [8–10] or forming capping layers such as Al_2O_3 [11] or MoTa alloy [12]. A combination of alloying and a partial Mo capping layer was used in this work. The six-mask Al-gate process flow is shown in **Figure 5**. The first step [Figure 5(a)] is the deposition and patterning of indium–tin oxide (ITO) to form the pixel electrode. An ITO-first process has the advantage that if wet etching is used, there are no prior metallization levels present which can be attacked by the aggressive etchant. The second step [Figure 5(b)] is the deposition and patterning of the Mo/Al-alloy metallization to form the gate lines. A variety of Al-alloy compositions, which are currently proprietary, were

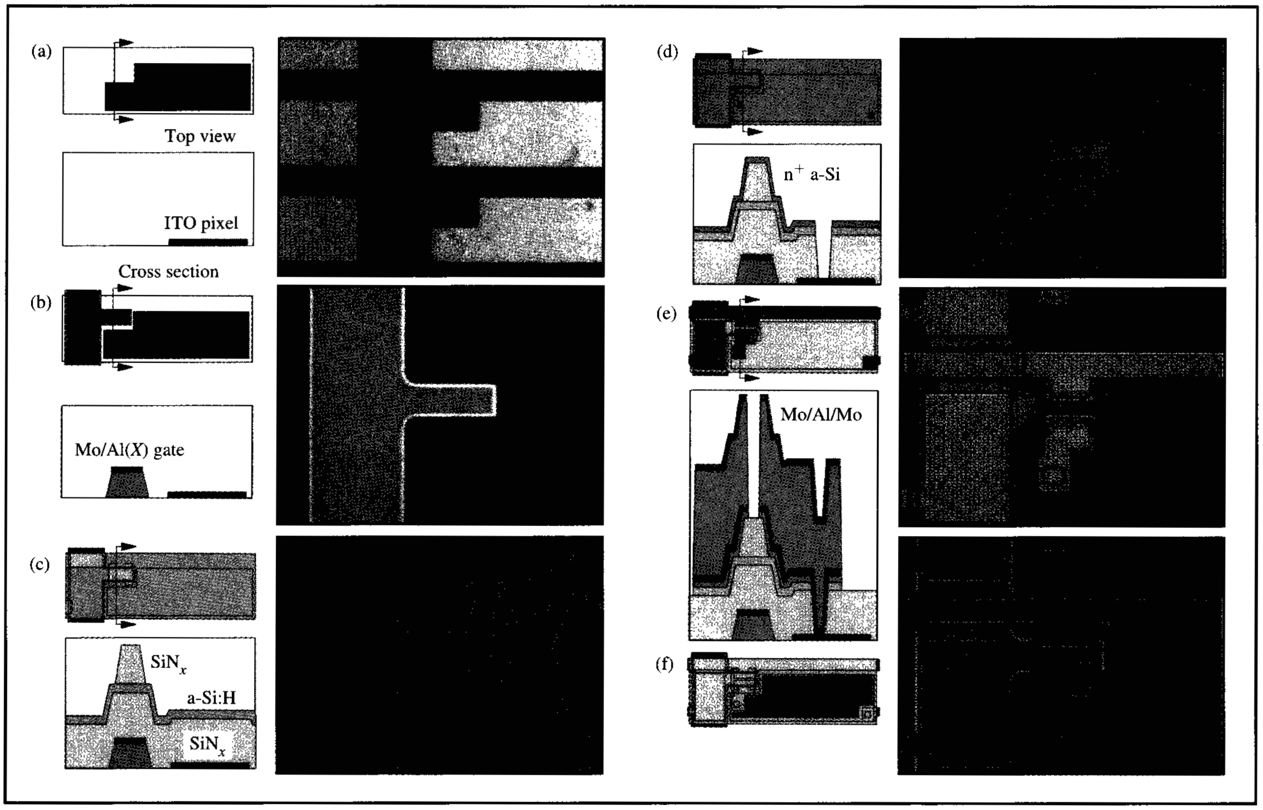
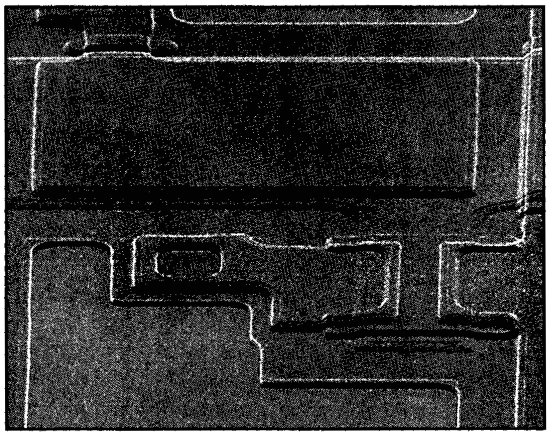


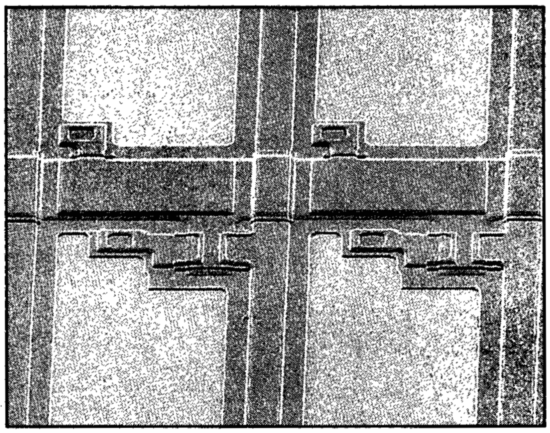
Figure 5

Schematic diagram of six-mask Al-alloy gate TFT process flow, with optical micrographs at corresponding steps. The subpixel size is 162 μm × 54 μm. The process steps are (a) ITO patterning, (b) Mo/Al-alloy gate patterning, (c) IStop patterning, (d) n$^+$ a-Si deposition and via patterning, (e) Mo/Al/Mo data metallization patterning, and (f) passivation patterning. In (b)–(f), the gate-line width is about 28 μm.

used in this work, and are referred to collectively as Al(X). By using immersion etching, whereby the Mo is etched more rapidly than the Al alloy, a taper can be reliably formed on the edges of the features [12]. An edge taper is important to ensure good insulator coverage, which protects the gate lines from attack by subsequent etching steps and minimizes the increase in resistance for crossings of data lines over the insulator topography created by the underlying gate lines. The Mo layer is left in place on top of the gate line to reduce the formation of hillocks and whiskers upon heating during subsequent processing. Unlike the process in which the Al gate is totally covered with MoTa [12], this process does not require an additional lithographic step. The third step [Figure 5(c)] is the plasma-enhanced chemical vapor deposition (PECVD) of a SiN_x/hydrogenated amorphous Si, a-Si:H/SiN_x trilayer, and the wet etching of the upper SiN_x layer. The lower SiN_x layer acts as the gate insulator for the TFT and as the insulator for the storage capacitor formed between the gate and data metallizations. The upper SiN_x layer is patterned to define the TFT channel (center of the I-shaped region on the gate tab) and to provide an additional insulating layer where the data lines cross the gate lines or connect to the storage capacitor. In the case shown, the channel length of the TFT was 6 μm. An advantage of the trilayer TFT is that the a-Si interfaces are formed and passivated *in situ*. The fourth step [Figure 5(d)] is the deposition of a heavily doped n-type microcrystalline silicon layer to form the contacts to the a-Si and the reactive ion etching (RIE) to pattern via openings down to the ITO pixels. A process option at this point is to remove the gate insulator from the entire ITO area with the passivation opening shape instead of just opening two vias. This reduces the time required to expose the ITO during the passivation etching. An RIE process was developed which produces a slight taper to ensure that the data metallization is continuous and forms low-resistance contacts to the ITO areas. The fifth step [Figure 5(e)] is the deposition of the data metallization [typically, thin Mo/Al(X)/thin Mo] and the patterning of both the metal and silicon layers using a combination of wet and reactive ion etching to form the data lines. The lower Mo layer improves the contact resistance and prevents interdiffusion between the Al alloy and Si. An



(a)



(b)

Figure 6

Oblique-angle scanning electron micrographs of the array depicted in Figure 5. The subpixels are 54 μm wide.

RIE process is used to pattern the Si layers after the metal layers are patterned by wet etching. This etching process must be somewhat selective to SiN_x. Note that the process leaves both the a-Si and the n^+-doped microcrystalline Si layers under the data-line metallization, including the storage capacitor. The sixth and last step [Figure 5(f)] is the deposition of a SiN_x passivation layer and RIE to expose the ITO in the array and the data metal in the periphery. The SiN_x over the ITO pixel includes the gate SiN_x; hence, the RIE process must be somewhat selective to the data-line metallization because of the over-etching required to remove the gate SiN_x from the ITO pixels in the array. Oblique-angle SEM micrographs of a completed array fabricated with this process are shown in **Figure 6**. The large taper width ($\geq$1 μm) from immersion etching the Mo/Al(X) gate metallization is apparent in Figure 6(a) at the gate-metal edges.

- *TFT array performance*

The performance of the TFT arrays was evaluated using a dynamic array tester [13] which writes charge to and reads charge from the individual subpixels of the array. Key performance metrics are charge uniformity across the array, the time constant, τ_{arr}, for the TFT to charge the storage capacitors, and charge retention during the frame time. In **Figure 7(a)**, a charge histogram is shown for the Al-alloy gate array depicted in Figures 5 and 6 having TFTs with a channel length of 6 μm. The mean charge was 1.49 pC, with a standard deviation of 0.08 pC. The charge was written to the individual 3.9M subpixels, held for 16 ms (the frame time), and then read out. A contour map of the array showed that the variations were gradual across the array, and that the uniformity was adequate for displaying 6-bit gray levels. In **Figure 7(b)**, the stored charge versus the charging time is plotted for a gate voltage of 24 V. The initial charging curve was fitted to an exponential, and τ_{arr} was calculated to be 1.24 μs. The initial slope of the charge versus charging time plot is equal to the on-current of the TFT. As stated earlier, for driving an SXGA display at 60 Hz with a 6-bit gray scale, a τ_{chg} of 2.7 μs is required. In this design, $C_S + C_{LC}$ is about $1.6C_S$, so τ_{chg} corresponds to $1.6\tau_{arr}$ or 1.98 μs in this case. This TFT process should be extendible to larger-diagonal, higher-resolution displays with a 6-μm channel length. In **Figure 7(c)**, the stored charge after a hold time of 16 ms is plotted against the gate voltage during the hold time. During typical operation, the gate voltage when not enabled was -3 V. The charge uniformity over the range of gate voltages examined indicated that there was no charge-retention problem with the TFT array.

System electronics

- *Approach*

The prototype electronics and display subsystem had two general requirements. On one hand, sufficient flexibility in addressing had to be provided to allow characterization and study of the display performance. Such flexibility is most easily achieved using unique hardware with little concern for packaging and form factor. On the other hand, a system was needed that would allow the display to function with standard personal computers and software and in a compact package, so that portable demonstrations and human-factors studies could be carried out. One motivation for this work was to explore the advantages that high spatial resolution brought to reading from displays. A compromise solution that met these needs is described below. A photograph of the completed display is shown in **Figure 8**. This package proved suitable both for office use and (with its screen folded down) for laboratory measurements.

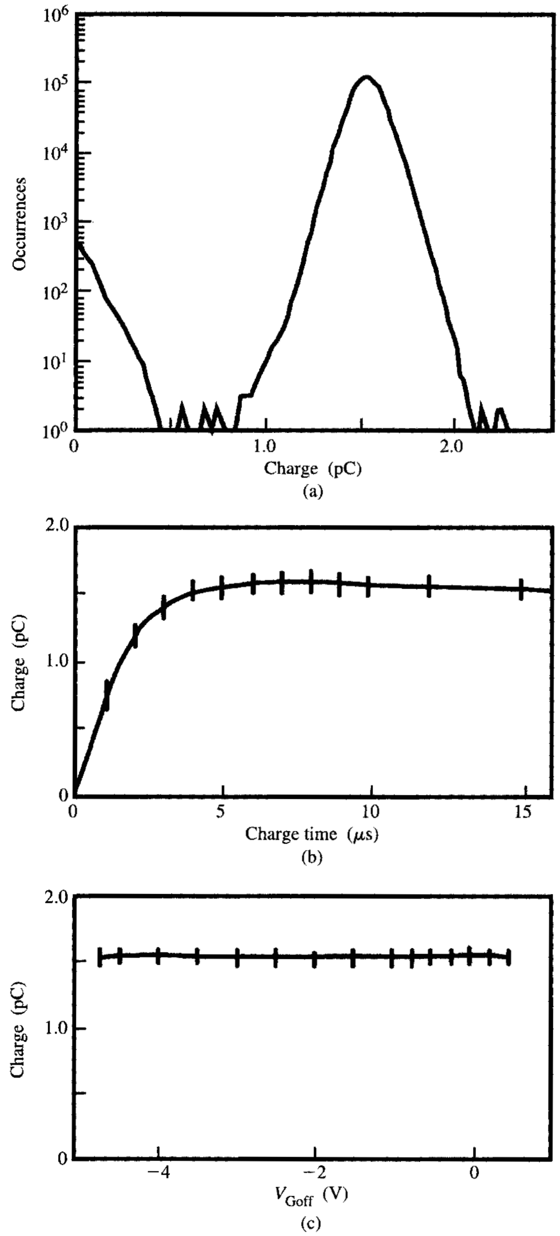


Figure 7

Array test results for Al-alloy gate array having TFTs with a channel length of 6 μm depicted in Figures 5 and 6. A charge histogram is shown in (a), a plot of stored charge vs. charging time is shown in (b), and a plot of stored charge vs. gate voltage during the hold time is shown in (c). The data taken in (b) and (c) were collected from different array locations simultaneously and then combined. Each data point represents the measurement of many pixels.

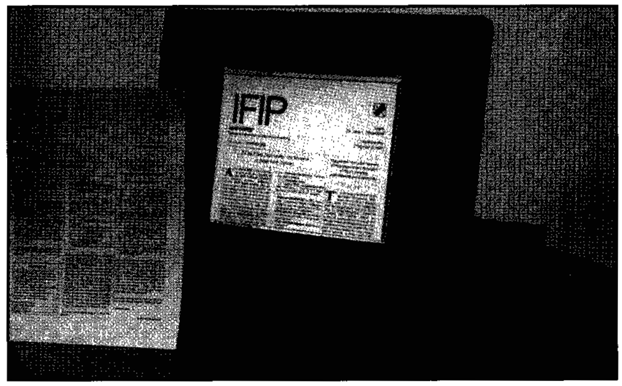


Figure 8

Photograph of packaged SXGA prototype display in operation.

- *Addressing the array*

The first decisions that had to be made were how to address the array and how the addressing electronics were to be packaged. Data drivers with at least 6 bits of resolution were needed. Array design considerations did not permit the use of a separate return line for the pixel storage capacitors, so using a low-voltage design approach such as V_{com} modulation was not an option [14]. Low-voltage (5-V) drivers were used, and the required higher voltages were achieved by dynamically switching the voltage rails of the data drivers. The data drivers were Crystal Semiconductor 55-MHz parts having 201 outputs with 6 bits of voltage precision and a 5-V_{max} specification. Ten data-driver chips were used to drive odd-numbered lines from the top edge of the display, and ten data-driver chips were used to drive even-numbered data lines from the bottom edge. Using 192 outputs from each driver provided the required 3840 data-line signals (1280 pixels × 3 subpixels per pixel). Six of the remaining nine outputs for each driver chip provided active line repair (ALR) signals, as described briefly below and in a related paper [15]. The gate lines were driven by standard-architecture 30-V IBM drivers having 128 outputs. Each gate line was driven from both ends, providing both redundancy and a 4× response-time improvement compared to single-end driving. Sixteen gate-drive chips were used.

The voltage-level shifting of the data drivers was achieved by following an approach proposed by the driver vendor. A high-level schematic of this function is shown in **Figure 9**. This approach proved reliable and effective, and we were able to switch and stabilize the driver rails in approximately 1 μs, using only about 6% of the total gate-line time and fitting within the gate-line time budget mentioned previously. Both discrete and partially integrated versions of this circuitry were used. Note that

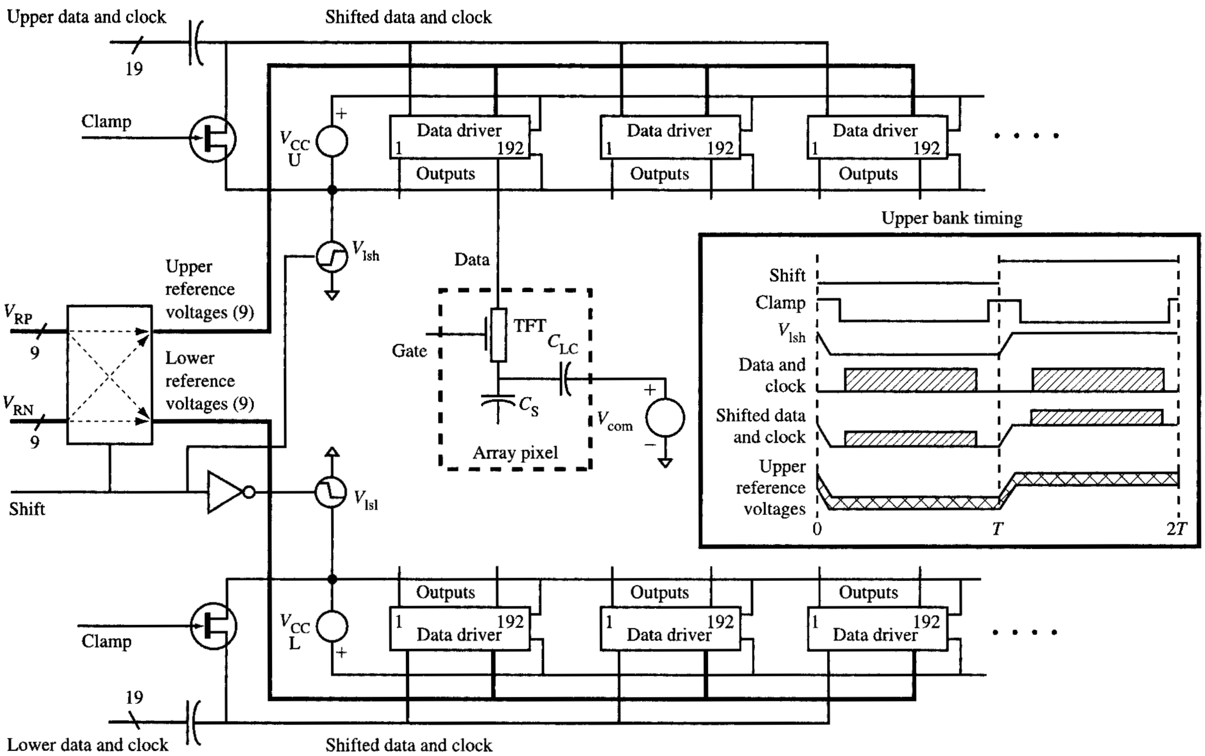


Figure 9

High-level diagram of rail-shifting scheme used for the data drivers. This approach allows low-voltage drivers (5 V) to be used in a display that requires higher voltage (11 V in this case) on the data lines.

in addition to dynamically floating the driver rails, the ground-referenced input signals (data and clock) were level-shifted. This was carried out by the simple expedient of using a capacitor and a reset switch. The reset switch on each data input pin was integrated into recent versions of the data drivers.

The voltage levels used in the display and the relationships among the LC transmission-voltage (T-V) curves, the data-driver reference voltages, and the voltage-shift levels are shown in **Figure 10**. The 6-bit data drivers accept nine reference voltages and internally generate the remaining levels by linearly interpolating between the references. The level-shifted rail voltages for the data drivers are labeled V_{lsh} and V_{lsl}. In all cases the voltage difference between these two rails was 5 V or less. The amplitude of the shift was of the order of 6 V.

We were able to simultaneously load the upper and lower data drivers with the 55-MHz pixel clock and a single data bus for each group of 10 data drivers. Each driver accepted 3 subpixels of data (18 bits) per pixel clock. It thus required (192/3) × 10 clocks or (640/55 MHz) = 11.6 μs to load all 1920 drivers using a single bus. For greater parameter control, however, two data buses were used for the top and two for the bottom. Each set of five drivers could be loaded at lower rates if desired. We typically loaded the data into the drivers with a 40-MHz clock from a FIFO (first-in-first-out) buffer.

- *System partitioning*

The TFT/LCD electronics and display subsystem are shown in **Figure 11**. The functions were distributed over four units. An inner picture-frame circuit board was connected to the display glass via the flex circuits containing the driver chips. This board contained only the display drivers, decoupling capacitors, and six connectors. A socket was provided to allow the optional use of ALR. Since many variations of display processing were used, we wanted to minimize the electronics cost associated with each display. The inner picture frame was electrically connected to an outer picture frame with six low-profile

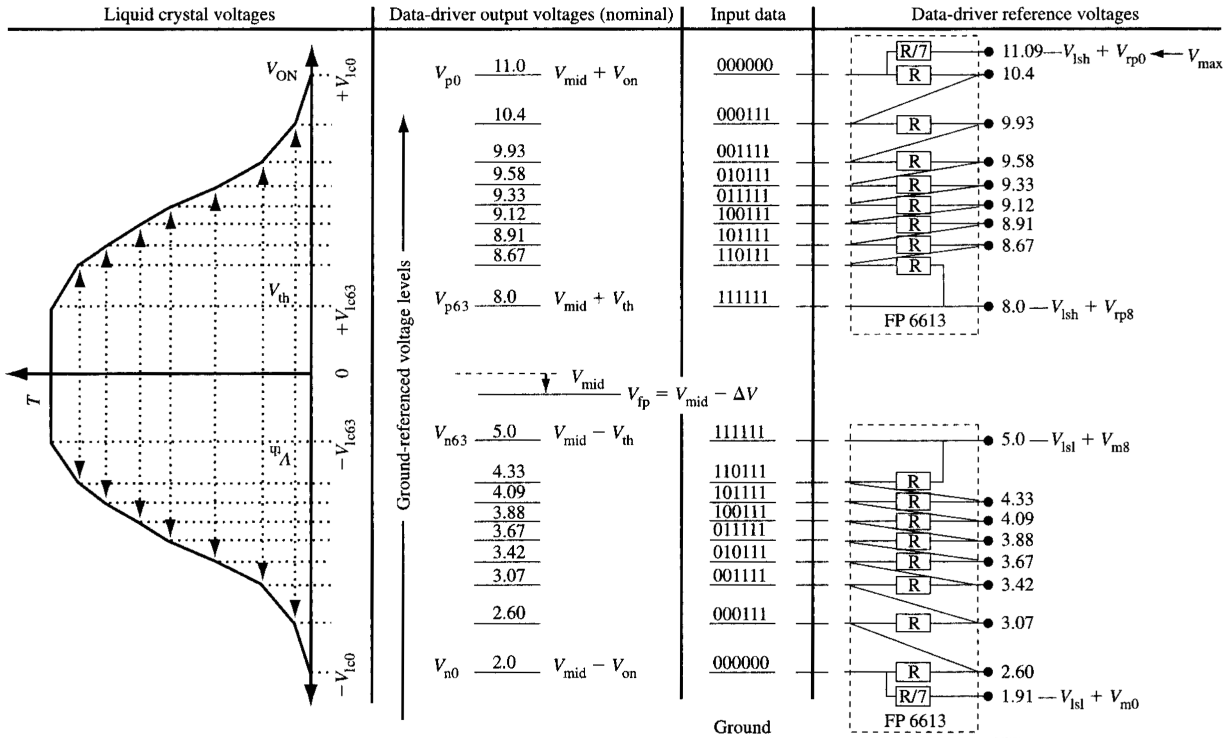


Figure 10

Diagram showing relationships among the LC T-V curve, the ground-based voltages on the display, the input data, and the reference voltages applied to the data drivers.

50-pin connectors and cables. The outer picture frame contained many of the discrete components required for level shifting, and the connectors to the rest of the system. A backlight mounted on the outer picture frame completed the display module. The base unit contained all of the electronics required for voltage generation, control of the display, and pixel formatting, including ALR. This unit served as a mechanical base for the display, which was attached to it with hinges. The fourth unit was the display adapter located in a PCI bus slot of the personal computer used to drive the display. The display adapter was of standard commercial design, using the 968 controller manufactured by the S3 Corporation and the IBM 528 Palette DAC chip (250-MHz version). The adapter was modified to provide synchronization signals and 2-pixel-wide digital output from the palette DAC. The system was typically run under Windows** 3.1 in 1280 × 1024 mode (SXGA) with 24 bits per pixel and a 60-Hz refresh rate. This corresponds to a serial pixel clock of 110 MHz. The serial port of the computer could be used to input display operating parameters.

• *Control features*

All display-addressing voltages and timings having an effect on display performance could be programmably set. While this allowed numerous characterization studies to be carried out, it also presented the problem of how to simply convey this versatility to the user. The approach used was to have all parameters individually keyboard-settable, to provide the user with sets of previously determined parameters, and to develop a simple graphical user interface for display control, described below.

The electronics were controlled by a Philips 552 microprocessor; see Figure 11. This microcontroller could operate autonomously with no connection to a host computer. Display operating conditions were contained in a default EPROM or in one of several user parameter sets stored in a nonvolatile EEPROM. When connected to an external computer via a serial port, it responded to external commands. In addition to setting and sequencing voltages and timings, the microprocessor also monitored the system for proper voltage levels, synchronization signals, and temperatures, shutting down the system if an

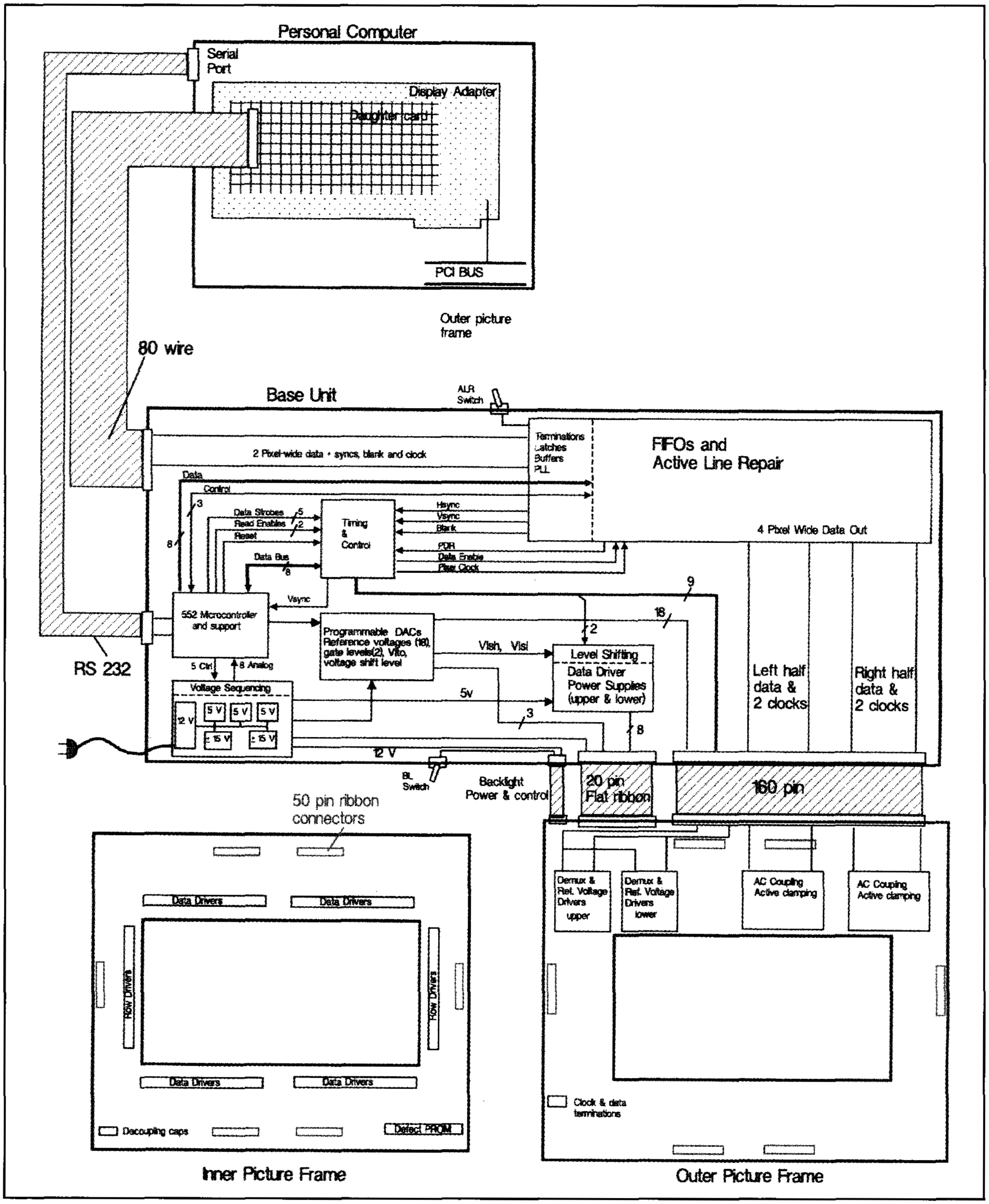


Figure 11

Mechanical and electrical partitioning of prototype SXGA display. Four basic units are shown: the inner picture-frame board, which connects to the display; the outer picture-frame board containing level-shifting components and I/O connections; the base unit, which provides all of the display control electronics and power supplies; and the display subsystem, which is housed in a personal computer.

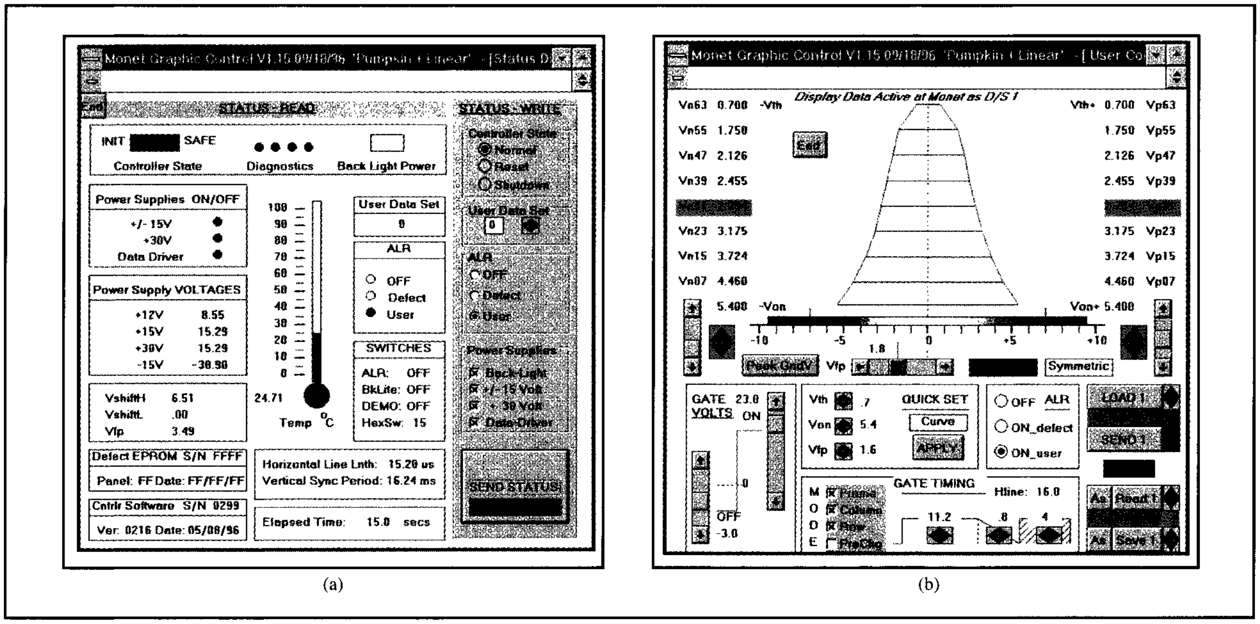


Figure 12

(a) Screen capture of prototype SXGA display status information; (b) screen capture of the user interface for setting display operating parameters.

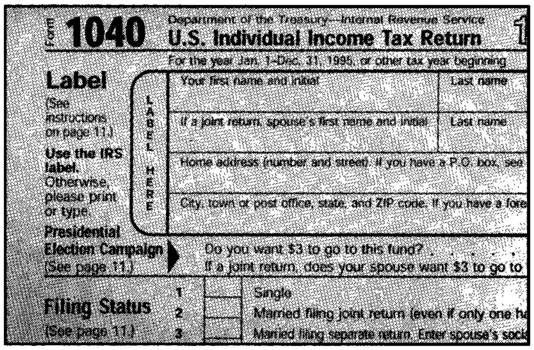
out-of-tolerance condition was detected. All voltages set by the microcontroller were implemented with 12-bit digital-to-analog converters (DACs) having a 10-V full-scale swing. A fixed-voltage-gain stage following the DAC was provided for signals requiring higher voltages.

For long-term stable operation, the net dc content of the liquid crystal excitation had to be under 50 mV. The microcontroller and timing circuits supported three basic modes of inversion control: column inversion, row inversion, and frame inversion. These modes could be selected individually or in combination. Column inversion, for example, involves setting all even columns at one polarity and all odd columns at the opposite polarity during one addressing frame (writing all the pixels from start to finish). During the next frame of information, the column polarities are reversed. Exchanging the word *row* for *column* in the above description describes row inversion. Frame inversion involves setting all pixels at one polarity in a given frame and at the opposite polarity in the next frame. All of these modes (and combinations) provide zero net dc excitation. They differ in their ability to minimize either flicker or crosstalk on the screen. The electronics used also supported choosing pixel precharging or not, doing so in any of the modes defined earlier in this paper.

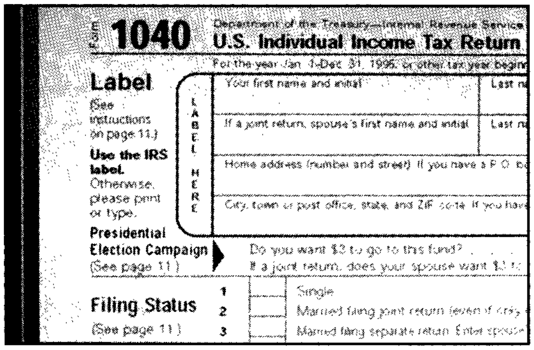
The user interface developed for display status and control is shown in **Figure 12**. The status screen [Figure 12(a)] shows the values and conditions of the important system parameters, which were continuously monitored. To set parameters for display use, an operator used the interface shown in Figure 12(b). The user could control the T-V curve in numerous ways: Setting each of the 18 voltages individually, applying the same voltages for plus and minus fields, quick-setting the T-V curve according to a predetermined algorithm, taking the threshold voltage and the full-on voltages as parameters, loading predefined parameter sets, etc. In every case, a plot of the resulting T-V curve was presented to the user. Also shown in the figure are the controls for selecting an inversion method and for setting the gate timing, the gate voltage level, and ALR.

- *Active line repair (ALR)*

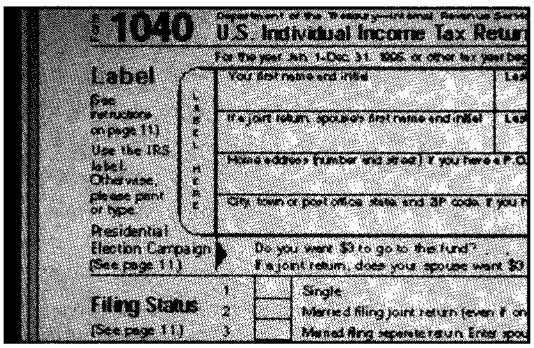
Active line repair is a new technique which was developed to repair open data lines. The technique works by driving both ends of an opened data line with the same data; a normal data line is driven from one end only. This was accomplished by designating several uncommitted data-driver outputs in each driver chip for this task and having a means to connect one of these ALR outputs to a repair bus on the glass outside the LC seal. An EPROM on each display contains information on the defective column numbers and which subpixel(s) is (are) nonfunctional. Circuitry keeps track of data coming into the display.



(a)



(b)



(c)

Figure 13

Photographs of a portion of the 1040 Federal tax form: (a) Printed on a 300-dpi laser printer, (b) rendered on the prototype SXGA display, and (c) rendered on an 80-dpi TFT/LCD with VGA resolution.

When data arrives for a defective column line, it is not only sent to its normal driver, but it is temporarily stored and subsequently fed to a driver on the other end of the open data line after data is supplied to all 192 normal outputs. This digital routing of repair data together with the use of standard data drivers allows accurate, noise-free driving of defective lines; repaired lines appear the same

Table 1 SXGA display prototype parameters.

Parameter	*Value*	*Unit*
Columns	3840	number
Rows	1024	number
Subpixel	54×162	$\mu m \times \mu m$
Subpixel count	3,932,160	number
Color pixel	162×162	$\mu m \times \mu m$
Array diagonal	10.5	inch
Spatial resolution	157	color pixels per inch
Aperture ratio	35	%
Colors	252,144	number
Luminance	120	cd/m^2
Contrast ratio	130	number
Gate metallization	Cu and Al alloy	
TFT	Amorphous Si	
Process steps	6	photo steps
LC effect	Twisted nematic	

as normal lines under row inversion, unless the open also causes a pixel defect because of its location. We were thus able to show line-defect-free operation of our prototype displays, even though these limited-production panels had several open lines. The ALR technique is described in an accompanying paper in this issue [15].

Display performance

The parameters of the prototype SXGA display are summarized in **Table 1**. This display is unique in its combination of spatial resolution, number of colors, and contrast, allowing for the rendering of electronic documents that truly appear to be paperlike. A previous report of high spatial resolution [16] described a display having 150 color pixels per inch, but binary drivers severely limited its ability to render natural images or to anti-alias text. Selections of text rendered on paper, on a VGA TFT/LCD, and on the SXGA prototype are compared in **Figure 13**. The paper sample in this figure was from a 300-dpi laser printer. In comparing this high-resolution electronic display with printer output, one concludes that the printer has less staircasing and better kerning of text. Some observers, nonetheless, prefer the electronic version, probably because of its higher background luminance and higher text contrast. Tests are under way to measure how well the electronic display compares with paper in business reading situations. Continuous-tone images rendered on this SXGA display are comparable in quality to those found in publications such as this one. **Figure 14** compares the halftone color spots on the cover of the previous TFT/LCD issue of this journal with the pixels on the SXGA display. These examples illustrate the excellent image quality provided by the combination of high resolution and gray-scale accuracy in this display.

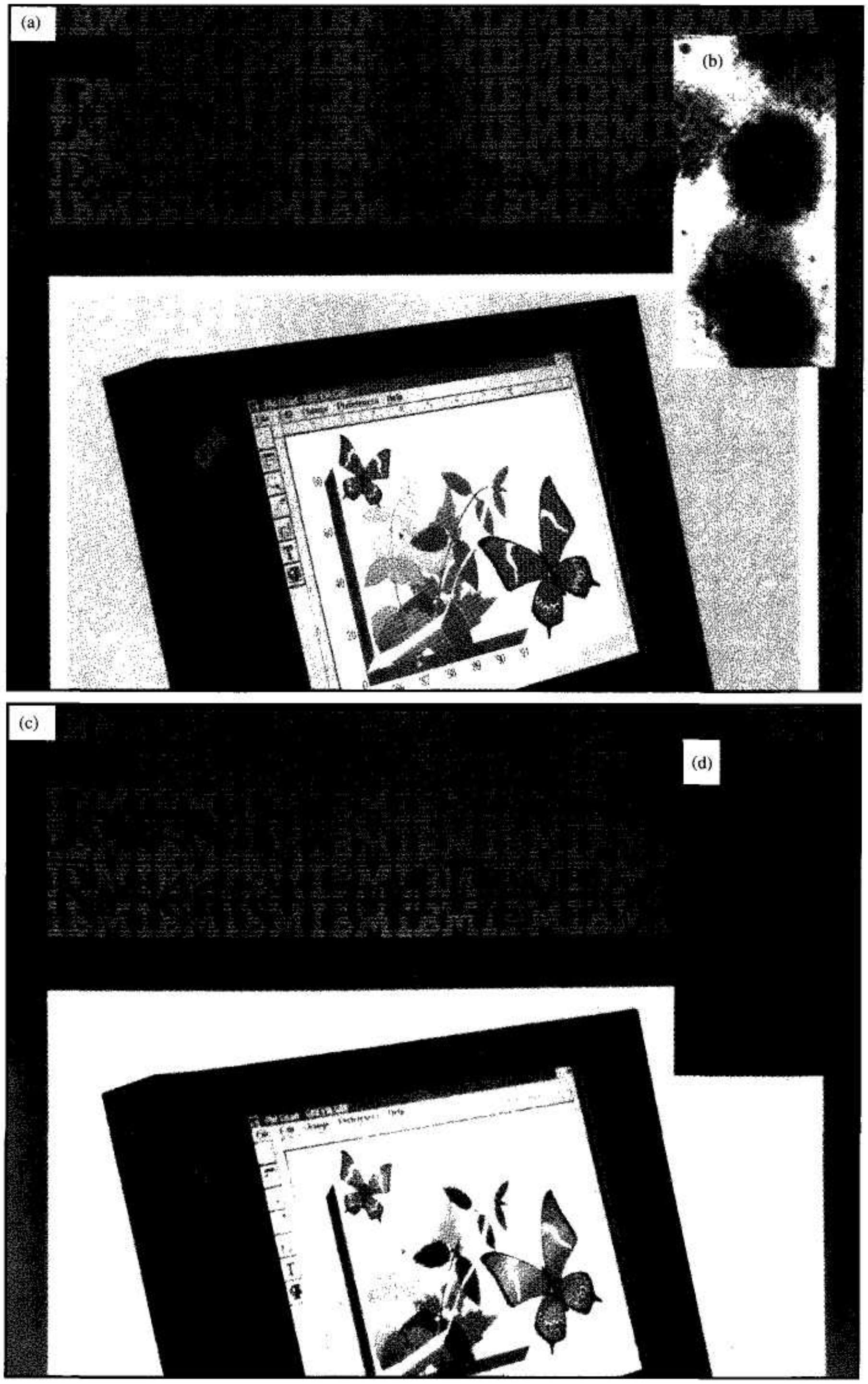


Figure 14

Comparison of basic rendering elements used in color printing and color TFT/LCDs: (a) Scanned image of the printed cover of the January 1992 issue of the *IBM Journal of Research and Development*; (b) color halftone pattern from a section of the cover; (c) photograph of the scanned cover image displayed at actual size on the prototype SXGA display; (d) at the same magnification as (b), color subpixels used to render images on the display. The spatial resolution of the display and journal cover color elements are seen to be comparable.

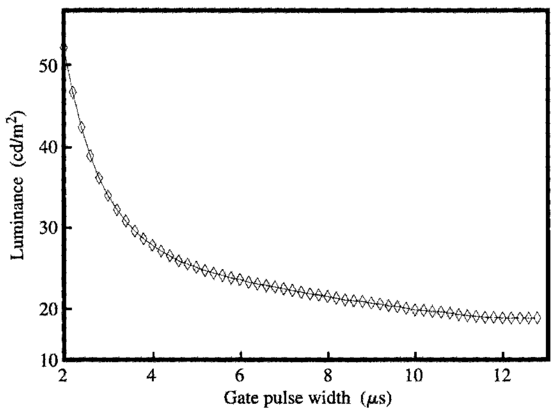


Figure 15

Mid-gray-level luminance vs. gate pulse width, with pixel precharging.

Measurements that relate the observed luminance to the TFT array performance are shown in **Figure 15**, in which the screen luminance is plotted versus gate pulse width with pixel precharge. Dot inversion, which combines column and row inversion, was used in order to minimize crosstalk. The measurements used the 50% gray level because it is most sensitive to shifts in voltage. The channel length of the TFTs was approximately 8 μm. With increasing gate-pulse width, the screen luminance saturated, as expected from the previously described charging time constant.

The power consumed by this prototype was substantially greater than that found in the display subsystem of a commercial notebook computer, though the prototype offered substantially more display performance, highly selectable drive conditions, and new functions such as ALR and system diagnostics. The backlight power was approximately 3 W. The timing, control, ALR, microprocessor, and array drivers required a total of 26 W. Finally, the display adapter accounted for 7.7 W while showing a typical multiwindow image, with extremes of 5.9 W for a typical DOS window and 9.9 W for alternating black and white columns.

Summary

A 157-dot-per-inch, 262K-color, 10.5-in.-diagonal, 1280 $\times$ 1024 (SXGA) display has been fabricated using a six-mask process with Cu or Mo-capped Al-alloy gates. The combination of high resolution and gray-scale accuracy has been shown to render color images and text with paperlike legibility. The relatively low-resistivity gate metallization and trilayer-type TFTs with 6–8-μm channel lengths were fabricated using a six-mask process which should be extendible to larger-diagonal, higher-resolution displays. A combination of double-sided driving and active line repair was used so that open gate or data lines would not result in visible line defects. An extremely flexible drive-electronics system was developed to support the display and characterize its performance under different drive conditions.

Acknowledgments

The authors would like to acknowledge the superb technical support of T. Harris, S. Libertini, D. Manzer, L. Mok, B. Owens, and M. Palomba, and the management support of Dr. S. Depp, without whom this work would not have been possible.

**Trademark or registered trademark of Microsoft Corporation.

References

1. J. Gille, R. Martin, and J. Larimer, "Spatial Resolution, Grayscale, and Error Diffusion Trade-offs: Impact on Display System Design," *Proceedings of the 1994 International Display Research Conference* (Society for Information Display), 1994, p. 381.
2. N. Hirano, N. Ikeda, H. Yamaguchi, S. Nishida, Y. Hirai, and S. Kaneko, "A 33cm-Diagonal High-Resolution Multi-Color TFT-LCD with Fully Self-Aligned a-Si:H TFTs," *Ibid.*, p. 369.
3. A. Naitoh, "History of A4-Size Notebook PC with TFT-LCDs," *Digest of Technical Papers*, Society for Information Display International Symposium, 1996, p. 319.
4. P. Fryer, L. Jenkins, R. John, Y. Kuo, A. Lien, R. Nywening, B. Owens, L. Palmateer, M. Rothwell, J. Souk, J. Wilson, S. Wright, J. Batey, and R. Wisnieff, "A High Resolution Copper Gate TFT/LCD Process," *Proceedings of the 1994 International Display Research Conference* (Society for Information Display), 1994, p. 146.
5. E. G. Colgan, P. M. Fryer, E. Galligan, W. Graham, R. Horton, D. Hunt, L. Jenkins, R. John, P. Koke, Y. Kuo, K. Latzko, F. Libsch, A. Lien, I. Lovas, R. Nywening, R. Polastre, M. E. Rothwell, J. Wilson, R. Wisnieff, and S. Wright, "Copper-Gate Process for High Information Content a-Si TFT LCDs," *Digest of Technical Papers*, International Workshop on Active Matrix Liquid Crystal Displays in conjunction with International Display Workshop '96, Kobe, Japan, 1996, p. 29.
6. R. L. Wisnieff, "AMLCD Design," *AMLCDs '95 Workshop Proceedings*, 1995, p. 25.
7. P. Fryer, E. Colgan, E. Galligan, W. Graham, R. Horton, D. Hunt, L. Jenkins, R. John, P. Koke, Y. Kuo, K. Latzko, F. Libsch, A. Lien, I. Lovas, R. Nywening, R. Polastre, M. Rothwell, J. Wilson, R. Wisnieff, and S. Wright, "Six Mask TFT-LCD Process Using Copper Gate Metallurgy," *J. SID* **5**, No. 1, 49 (1997).
8. S. Takayama and N. Tsutsui, "Low Resistivity Al RE (RE = La, Pr, and Nd) Alloy Thin Films with High Thermal Stability for Thin Film Transistor Interconnects," *J. Vac. Sci. Technol. B* **15**, No. 5, 3257 (1996).
9. S. Takayama and N. Tsutsui, "Effects of Y or Gd Additions on the Structure and Resistivity of Al Thin Films," *J. Vac. Sci. Technol. A* **14**, No. 4, 2499 (1996).
10. H. Takatsuji, E. G. Colgan, C. Cabral, Jr., and J. M. E. Harper, "Evaluation of Al(Nd)-Alloy Films for Application to Thin-Film-Transistor Liquid Crystal Displays," *IBM J. Res. Develop.* **42**, No. 3/4, 501–508 (1998, this issue).

11. T. Arai, H. Iiyori, Y. Hiromasu, M. Atsumi, S. Ioku, and K. Furuta, "Aluminum-Based Gate Structure for Active-Matrix Liquid Crystal Displays," *IBM J. Res. Develop.* **42,** No. 3/4, 491–499 (1998, this issue).
12. T. Tsujimura, H. Kitahara, A. Makita, P. M. Fryer, and J. Batey, "Low Resistance Gate Line for High-Resolution TFT/LCD Display," *Proceedings of the 1994 International Display Research Conference and International Workshop on Active Matrix LCDs and Display Materials*, 1994, p. 424.
13. L. C. Jenkins, R. J. Polastre, R. R. Troutman, and R. L. Wisnieff, "Functional Testing of TFT/LCD Arrays," *IBM J. Res. Develop.* **36,** No. 1, 59 (1992).
14. H. Okada, Y. Ogawa, H. Fukuoka, Y. Kanatani, Y. Sano, Y. Itoh, and M. Hijikigawa, "Development of a Low Voltage Source Driver for Large TFT-LCD System for Computer Applications," *Proceedings of the 1991 International Display Research Conference* (Society for Information Display), 1991, p. 111.
15. S. L. Wright, K. W. Warren, P. M. Alt, R. R. Horton, C. Narayan, P. F. Greier, and M. Kodate, "Active Line Repair for Thin-Film-Transistor Liquid Crystal Displays," *IBM J. Res. Develop.* **42,** No. 3/4, 445–457 (1998, this issue).
16. R. A. Martin, T. Chuang, H. Steemers, R. Fulks, S. Stuber, D. D. Lee, M. Y. T. Young, J. Ho, M. Nguyen, W. P. Meuli, T. Fiske, R. H. Bruce, V. Da Costa, R. P. Kowalski, A. Lewis, W. Turner, M. J. Thompson, M. Tilton, and L. D. Silverstein, "The Electronic Document Display: A 6.3 Million-Pixel AMLCD," *J. SID* **4,** No. 2, 65 (1996).

Received March 17, 1997; accepted for publication February 20, 1998

Evan G. Colgan *IBM Research Division, Thomas J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598 (ecolgan@us.ibm.com).* Dr. Colgan is a Research Staff Member at the IBM Thomas J. Watson Research Center in the Flat Panel Display Technologies area. He previously managed the Thin-Film Transistor Processing Department. Dr. Colgan joined the Research Division in 1995; he was previously an Advisory Engineer at the Semiconductor Research and Development Center in Hopewell Junction, New York. While at the Development Center, since joining IBM in 1987, he worked on aspects of metal silicide formation, selective chemical vapor deposition of tungsten, diffusion barriers, Al(Cu) microstructure evolution, and integration of both Cu- and Al-based metallizations for integration circuits. Dr. Colgan received his B.S. degree in applied physics from the California Institute of Technology in 1982 and his Ph.D. in materials science and engineering from Cornell University in 1987. His thesis work involved the formation of aluminides from thin-film couples. Dr. Colgan has published more than seventy papers and has been issued eleven patents; he is a member of the MRS, IEEE, APS, Bohmische Physical Society, and Sigma Xi.

Paul M. Alt *IBM Research Division, Thomas J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598 (alt@us.ibm.com).* Dr. Alt is a Senior Manager in the Subsystems Technologies Department at the IBM Thomas J. Watson Research Center, where he has been a Research Staff Member since 1970, concentrating on display technologies and display systems. He is a Fellow of the Society for Information Display, a Senior Member of the Institute of Electrical and Electronics Engineers, and a member of the IBM Academy of Technology.

Robert L. Wisnieff *IBM Research Division, Thomas J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598 (wisnieff@us.ibm.com).* Dr. Wisnieff graduated from Tufts University in 1980 with a B.S.M.E. and from Yale University in 1986 with a Ph.D. in applied physics. He joined IBM in 1986, working in the research group developing amorphous-silicon-based active-matrix liquid crystal displays. He earned a Corporate Award for the development of array testing of thin-film transistors. Dr. Wisnieff is currently the manager of IBM's Advanced Display Technology Laboratory. He holds four patents and has authored or co-authored 14 publications, and has given invited talks and seminars on active-matrix technology. Dr. Wisnieff has held the offices of Secretary, Treasurer, Vice Chairman, and Chairman of the SID Mid-Atlantic chapter. He has served on and chaired the SID Symposium Active-Matrix Subcommittee and has been the Seminar and Program Chair of the SID Symposium. He is a member of the ACM, IEEE, and SID.

Peter M. Fryer *IBM Research Division, Thomas J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598 (fryer@us.ibm.com).* Mr. Fryer joined IBM in 1983. He holds a B.S. degree in physics from Iona College, an M.S. in electrical engineering from Polytechnic University, and an M.S. in computer science from Iona College. He currently manages the TFT Array Process group at the Thomas J. Watson Research Center.

Eileen A. Galligan *IBM Research Division, Thomas J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598 (galligan@us.ibm.com).* Ms. Galligan received an associate degree in business from Dutchess Community College in 1984. She joined IBM in 1987 and is currently a Senior Laboratory Specialist working on process development in the area of thin-film transistors and liquid crystal displays.

William S. Graham *IBM Research Division, Thomas J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598 (wgraham@us.ibm.com).* Mr. Graham joined IBM in 1982. He has been a member of the flat-panel display project in the thin-film-transistor group at the Thomas J. Watson Research Center since 1993. Previously he had worked on superconductor technology, mainframe packaging, and contamination control.

Paul F. Greier *IBM Research Division, Thomas J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598 (greier@us.ibm.com).* Mr. Greier joined IBM at the Thomas J. Watson Research Center in 1966 to work on digital interface logic design and laboratory automation. From 1978 to 1982, he worked on systems programming, and participated in the development of VM Host bisynch communications software for distributed data-acquisition systems. He received a B.S. in mathematics from Mercy College in 1980 and an M.S. in computer science from the Polytechnic Institute of New York in 1982. From 1982 to 1983, he worked on developing test software for Josephson-junction devices, and from 1983 to 1989 was responsible for the functional testing of VLSI memory and logic circuit chips. During the 1989–1990 academic year, through the IBM Faculty Loan Program, he taught computer programming and computer architecture in the Computer Science Department of New

Mexico State University. He returned to the Research Center and was responsible for software development in various advanced development projects until 1994, when he began working on hardware and software support in the flat-panel display system area.

Raymond R. Horton *IBM Research Division, Thomas J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598 (hortonra@us.ibm.com).* Mr. Horton served a five-year mechanical engineering apprenticeship at Clayton Dewandre Company, Lincoln, U.K. He joined IBM Research in 1987 with 21 years' mechanical engineering experience. From 1987 to 1995 he was a member of the VLSI packaging group, gaining experience in the area of advanced packaging interconnect technology regarding surface mount component attach and rework. Since 1995, Mr. Horton has been a Development Engineer in the LCD Processing and Display Design group, with responsibilities primarily in the area of interconnection technology. He is an inventor or coinventor of 27 U.S. patents and a coauthor of 51 *IBM Technical Disclosure Bulletin* papers and of several IBM research reports. Mr. Horton received an IBM Research Division Outstanding Technical Achievement Award in 1991, and Technical Group Awards in 1995 and 1996.

Harold Ifill *IBM Research Division, Thomas J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598 (ifill@us.ibm.com).* Mr. Ifill received a B.S. degree from the City College of New York in 1972. He joined IBM in 1973 at their manufacturing facility in New York, New York. Since joining the IBM Research Division in 1975, he has worked in semiconductor injection laser technology, multibeam CRT technology, and the Display Systems group; in 1996 he joined the TFT Processing group at the Thomas J. Watson Research Center.

Leslie C. Jenkins *Retired from the IBM Research Division, Thomas J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598 (ljenk@ibm.net).* Mr. Jenkins received an Associate of Science certification from the Ohio College of Applied Science in 1961. From 1961 to 1975, he worked in the IBM Field Engineering Division. He then joined the Research Division to work on packaging and cooling of superconducting devices and subsequently on TFT/LCD arrays. He received an IBM Corporate Award for his work on the development of a tester for TFT/LCD arrays. Mr. Jenkins retired from IBM in January 1998.

Richard A. John *IBM Research Division, Thomas J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598 (johnr@us.ibm.com).* Mr. John holds an A.A.S. degree from the RCA Institute and attended City College of New York. Since joining IBM in 1967, he has worked on a variety of research projects including integrated-circuit packaging, gas-panel displays, and LED, ink-jet, thermal, and color electrophotographic printing. He is currently involved in the design and fabrication of high-resolution color liquid crystal displays. Mr. John is an inventor or coinventor of three U.S. patents and a coauthor of several published papers.

Richard I. Kaufman *IBM Research Division, Thomas J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598 (kauf@us.ibm.com).* Mr. Kaufman received a B.S.E.E. from Manhattan College in 1987 and an M.S.E.E. from the Polytechnic Institute of New York in 1991. He is an Advisory Engineer in the Central Scientific Services Department at the Thomas J. Watson Research Center. In 1994 he received an IBM Outstanding Technical Achievement Award for his work on the Scalable Parallel Processor supervisory system. Mr. Kaufman is currently working on electric circuits for high-performance AMLCD systems.

Yue Kuo *IBM Research Division, Thomas J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598 (ykuo@us.ibm.com).* Dr. Kuo is a Research Staff Member in the Thin Film Transistor Liquid Crystal Display Department at the Thomas J. Watson Research Center. He received an M.S. and a Ph.D. from Columbia University in 1979. Dr. Kuo has worked on thin-film transistors and plasma technology since joining IBM in 1987. Previously, he had worked on VLSI MOS and bipolar devices and circuits. He has reached two IBM invention plateaus as a result of his work on thin-film-transistor structures, processes, and materials. Dr. Kuo has published more than 100 papers as the major author, presented over 30 invited talks, and organized and chaired numerous international conferences. He is a Senior Member of the IEEE and a member of the Electrochemical Society and the Materials Research Society.

Alphonso P. Lanzetta *IBM Research Division, Thomas J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598 (ptlanz@us.ibm.com).* Mr. Lanzetta joined the IBM Research Division in 1988 after having worked for twenty years as a mechanical designer. He currently designs printed-circuit boards and is a coauthor of many technical papers and an inventor or coinventor of 22 U.S. patents. Mr. Lanzetta received an IBM Outstanding Technical Achievement Award in 1991, an IBM Technical Group Award in 1993, an IBM Research Division Award in 1994, an IBM Technical Group Award in 1995, and an IBM Research Division Award in 1997.

Kenneth F. Latzko *IBM Research Division, Thomas J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598 (latzko@us.ibm.com).* Mr. Latzko graduated from the Lincoln Technical Institute in 1990 with an A.S.T. degree in electronics technology. He then joined IBM at the Thomas J. Watson Research Center. Until 1994, he worked on silicon LPCVD processing; since then, he has worked on PECVD and RIE for thin-film-transistor liquid crystal displays.

Frank R. Libsch *IBM Research Division, Thomas J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598 (libsch@us.ibm.com).* Dr. Libsch received a B.S. degree in 1982, an M.S. degree in 1984, and a Ph.D. degree in 1989 from Lehigh University, all in electrical engineering. In 1989, he joined IBM at the Thomas J. Watson Research Center, where, as a Research Staff Member, he has worked on aspects of drive schemes and electronics, pixel design, CMOS FETs and TFTs, and their application in various direct-view and projection, transmissive and reflective flat-panel displays. Dr. Libsch currently manages a group engaged in advanced flat-panel display devices, processes, and testing research. He holds several U.S. and foreign patents and is the author or coauthor of more than 50 technical publications, including a recent book chapter entitled "SONOS Nonvolatile Semiconductor Memories" in the book *Nonvolatile Semiconductor Memory Technology*. Dr. Libsch is a member of the IEEE, the Society for Information Display, the New York Academy of Sciences, and Sigma Xi. He currently serves as the chairperson of the AMLCD Subcommittee of the Society for Information Display and as a member of the Executive Committee of the Society for Information Display.

Shui-Chih Alan Lien *IBM Research Division, Thomas J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598 (salien@us.ibm.com).* Dr. Lien received a B.S. degree in physics from National Taiwan Normal University, Taipei, Taiwan, in 1977, and an M.S. degree in electrical engineering and Ph.D. degree in physics from the University of Minnesota, Minneapolis, in 1984. From 1984 to 1987, he worked at Optical Imaging Systems, Inc., Troy, Michigan, where he was involved in the development of large-area active-matrix liquid crystal displays. In 1987, Dr. Lien joined IBM at the Thomas J. Watson Research Center, where he is currently a Research Staff Member in the Flat Panel Display Technologies group. His research interest is in liquid crystal display physics and technology. He is an author or coauthor of five U.S. patents and 70 technical papers. Dr. Lien is currently a member of the Board of Directors of the International Liquid Crystal Society and a member of the Liquid Crystal Technology Subcommittee of the Society for Information Display.

Steven E. Millman *IBM Research Division, Thomas J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598 (millman@us.ibm.com).* Dr. Millman received a Ph.D. in physics from Boston University in 1983. He joined IBM in 1982 as a Research Staff Member in the Magnetic Recording Department at the Almaden Research Center. In 1988 he moved to the Thomas J. Watson Research Center. Dr. Millman's current interests include system and application software for enabling prototype high-pixel-density displays to function with modern operating systems.

Robert W. Nywening *IBM Research Division, Thomas J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598 (nywen@us.ibm.com).* Mr. Nywening is a Senior Associate Engineer working in the Advanced Array Processing and Test group at the Thomas J. Watson Research Center's Flat Panel Display Laboratory. He joined the IBM Federal Systems Division in Owego, New York, in 1980, working on circuit packaging. He held several manufacturing support positions at the IBM Owego, New York, and Boulder, Colorado, facilities before joining the Thomas J. Watson Research Center in 1986. Mr. Nywening has studied computer science at Pace University in Pleasantville, New York, and is a member of the Society for Information Display.

Robert J. Polastre *IBM Research Division, Thomas J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598 (polastr@us.ibm.com).* Mr. Polastre is a Staff Engineer working in the Advanced Array Processing and Test group. He joined the IBM Research Division in 1983 with an associate degree in electronic technology and a bachelor's degree from LaSalle University. Mr. Polastre received an IBM Outstanding Technical Achievement Award in 1990 and an IBM Corporate Award in 1993 for his work on a dynamic array tester. He is the author or co-author of several papers on TFT/flat-panel testing and is a coinventor of patents in this area. Mr. Polastre is a member of the IEEE and an officer of the Mid-Atlantic Chapter of the Society for Information Display.

Carl G. Powell *IBM Research Division, Thomas J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598 (powellc@us.ibm.com).* Mr. Powell is a Staff Engineer in the Flat Panel Display Technologies Department at the Thomas J. Watson Research Center. He joined the Research Division at Yorktown Heights in 1966 and has worked on laser optical systems, surface acoustic wave devices, and analog and digital circuit design. Mr. Powell is currently working on digital display controllers.

Rick A. Rand *IBM Research Division, Thomas J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598 (rarand@us.ibm.com).* Mr. Rand received a B.S.E.E. degree from the Cooper Union, New York City, and an M.S.E.E. degree from the University of Pennsylvania. He joined the IBM Research Division in 1985, working on the development of the SP1 and SP2 Scalable POWERParallel Systems. He was subsequently responsible for the development of the controller section of an SXGA display system. Currently Mr. Rand is in the VLSI design group, working on future System/390 projects.

John J. Ritsko *IBM Research Division, Thomas J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598 (ritsko@us.ibm.com).* Dr. Ritsko received a Ph.D. in physics from Princeton University in 1974. From 1974 to 1983, he worked at the Xerox Webster Research Center, where he carried out fundamental studies of the electronic structure of organic and molecular solids using high-energy inelastic electron-scattering spectroscopy. He joined the IBM Research Division in 1983 as a Research Staff Member in the Packaging Technology Department. He subsequently managed research and development projects in multilayer ceramic packaging used in bipolar mainframe computers and multilayer thin-film wiring packaging used in CMOS mainframe and mid-range servers. In 1993, Dr. Ritsko joined the Flat Panel Display Department, which he now manages.

Mary Beth Rothwell *IBM Research Division, Thomas J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598 (mbroth@us.ibm.com).* Ms. Rothwell joined the IBM Research Division in 1985. She first worked in an electron-beam lithography group and then, in 1991, joined the TFT processing group. She received a B.S. in chemistry from

Pace University, Pleasantville, New York, and is currently an Engineer working on exploratory process development for TFT fabrication.

John L. Staples *Retired from the IBM Research Division, Thomas J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598.* Mr. Staples received a B.S. degree in electrical engineering from Fairleigh Dickinson University. Upon joining the Thomas J. Watson Research Center, he worked in a variety of areas, including high-frequency transistors, Gunn-effect microwave devices, plasma display devices, multibeam high-resolution CRT displays, high-resolution laser printers, rf data entry devices, rf and EMI detection and suppression, and an aerial image measurement system. Mr. Staples also worked on the development of high-resolution liquid crystal color display systems. He is an inventor or coinventor of several U.S. and foreign patents and is an author or coauthor of several technical papers. Mr. Staples retired from IBM in March 1998.

Kevin W. Warren *IBM Research Division, Thomas J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598 (kwwarren@us.ibm.com).* Dr. Warren is currently Manager of the Flat Panel Display Systems group. He received a B.S. in computer engineering in 1983, an M.S. in computer engineering in 1984, and a Ph.D. in electrical engineering in 1990, all from the University of Illinois at Urbana-Champaign. Dr. Warren joined IBM Research in 1992. His primary areas of interest have included display systems support for high-image-content (multimillion-pixel with deep color) TFT/LCD displays and systems configurations utilizing flat-panel displays. Dr. Warren has received two technical group awards; he has twelve publications, holds four patents, and has two patents pending.

John S. Wilson *IBM Research Division, Thomas J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598 (wilsonj@us.ibm.com).*

Steven L. Wright *IBM Research Division, Thomas J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598 (wrightsl@us.ibm.com).* Dr. Wright is a Research Staff Member in the Flat Panel Display Technologies group. His master's thesis work at the University of Colorado and doctorate work at the University of California at Santa Barbara involved crystal growth of III–V compound semiconductor materials, including the growth of GaP on Si (211) surfaces by molecular beam epitaxy and fabrication of bipolar transistors with a wide-bandgap emitter. After joining IBM in 1982, he continued work on molecular beam epitaxy of III–V materials for high-speed devices, including the first reliable measurements of GaAs/AlGaAs heterojunction band offsets, and fabrication of AlGaAs/GaAs bipolar transistors with graded-gap InGaAs emitter contacts. In 1991, he began work on flat-panel display technology for high-resolution TFT/LCDs. Areas of interest include PECVD materials and a-Si TFT characterization; array design, test, and repair; and front-of-screen characterization. Dr. Wright has received five IBM Invention Achievement Awards, an IBM Outstanding Technical Achievement Award, and an IBM Technical Group Award; he has contributed to more than 120 publications.