Silicon light-valve array chip for high-resolution reflective liquid crystal projection displays

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A crystalline silicon active-matrix 2048 × 2048-pixel light-valve array chip has been designed and fabricated as part of the development of a reflective liquid crystal technology for projection displays. The small feature processing and higher circuit performance available with crystalline silicon technology were exploited for the design and fabrication of the active-matrix chip. A 10-V CMOS process was developed to satisfy active-matrix pixel-cell requirements. Row-selection circuits were integrated which incorporate redundant data paths. Adjacent-line demultiplexing circuitry was integrated to minimize the number of external data drivers, to minimize the number of connections, and to maximize chip yield. The pixel, row-driver, and data-driver demultiplexing circuit designs and performance are discussed. The testing methods are presented. The chip is 64 mm on a side and is used in a prototype rear-projection color display system. Companion papers describe the system and its additional components incorporated in the prototype display system.

Introduction

The chip described in this paper was designed, fabricated, and incorporated in a prototype rear-projection color display system [1]. The liquid crystal (LC) cell which was fabricated on the array chip is described elsewhere in this issue [1], as are the LC mode, reflective metallization layers, light-valve packaging, and other components of the prototype display [2–4].

Transmissive liquid crystal active-matrix light-valve arrays are widely used in front- and rear-screen-projection display systems. Reflective arrays are coming into use

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because they offer more light output at high resolution than transmissive light valves because of their higher effective aperture ratios, and because they permit the use of crystalline silicon technology. Amorphous silicon and high-temperature polysilicon technologies are being used for transmissive projection displays having VGA, SVGA, and XGA formats. For higher-resolution applications, optical throughput or efficiency falls off because of a decreasing pixel aperture ratio. A reflective single-crystal silicon approach is better suited for such applications, since the pixel and array infrastructure consisting of row and column conductors, pixel transistors, and capacitors is beneath the pixel mirrors. Thus, the aperture ratio is limited only by the minimum spacing between the mirrors. Carrier mobility is much higher in crystalline silicon, permitting the faster addressing rates required in high-resolution displays.

Reflective single-crystal silicon light valves with resolution as high as SXGA have been fabricated using binary-state deformable mirrors [5] and surface-stabilized ferroelectric liquid crystals [6]. Single-crystal silicon has also been used in transmissive active-matrix LC displays [7], using twisted nematic LC material. Recently, reflective arrays with polymer-dispersed and vertically aligned liquid crystal materials have been reported [8, 9]. The highest-resolution display reported so far is an SXGA 1280 × 1024-element array. The combination of reflective single-crystal silicon and twisted nematic LC provides even higher pixel apertures, resolution, and gray-scale capability. As a vehicle to demonstrate its capabilities, a 2048 × 2048 array with a 17-μm-pixel-pitch design objective was established.

Array design choices

Standard active-matrix addressing consists of selecting one row or gate line at a time from top to bottom of the array while the column or data drivers provide the voltage levels to be written to the pixels. The DRAM-like pixel circuitry consists of a transistor having a gate that connects to a gate line, a source that connects to a data line, and a drain that connects to a storage capacitor and mirror electrode. When the gate of the transistor is made active by gate-line selection, the voltage on the data line is written onto the LC mirror and storage capacitor. The LC voltage is the voltage difference between the mirror electrode and a transparent conductor on a cover glass. The twisted nematic liquid crystal mode used in these devices requires a drive voltage level of approximately 3 V_{RMS} or 6 V peak to peak. A gate-line voltage of approximately 10 V is needed to ensure proper switching of the transistor.

A very important aspect of the array design is the pixel cell structure. The cell must store and sustain the accurate LC voltage levels needed to produce a large number of gray levels and function in a high-resolution array under intense illumination. The high voltage and the large lithographic exposure fields are not commonly available in existing CMOS fabrication processes. With concern for chip yield, decisions on whether to integrate the gate and data drivers or to use external drivers requiring thousands of input connections had to be made. Connection possibilities include wire bonds, solder balls, and anisotropic conducting film tabs. While the light-valve array structure is relatively simple, testing could not be ignored. Design choices could require new testing methods to be developed. In addition to the technology details, factors affecting display system performance had to be considered. A flicker-free, uniform display operation requires the use of high frame rates (74 Hz) and the use of column, row, or even pixel inversion capability. Noticeable crosstalk between pixels must be avoided.

After considering these issues, we chose to develop a new process specifically for our light-valve application and to integrate the row drivers. To minimize the design cycle time, external data drivers were chosen, and the number of inputs to the array from the data drivers was reduced by means of integrated data-driver demultiplexing circuitry. A diagram of the overall light-valve array structure is shown in **Figure 1**. The row drivers are on both sides of the array, and each gate line is driven at both ends. The data-line demultiplexers are located at the top and bottom of the array. Each input from the data driver is demultiplexed to two adjacent data lines. Top and bottom interleaved data-line pairs enable column pair inversion for minimizing flicker. For testing purposes, the data lines are terminated with diodes which are reverse-biased in normal operation. Signal and power-supply connections for the 1024 data-driver outputs, demultiplexers, and row drivers are made using a currently proprietary process for tabbing to silicon using anisotropic conducting films, which are heat- and pressure-cured epoxy layers with conducting spheres interspersed. Six external 198-output data-driver chips are used [1]. The final chip size is 64 mm by 64 mm.

Silicon light-valve array process

A medium-voltage CMOS process has been developed for the silicon light-valve array to meet the pixel-cell requirements. Many associated process details are currently confidential. The "front-end-of-line" process, up to the first metallization layer, is based on an n-well-on-p-epi-Si-substrate, 1.2-μm, single-level-polysilicon, double-level-metallization 5-V CMOS process. The metallization-related portion of the process, from first-level metallization to third-level metallization and spacer posts (for the liquid crystal cell), is based on an 0.8-μm triple-level-metallization process with tungsten via contacts. To provide for a 10-V operating range, pixel charge storage

capacitance, and good optical characteristics, the following process modifications were implemented:

- Thicker gate oxide (450 Å).
- Minimum gate length: 2.0 μm for both n-channel and p-channel devices.
- Additional mask process for n-channel masked lightly doped drain (LDD) structure.
- Tapered first-level-polysilicon layer edges.
- Second-level-polysilicon layer for storage capacitance.
- A single via mask for metal-to-metal layer connection.
- Chemical-mechanical polishing for a planar second-level metallization.
- Light-absorbing second-level-metallization layer.
- Chemical-mechanical polishing third-level metallization to achieve a planar surface; third-level metallization forms the reflective liquid crystal electrodes.
- Relatively thin third-level metallization to minimize surface roughness.
- Relatively thick SiO_2 spacer post structure on mirror layer for LC cell gap control.

Since the array size needed for efficient illumination was too large for stepper lithography, a 1× lithographic exposure tool was used. In order to meet the 1× magnification exposure tolerance specifications, modified layout design rules were used. The resulting process provided the required operating voltages, chip size flexibility up to a 5-in.-diameter wafer size, and good optical performance. **Figure 2** shows a cross section of the resulting silicon light-valve array structure, showing the processing attributes listed above.

Transistor models

Because use was made of a modified silicon chip fabrication process, and to ensure performance of the array, the row and data demultiplexing circuits, and the overall system, modified transistor models had to be developed. For initial circuit design, modified BSIM transistor simulation models were used. When test wafers became available containing 5-V n-MOS, 10-V n-MOS, and 10-V p-MOS transistors with a range of widths and lengths, nominal analog BSIM3 [10] level-two models were extracted. The extracted models gave good agreement with measured data, with RMS errors less than 0.8% and worst-case errors of less than 13% over 2–10-μm channel lengths and 3.8–50-μm channel widths. **Figure 3** shows the fit that was obtained for the 10-V p-MOS transistor with a bulk-to-source voltage of 4 V. The transistor models allowed accurate simulation of the gate-line drive, data-line drive, and array transient response and helped to ensure that the design would meet or exceed requirements.

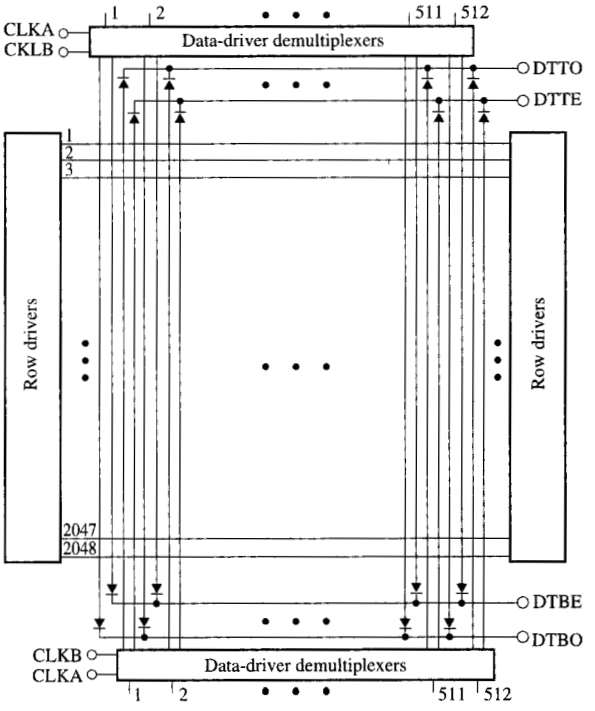

Figure 1

Overall structure of 2024 × 2048 reflective light-valve array chip. Gate lines are driven from both ends. External data drivers with integrated demultiplexers at top and bottom are used. Data lines are terminated with diodes (for testing).

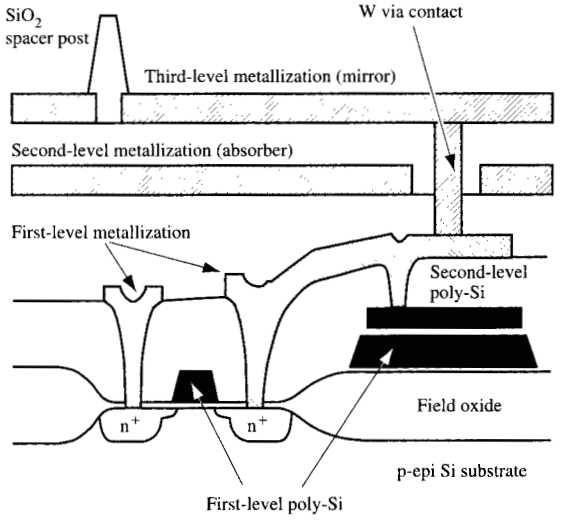

Figure 2

Cross section of silicon light-valve array structure.

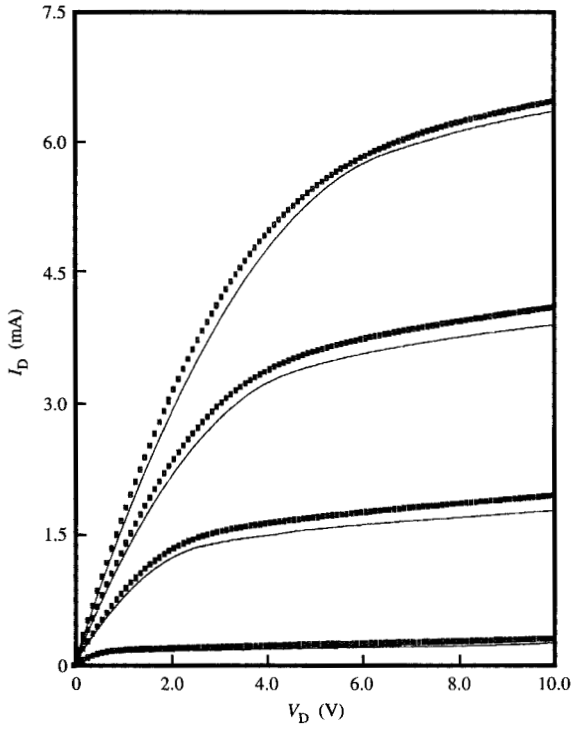

Figure 3

Image of an extraction program output, showing a comparison of BSIM3 model (solid line) with measured data (squares). Data are for a p-MOS transistor having $W/L = 50/2$, bulk-to-source voltage of 4 V, and gate-to-source voltage of -3, -5.33, -7.66, and -10 V.

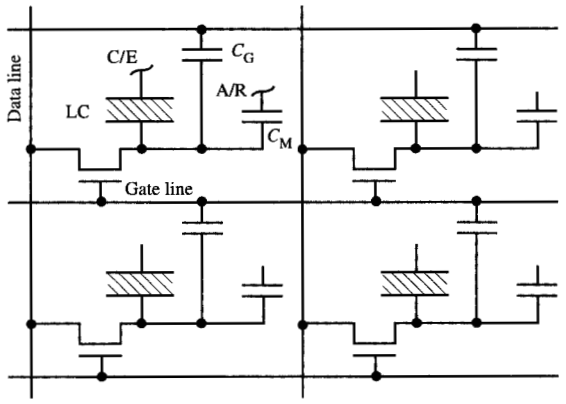

Figure 4

Schematic of a four-pixel section of array. C/E is the counter electrode of the liquid crystal cell, A/R is the second-level-metallization light absorber, C_G is the capacitance between the second-level polysilicon cell electrode and the preceding gate line, and C_M is primarily the capacitance between the third-level-metallization (mirror) electrode and A/R.

Pixel cell design

Figure 4 shows a schematic of a four-pixel section of the array—a small portion of the active matrix that is integrated into the array chip. **Figure 5** shows a layout of one pixel cell. The pixel MOSFET receives the gate pulses from the gate line and transfers data voltage from the data line to the pixel electrode. The latter is composed of the MOSFET drain, third-metallization-level (aluminum) mirror that also serves as an electrode of the liquid crystal (LC) cell, and a storage capacitor electrode. The other liquid crystal electrode is the transparent counter electrode (C/E) on the glass plate which encapsulates the liquid crystal layer [2]. The considerations which defined the pixel cell design and the aspects of the process that were specific to this application are summarized as follows:

- The pixel size was selected as 17 μm $\times$ 17 μm to provide space for sufficient cell capacitance while keeping the array size within reasonable bounds to facilitate the design of moderate-cost illumination and projection optics. A large cell capacitance is important because it minimizes the effect of charge injection into the cell when the gate turns off, the effect of charge leakage from the cell, and the effect of crosstalk due to capacitive coupling from the data lines to the pixels. With crystalline silicon pixel MOSFETs, in contrast to the amorphous silicon or polycrystalline silicon thin-film transistor arrays which are more commonly used, the transistor has a low enough resistance when turned on that there is no problem of excess cell charging time due to cell capacitance.
- The pixel transistor is an n-MOS transistor to achieve maximum transconductance with minimum channel width. A CMOS cell design would reduce the required amplitude of the gate pulses, but would dictate the use of two gate lines per row, carrying gate pulses of opposite polarity. CMOS cells would also require that space be taken in the cell to distribute n-well bias, reducing the available capacitance.
- A second polysilicon level (poly-2) is provided in the technology to supply a capacitance C_G from the pixel cell electrodes to the first-polysilicon-level (poly-1) gate line of the preceding row in the direction of the sequential application of the gate pulses to the rows. The poly-1 gate line is widened to fill the available space in order to maximize the capacitance. Both polysilicon levels are also used for interconnections outside the

bounds of the active matrix, since only the first of three metal layers is usable for interconnections.

- It is necessary to block the incident illumination passing through the gaps between the pixel mirrors from the silicon substrate because the photocarriers generated in the silicon would severely degrade the operation. A second absorber/reflector metal layer (A/R) is provided between the first-metal interconnection layer and the third-metal-layer mirror. A/R is continuous except for openings for the vias carrying the pixel voltage from the first-level metallization (metal-1) to the mirrors. Metal-1 underlies the apertures as a further light barrier. The A/R layer is biased at the same fixed voltage as the counter electrode, so that in the present case of a normally dark liquid crystal mode, the gap between mirrors produces a dark image. The mirror to A/R capacitance, C_M, together with C_G, contributes most of the cell capacitance.

Integrated row drivers

In active-matrix addressing, row drivers apply pulses to the gate lines to select rows, sequentially, one at a time from top to bottom. While data voltages are presented on the data lines, a high voltage on the gate line turns on the pixel transistors that charge the pixel capacitors to the data voltage presented. As dictated by the pixel-cell design, the gate lines consist of polysilicon having a much lower conductivity than conventional Al-alloy wiring. Since a large portion of the cell storage capacitance is coupled to the previous gate lines, the gate lines also have high capacitances. Pulse propagation on the gate lines was simulated using lumped RC approximations to the distributed resistance and capacitance of the lines. Models having 100 lumped RC sections were compared to an analytical model [11] and found to be in excellent agreement. Using the lumped-element circuit simulation, the skew in the times at which transistors switch at various points along the line was found to be too great when the lines are driven at one end. Driving the gate lines from both ends, the time skew (between the ends and the middle) is less by a factor of 4 and is satisfactory. Gate-line precharging is incorporated; that is, the following gate-line pulse turns on before the present one turns off, so only the skew of the turn-off contributes to the row-selection time.

For the 2048 × 2048-array, 4096 row-driver and row-selection circuits are needed. Commercially available row-driver circuits have as many as 56 transistors per driver circuit. With 4096 such driver circuits, more than 200000+ transistors would be required and would have a significant impact on the overall chip yield. Row-driver yield impact was reduced in two ways. First, the number of transistors needed to select and drive a row line was minimized. Second, redundancy was used in the row-line selection path. Row selection is performed by shift registers. Without redundancy, a row-selection failure at the 1000th

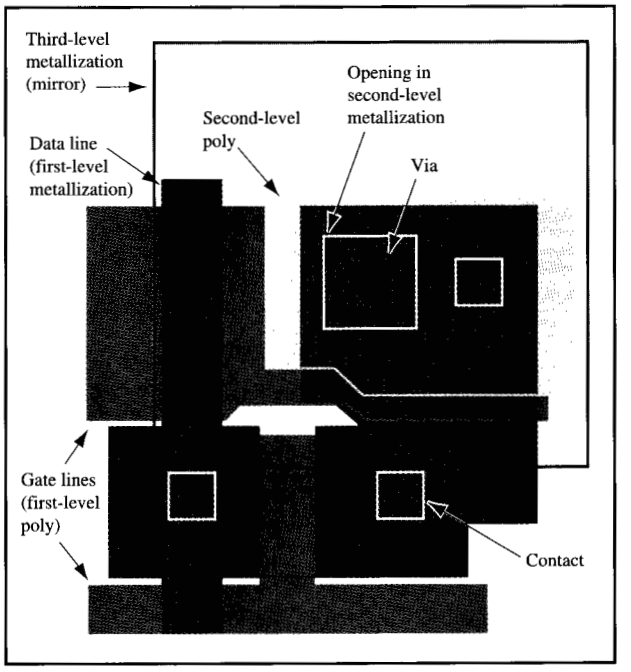

Figure 5

Layout of prototype pixel cell.

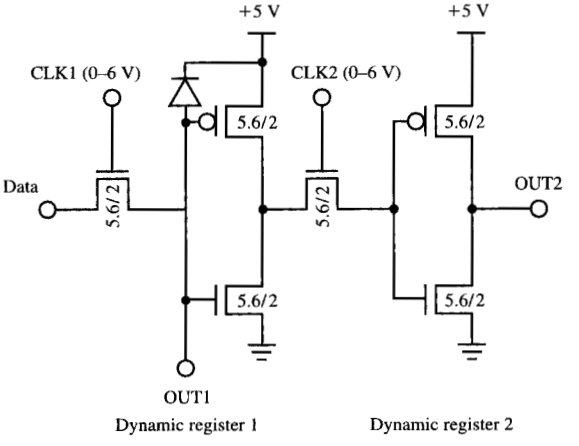

Figure 6

Row-driver selection circuit. Two dynamic registers form a shift register with two positive data-row-line selection outputs. The first dynamic register output can be used, since row-line selection is not a high-performance operation, and only static capacitance loads are connected.

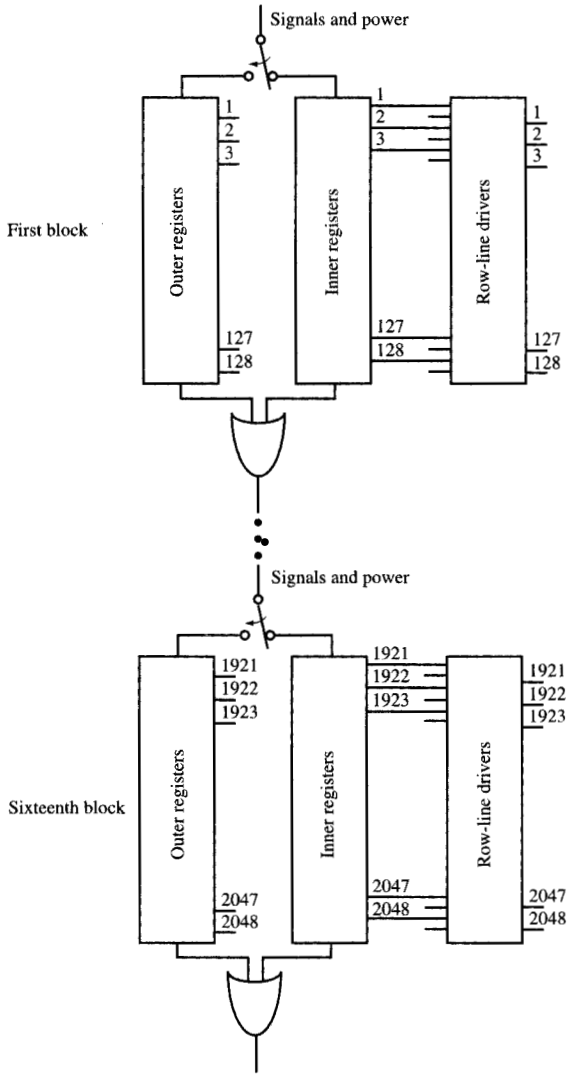

Figure 7

Row-driver data-selection redundancy concept. Signal and power are steered away from the inner group of registers to the outer group of registers in each of the 16 blocks of row-line drivers.

row would render the entire lower half of the array useless. A row-line driver failure, on the other hand, affects only part of one row line. Consequently, to reduce the number of transistors needed, redundancy was not used in the row-line driver circuits.

Conventional row drivers incorporate static logic and bidirectional selection capability to serve different applications. Dynamic shift registers were used, without the bidirectional function, reducing the number of transistors needed by a factor of 4. Since row-line precharging was used and performance requirements are modest, further simplifications were employed in the shift register. A single dynamic register (a transmission gate driving an inverter) was used per output instead of the usual two dynamic register stages. **Figure 6** shows two dynamic register stages, each having a positive output. An n-MOS transistor provides the transmission-gate function to each inverter input. To minimize power dissipation and ensure reliability, the row-selection circuitry inverter is connected to a 5-V power supply. To ensure that the inverter inputs pull up in voltage sufficiently and that the inverter is never in a partially conducting state, 6-V clock pulses are used. The input to the inverter of the first dynamic register serves as the positive data output signal for odd-row selection. The output from the second dynamic register inverter serves as the positive data output signal for even-row selection. The two dynamic registers use nonoverlapping clocks and function like an ordinary two-register dynamic-shift-register stage. The odd output is provided by the pass transistor without buffering, but the frequency is constant at about 75 Hz and the load capacitance is the static input capacitance of a row-line driver circuit; hence, the scheme works well.

The block row-selection redundancy concept is shown in **Figure 7**. The 2048 row-selection registers for each side of the array are subdivided into 16 blocks of two 128-selection-register groups each. A control signal to each block steers the row-selection signal, clocks, and power to either the inner or outer selection-register group. The power inputs to unselected groups must be grounded to guarantee that their outputs are low. To ensure this, all row-selection outputs are connected to a p diffusion in the n-well. The pn diodes guarantee that selection outputs are less than a threshold voltage when the power supply is low. In Figure 6, a p- to n-well diode is shown, for this purpose, on the output of the first dynamic register. The drain diffusion of the p-MOS in the inverter provides the diode for the even outputs.

Selection is accomplished by laser cutting after testing. **Figure 8** shows the specific circuit configuration used for inner or outer group selection. The p-MOS and n-MOS transistors at the upper right, with unbalanced channel sizes, are used for the group selection control. The inner row-selection group is the default. The drain connection of the p-MOS transistor is laser-deleted if the inner row-selection group is defective. The two inverters which follow separately provide power to either the inner or outer register groups, and provide signal steering input to the six AND gates. The 128th-register outputs of the two groups are OR-gated to pass the row-selection signal to the next block.

The circuit for the row-line drivers is shown in **Figure 9**. It must supply 10-V pulses to the gate lines with a fall time of about 100 ns. The slow fall time minimizes charge injection from the pixel transistor to the pixel capacitors

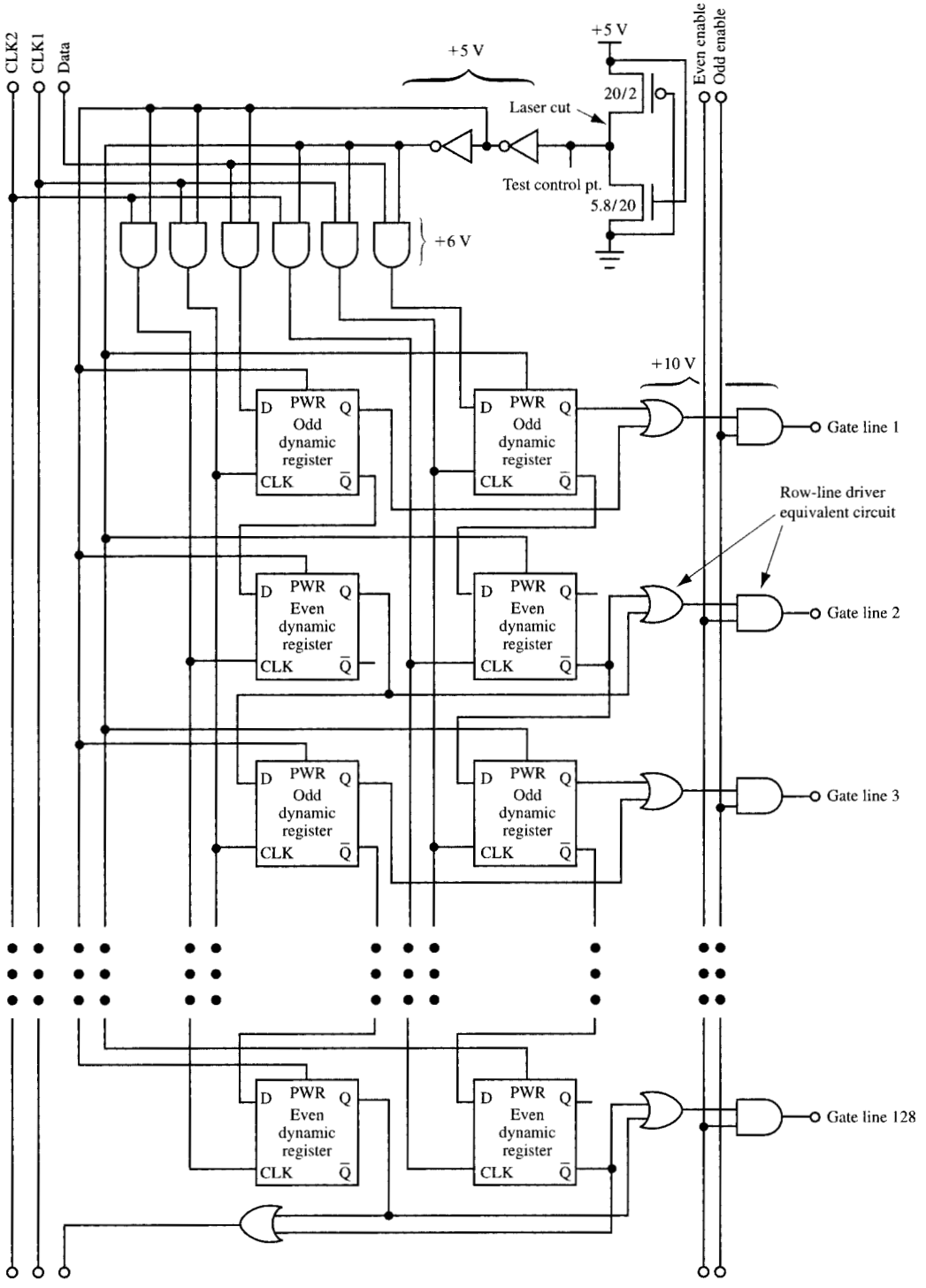

Figure 8

Detailed implementation of the row-line selection redundancy concept. Two inverters provide the data and clock signal steering information, and power for the inner and outer register groups. The data outputs for each row-line selection and group of selection registers are connected to inputs of OR gates for signal propagation.

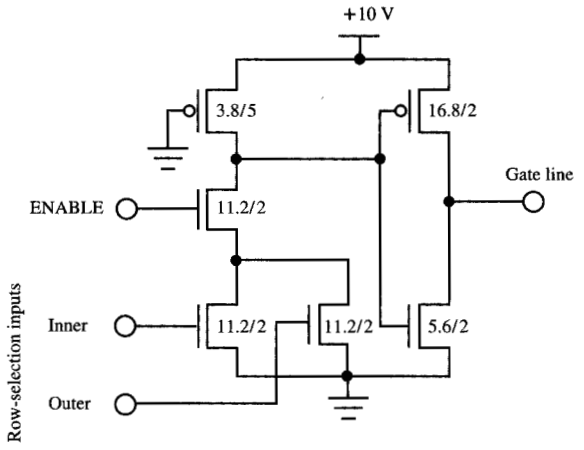

Figure 9

Circuit for a row-line driver. The level shift function is provided by the grounded p-MOS transistor. An ENABLE gate input transistor provides for precise timing of gate-line precharging and turnoff.

as the gate pulse falls by allowing charge injected before the transistors turn off to be conducted back to the data lines. With a 5-V row-selection signal, level shifting to 10 V is needed in the row driver. The grounded gate p-MOS transistor in the row driver with its source connected to 10-V functions as a passive load device used to provide the level-shift function. Power is dissipated only during row selection and is minimized by adjusting transistor width to length ratios to just satisfy the circuit fall time requirement. The overall function of the circuit is that the row selection inputs are OR-gated and AND-gated with an ENABLE signal. The ENABLE transistor provides flexibility in controlling precharging turn-on and turn-off timings for even and odd rows.

In order to lay out the row drivers on the 17-μm pitch, row-selection circuits and row-driver circuits were arranged four deep in the row direction. The four in-line drivers were designed to fit on a 4 $\times$ 17-μm or 68-μm vertical pitch. The horizontal length was greater than 1 mm. Since the metal-2 and metal-3 layers were dedicated to the array light-absorbing and mirror function, only metal-1 could be used for general-purpose metal wiring. The enabling signals, +6 V, +10 V, and ground were distributed using metal-1 from top to bottom of the entire row-driver circuitry, as shown in **Figure 10(a)**. The clock signals and +5 V for row selection are distributed in a similar manner; they are not connected at redundancy block boundaries, but are connected to the steering logic via polysilicon lines. Since metal-1 is used for vertical distribution of signal and power, the connections between the inner and outer row-selection registers to the row-line drivers are made with poly-1 and poly-2 layers, as conceptually depicted in **Figure 10(b)**. In most circuits, long polysilicon wiring would give an unacceptable timing performance, but a 100-ns variation in row-selection timing is avoided by using ENABLE signal timing.

Data drivers

The data lines of the active-matrix array each distribute signals from external data-driver circuits to the source electrodes of the pixel cell MOSFETs. The signals are sampled and stored on the capacitance of each cell, a row at a time, by means of pulses distributed via gate lines to the gate electrodes of the cell transistors in each row. The resulting cell voltages determine the luminance of the corresponding screen image pixels. The data-driver circuits which supply the data signals to the data lines also function as digital-to-analog converters.

For the prototype rear-projection display system [1] in which the chip was used, we elected to use external data-driver chips designed for use with direct-view active-matrix liquid crystal displays. Some of the motivating factors were the time required to develop specialized drivers, the possible impact on array yield of integrated data drivers, and the impact on the array process of making the second metal layer, used as a light shield, suitable for wiring in dense circuits.

It would have been impractical to provide a driver output for each of the 2048 column lines, since 11 or 12 chips would have been required, each to be attached to the edge of the silicon substrate. Instead, six driver chips were used with a 1:2 demultiplexer circuit to time-share each driver output among two data lines. The demultiplexing scheme is illustrated in **Figure 11**. The demultiplexer consists of one n-MOS device per data line. Adjacent pairs are fed by a common driver output, and the gates of all even devices and those of all odd devices are each driven with common timing. The independent driving of the gates of the odd and even demultiplexer transistors, the grouping of adjacent pairs of data lines, and a pairwise arrangement of the outputs of the row drivers are intended to permit operation of the array as a 1024 $\times$ 1024 matrix, with each pixel composed of four cells. This option has not been exercised.

During each display-line time, all six drivers are loaded simultaneously with data, and the analog output voltages are stored on the capacitance of the first of each pair of data lines by the demultiplexer. The drivers are loaded a second time, and the new analog output voltages are stored on the capacitance of the intervening data lines by the demultiplexer. The row-line pulse transfers the data-line voltages to the pixel capacitances of the row. Half of the data lines are driven from each edge, alternating by pairs of lines. As shown in **Figure 12**, the space required

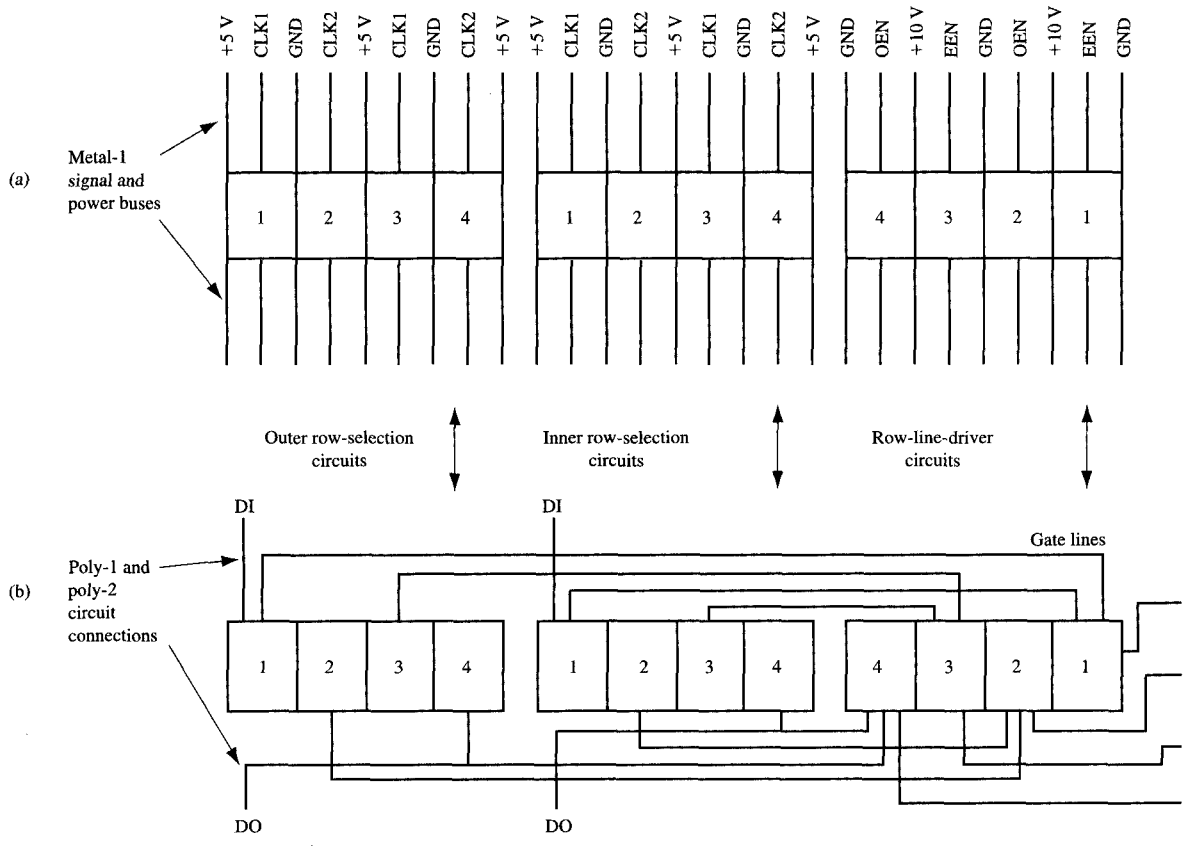

Figure 10

Conceptual illustration of the row-driver circuit layout. Four row-line-driver circuits are laid out on a 68-μm pitch with outputs on a 17-μm pitch. (a) Vertical signal and power lines are formed from the first level of metallization (metal-1). (b) The horizontal connections between row-line selection, driver circuits, and driver outputs are formed using the first and second levels of polysilicon (poly-1 and poly-2).

to attach the six drivers to three edges of the chip and that needed for wiring to the data lines were major contributors to the 64-mm-edge chip size needed for the prototype. A higher degree of multiplexing would reduce the number of drivers and decrease the chip size, but timing considerations, particularly the data-loading time of the driver chips, precluded its use for the 2048 × 2048-pixel array.

The pixel voltage must invert periodically relative to the counter-electrode voltage. For our reflective liquid crystal operating mode, a voltage range of ±3 V relative to the 3-V counter-electrode voltage is used. The data drivers are operated in a way that decodes the four input data bits into 32 gray-scale voltage levels, 16 above and 16 below the counter-electrode voltage. The gray-scale voltage levels are determined by reference-voltage inputs to the data drivers, derived from digital-to-analog converters. They are fully programmable. One such group of 16 levels is usually supplied to the upper row of drivers, while the other group is supplied to the lower row, reversing each frame at a 74-Hz rate. This inverts the pixel voltages by column-pairs and by frame.

Chip testing

Testing the 2048 × 2048-light-valve chip consists of checking the data lines for opens and shorts, the row-selection circuitry for data propagation, and the power-supply lines and light-absorber layer for shorts. Data lines are 2 μm wide and 35 mm long, making 2048 contacts to diffusions, which causes a major yield concern. A testing method with the data-line termination (p diffusion to n-well) diodes, shown in Figure 1, is used. To test for line continuity while measuring voltage, a current is injected into a data line with its diode termination at 0 V, while

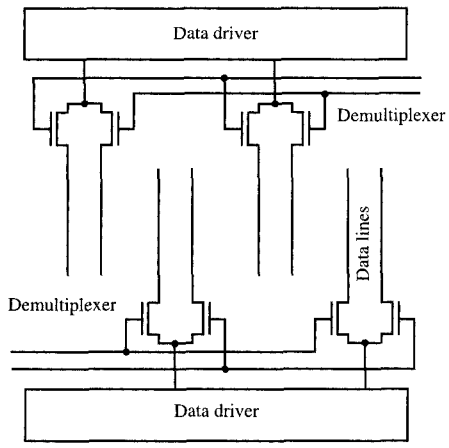

Figure 11

Schematic of data demultiplexing scheme.

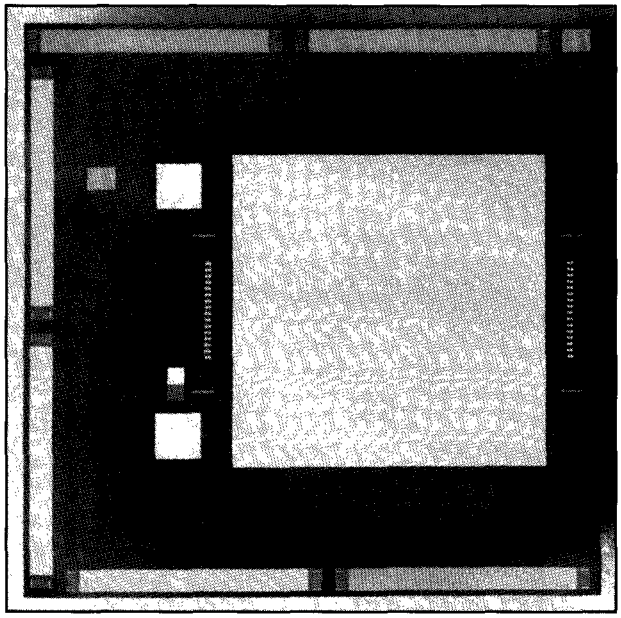

Figure 12

Photograph of 2048 × 2048-pixel light-valve array chip. The six external data-driver connections are on the top, left, and bottom edges of the chip. The two large squares left of the array are for connecting to the common electrode. The overall chip size is 64 mm by 64 mm.

adjacent data-line diodes are terminated at 10 V. If an appreciable voltage drop is measured (for example, greater than 1 V), the data line is regarded as being open. To test for shorts, a current is forced, while voltage is measured, into a data line with its termination diode at 10 V and adjacent data-line diodes terminated at 0 V. If a voltage less than 1 V is measured, the data line is regarded as being shorted. Four n-wells (two above and two below the array) provide four sets of diode terminators to the even and odd data lines. Four diode control lines (DTTE, DTTO, DTBE, DTBO) are needed, since the data lines are interleaved pairwise from top and bottom.

To avoid designing and building a custom test station, 52 2 × 16 test-pad structures were used. Forty-eight test structures are used for data-line testing and are located on the wafer outside the chip boundary. Since the data-driver tabs attach to pads that are located at the chip edge, access is readily available outside the chip boundary. The data-line test structures are removed upon dicing the chip. Using the data-line demultiplexers, 44 column lines are tested with each test structure. In addition to providing contacts for the data-line demultiplexer and diode termination inputs, the test structure has connections to ground, +10 V, and +5 V. The +10-V connection is used for input-protection diodes. To ensure that row-line drivers are not driving the pixel electrodes, the +5-V power-supply input for the row-selection drivers is grounded.

The row-selection circuitry consists of dynamic registers which, when clocked, operate as a shift register. Four 2 × 16 test structures positioned near the row-selection registers are used to test the 32 blocks of row-selection registers. The data-path continuity for all 32 groups of registers is tested by setting both even- and odd-register clocks high, toggling the input, and monitoring the output. If successful, a more complete test is run that monitors the output of each register group while using non-overlapping clocks and clocking a low-high-low data input pattern through the register group. The group test failures are noted. If an inner group test fails but the associated outer group test is satisfactory, the block's data path can be made functional by laser deletion of a selection input pull-up connection.

Short testing of power and light-absorbing-layer inputs consists of applying a voltage and monitoring current at one input while the other inputs are grounded. Occasional light-absorbing-layer shorts are observed. The light-absorbing layer covers virtually the entire chip. Openings in the light-absorbing layer are made only for mirror, input, and output pad connections. These shorts can sometimes be blown open electrically, making the chip useful.

A low-voltage SEM technique [12] is used to inspect for pixel mirror opens and shorts. If the energy of the primary electron beam is below a few keV, the good mirrors can become positively charged to a stable voltage. The

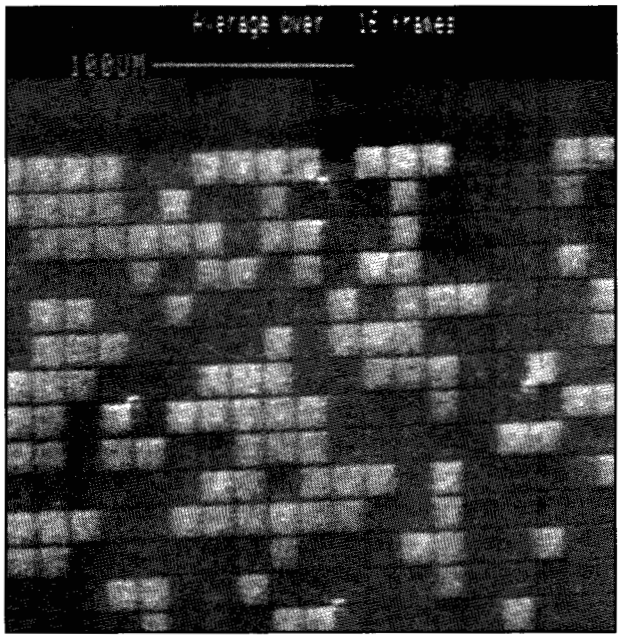

Figure 13

Low-voltage scanning electron micrograph of a portion of a defective chip containing normally connected (light) and unconnected (dark) mirrors.

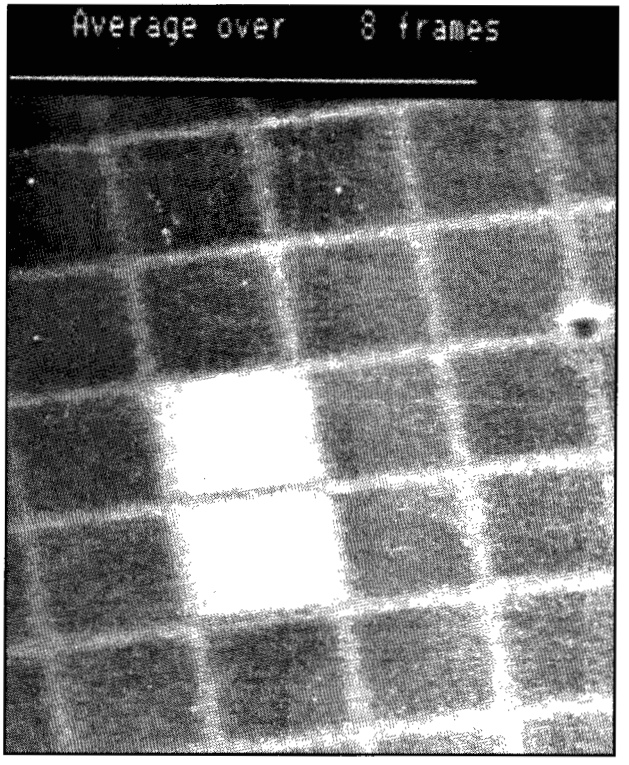

Figure 14

Low-voltage scanning electron micrograph showing a pair of (bright) pixels shorted to their chip. (The circular structure to the right is a spacer post.)

electron beam acts both as a current source to charge the mirrors and as a probe to measure the mirror voltages. A positively charged floating mirror attracts secondary electrons, leading to a darkened SEM image. Shorted mirrors give very bright SEM images. Illustratively, in **Figure 13**, a low-voltage scanning electron micrograph of a portion of a defective chip clearly shows both normally connected mirrors (light) and open mirrors (dark). Subsequent end-view high-voltage SEMs of the open pixels of the chip shown in Figure 13 showed poor contacts to its diffusions. **Figure 14** shows two pixels which were shorted to the silicon substrate.

Concluding remarks

This paper has focused on key design, fabrication, and testing aspects of an active-matrix 2048 × 2048-pixel-array chip, as part of the development of a reflective liquid crystal technology for projection displays. The chip contains fully integrated row drivers with a redundant row-selection feature and uses data-driver demultiplexing circuits with external data drivers, instead of fully integrated data drivers. Data-line-terminating diodes are used for testing for shorts and opens. A low-voltage SEM technique is used as an array diagnostic tool. As described elsewhere [1], the array chip has been incorporated into a prototype rear-projection color display system which produces high-quality images.

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