Thin-film-transistor process-characterization test structures

by E. G. Colgan
R. J. Polastre
M. Takeichi
R. L. Wisnieff

Electrical test structures provide a method of rapid, low-cost end-of-process metrology for both materials properties and specific process information. The results from electrical test structures for routine monitoring of key process parameters such as line width, edge-taper width, layer-to-layer alignment, and metal coverage are compared with those from traditional metrology methods. In all cases, the correlation coefficient R was near unity, $R^2 \geq 0.97$, demonstrating that electrical test structures have sufficient accuracy for process-control applications. For the structures used, the line width, edge-taper width, and layer-to-layer-alignment electrical measurements have uncertainties of less than 0.1 μm. The test structures are all compatible with typical thin-film-transistor (TFT) array processing.

Introduction

The active-matrix liquid crystal display (AMLCD) market is highly competitive and requires high yield and rapid product introduction at the lowest possible cost. Economic success depends on producing state-of-the-art displays in volume before market saturation and price erosion. The use of electrical-process-characterization test sites on product glass between displays can reduce the need for special process- or tool-characterization runs and limit the number of expensive inspection stations while providing the necessary information for statistical process control [1]. Electrical test sites can monitor important material properties such as sheet resistance, capacitance per unit area, and transistor performance characteristics, and can process specific information such as line width, edge-taper width, layer-to-layer alignment, and metal step coverage. In TFT array fabrication the total process time is typically two weeks or less, so the information lag is acceptable for maintaining a stable process testing only after array completion.

The microelectronics industry extensively uses electrical test sites for characterization of specific processing parameters [2] that may be unavailable or difficult to measure using traditional measurement techniques. Specific electrical test sites and examples of applications are as follows:

1. *Resistance measurements to determine line width*
   Resistance measurements have determined submicron line widths with total measurement uncertainties of less than 1 nm [3]. The simplest structure for an electrical line-width determination by measuring resistance consists of two conducting lines of different design

0018-8646/98/$5.00 © 1998 IBM

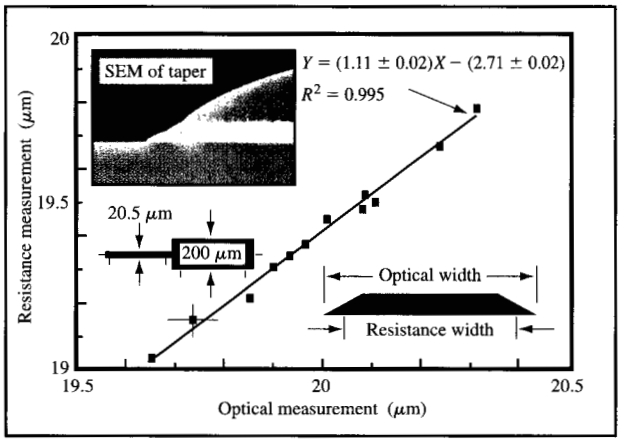

Figure 1

Plot of 300-nm MoW alloy gate-metal line width measured by resistance vs. line width measured optically. Representative error bars are indicated for one data point. The insert SEM cross section of the 300-nm MoW shows the taper width. The layer on top of the MoW is the photoresist used in patterning. A schematic of the test structure used is also shown.

widths but with the same design length [4]. A cross-bridge resistor structure (or variants thereof) achieves greater measurement accuracy [3].

2. *Resistance measurements to determine feature placement*
   Resistance measurements have determined feature placement with total measurement uncertainties less than 10 nm [3]. A variety of structures to determine feature placement are available [2, 3]. A typical method uses structures such as voltage-dividing potentiometers [3], where a first mask patterns a conductor and a second mask defines a contact to the patterned conductor. This process flow is compatible with microelectronic-wiring-level processing, where wiring planes and interlevel contacts alternate.
3. *Resistance measurements for metal step coverage over topography*
   The resistance of a wire crossing topography can increase if the metal step coverage is not adequate owing to the slope being too steep or the step too high. This is monitored electrically by comparing the resistance of serpentine lines on a flat surface to identical lines crossing topography formed by an underlying pattern [2].
4. *Capacitive measurements for interlevel dielectric thickness over patterned lines*
   The interlevel dielectric thickness over patterned features was characterized by measuring the capacitance between an array of lines and a conducting plate on top of the insulating layer, where an adjacent resistance test structure determined the line width and two-dimensional computer capacitance simulations corrected for the fringe field [5].

Thin-film-transistor (TFT) array fabrication processing for AMLCDs [6] has significantly different requirements than VLSI microelectronics. Fundamentally, the features are large for direct-view displays. Line widths of interest are in the 5–15-μm range, and patterning is frequently by wet etching. A key issue for gate metal is the taper width; the sloped edge ensures good insulator and metal coverage. When forming tapered edges by wet etching, the required over-etch can result in a large etch bias. For AMLCDs, multiple lithographic exposures are "butted" together to form a pattern for a single display, which creates additional alignment requirements. The resistive method described above for determining layer-to-layer alignment is not applicable to the key levels used to form TFTs in a typical process flow [6] (gate metal, IStop,[1] and data metal), and a novel capacitance method must be used instead. Excellent data metal coverage is necessary because a data line for a 12.1-in.-diagonal XGA display is about 10 μm wide and more than 18 cm long, and crosses 768 gate and storage capacitor lines.

This work does not describe test structures for monitoring material properties such as conductor sheet resistance, insulator capacitance per unit area, or test structures for characterizing transistor performance. Instead, the emphasis is on the use of electrical test structures to characterize the critical process steps that most directly affect performance and yield. The electrical measurement results are compared with measurements from standard metrology tools to determine the accuracy of the electrical measurement. The objective of using electrical testing is not to replace the standard metrology tools for initial process characterization and development, but to provide a rapid, low-cost method for tracking process variations for production support and yield management so that more expensive and difficult physical measurements are not needed. Additionally, the relative ease of the measurements promotes more frequent testing and a more complete characterization of the process. The next sections describe the structures and results for electrically measuring line width, edge-taper width, layer-to-layer alignment, and data-metal coverage for AMLCD fabrication. The structures were fabricated either on 381 × 381-mm glass at an AMLCD pilot line or on glass sizes up to 550 × 650 mm at a number of AMLCD production lines. Electrical measurements used standard semiconductor test equipment. Optical measurements of line width used a confocal laser scanning microscope [7, 8]

[1] The term *IStop* refers to the patterning of a silicon nitride layer to define an I-shaped channel region in a trilayer TFT process.

with a resolution of 0.25 μm and a specified critical dimension repeatability of 0.03 μm $\pm$ 3σ. The scan line was moved to ten different positions, and an average value was used. Computer capacitance modeling results used a suite of analysis tools developed at IBM Research for packaging applications; the capacitance tool is a modification of a previously reported method [9].

Electrical measurement of line width and taper width

The cross-sectional area, and hence the width, of a line can be measured using resistance. **Figure 1** shows a plot of the line width of a 300-nm MoW-alloy gate-metal line nominally 20.5 μm wide measured by resistance and optically. Intentional variations of the over-etch time during dry patterning of the MoW-alloy film created the observed distribution of line widths. The test site used was two resistors of different width in series [4], as shown schematically in Figure 1. The resistance measurement applied a current along the resistors and measured voltages at taps known distances apart. The width measured by resistance is fundamentally different from the physical width and is the effective conductivity path width along the length of the test resistor (Figure 1). The width measured optically is that of short segments of the resistor. Under ideal circumstances (i.e., where the line width is uniform, the line has vertical edges, uniform thickness, and uniform conductivity), the two line-width measurements should be equal. In fact, there is an excellent correlation (R^2 = 0.995), but the two measurements differ by about 0.6 μm. This is consistent with the observed taper width, as shown in the insert SEM cross section in Figure 1. The layer over the 300-nm MoW gate line is the photoresist mask used during patterning. If the taper has a linear slope and the conductivity does not change with thickness, the line width measured by resistance would be equal to the optical line width minus the width of the taper (Figure 1). The slope of the fit line is not equal to 1 because the taper width increases systematically as the width decreases, since an extended over-etch was used to form the narrower lines. The accuracy of resistive width measurements and structures which allow for higher-precision measurements are discussed in detail elsewhere [3]. The excellent correlation shown in Figure 1 demonstrates that the resistive width measurement is adequate for process monitoring for TFT fabrication because the dimensional changes of interest are larger than 0.1 μm.

A second means of electrically determining line width is to use a capacitor structure. A capacitive measurement can be used to determine the area of patterned features if a blanket calibration capacitor of known area is used and if a correction is made for the fringe field. The fringe-field term can be considered as a constant which increases

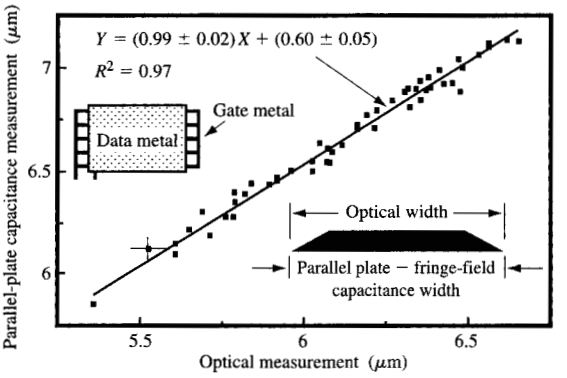

Figure 2

Plot of Mo/Al(X) gate-metal line width measured by capacitance vs. line width measured optically. Representative error bars are indicated for one data point. A schematic of the test structure used is also shown.

the capacitance over the value expected from a simple parallel-plate calculation. Plotted in **Figure 2** is the gate-metal width calculated from a capacitance measurement using a parallel-plate model versus the width measured optically. There is a very good correlation (R^2 = 0.97) between the two measurements with a near-unity slope. The test structure used consisted of nominally 10-μm-wide Mo/Al alloy, Al(X), gate-metal lines on 15-μm centers covered by a) gate insulator, b) intrinsic amorphous Si, and c) amorphous n^+ Si, located beneath the data metal, with a nominal overlap area of 115000 μm^2 (see schematic drawing of Figure 2). The capacitors are MOS (metal/oxide/semiconductor) devices because of the layers of amorphous n^+ and intrinsic Si under the data metal from the process flow used [6]; an appropriate bias was applied during the capacitance measurements so that the amorphous Si layer was in accumulation. The difference in width of 0.60 μm between the two measurements corresponds to the fringe-field capacitance. Two-dimensional computer calculations of the capacitance, which included the fringe fields, indicated that the fringe-field contribution is largely independent of the width (for widths from 4 to 12 μm with 15-μm center-to-center spacing), but does change with the dielectric layer thickness. For the results shown, the standard deviation in value of the reference capacitors was less than 2%. This suggests that the capacitance width for the specific structure and dielectric layer used can be calculated by using the parallel-plate model and then subtracting 0.60 μm to correct for the fringe-field term. If the blanket reference capacitor is placed close by the patterned capacitor, the absolute accuracy of the measurement is

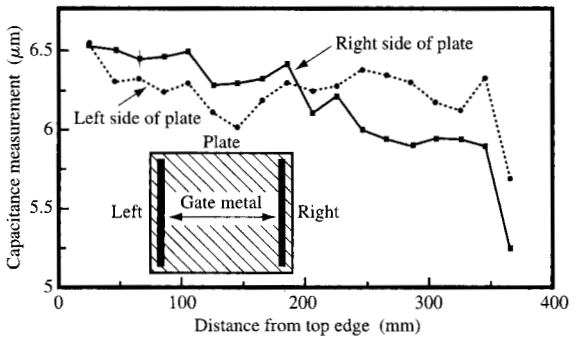

Figure 3

Plot of Mo/Al(X) gate-metal line width measured by capacitance as a function of position on the plate. A representative error bar is indicated for one data point.

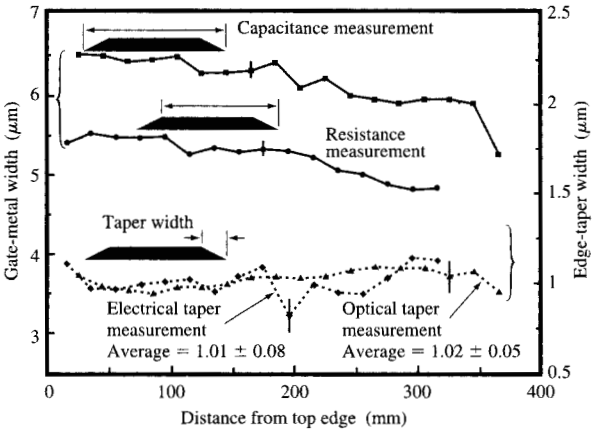

Figure 4

Plot of Mo/Al(X) gate-metal line width measured by capacitance and resistance, edge-taper width determined by subtracting the resistive line width from the capacitive line width, and edge-taper width measured optically as a function of position on the plate. Schematic drawings show the metal line widths corresponding to the measured values. Representative error bars are indicated for four data points.

probably limited by the uncertainty in the fringe-field correction term, which has a standard deviation of ± 0.05 μm for the results in Figure 2. Note that the capacitance width is proportional to the area and hence measures the bottom width of the line (see schematic of Figure 2).

The excellent correlations between both the resistive and capacitive width measurements and optical width measurements suggest that these measurements can be used instead of optical measurements for rapid, low-cost metrology. The following two figures show examples of using capacitive width measurements to measure etching uniformity as a function of location on a plate and of using the combination of resistive and capacitive width measurements to electrically measure the taper width. Plotted in **Figure 3** is the width measured by capacitance for Mo/Al(X) gate metal as a function of location on the plate. The test sites were the same as those for Figure 2 and were located in two rows along each side of the plate. The Mo/Al(X) gate metal was immersion-etched [6] to form tapered edges. This process results in an etch bias of about 3.5 μm and forms a taper of about 1 μm on each side. The results in Figure 3 show a gradual systematic decrease in width as the distance from the top edge is increased until near the bottom of the plate, where the width decreases sharply. The total variation in width is about 1.2 μm, which can have important implications because the TFT gate width is a critical parameter in display performance. This type of information on line width as a function of location can be used to monitor and improve the process uniformity, to determine what is an acceptable design margin, or to determine what area of the plate can be used. As mentioned previously, another key process parameter is the taper width. The taper width can be measured electrically by using a combination of resistance-width and capacitance-width measurements (**Figure 4**). The capacitance-width results from Figure 3 for the right side of the plate have been reproduced in Figure 4 and the results from a Mo/Al(X) gate-metal resistance-width test site added (left-hand y-axis). For this resistance-width test site, the design width of the narrow resistor was 6 μm, so for direct comparison with the capacitance-width measurements (design width of 10 μm), 4 μm was added to the measured values. The resistance test site failed for some of the smallest widths because the taper regions reached the center of the lines and no region remained of the original metal thickness at distances greater than 300 mm from the top edge of the glass plate (Figure 4). As described in Figures 1 and 2, the resistance width is equal to the bottom of the metal line width minus one taper width, and the capacitance width (after correcting for the fringe-field term) is equal to the bottom-line width, so subtracting the two electrical width values gives the taper width for one side, which is plotted in Figure 4 (right-hand y-axis). The taper width was also measured optically by measuring the Al bottom width and the top width (width of the Mo cap), subtracting the two values, and dividing by 2. The optically measured taper width is also plotted as a function of location in Figure 4. The average taper-width values are virtually identical—1.02 ± 0.05 μm for the optical measurement and 1.01 ± 0.08 μm for the electrical measurement. The excellent

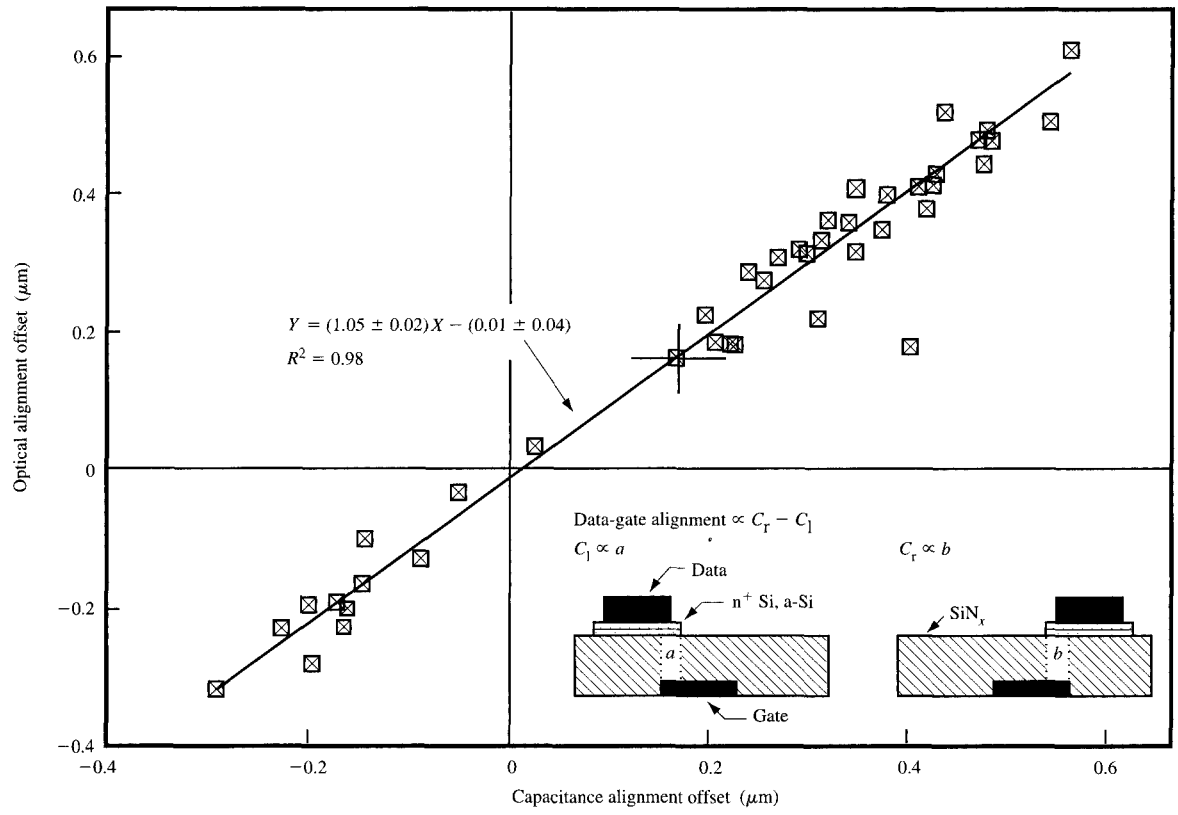

Figure 5

Plot of left-to-right data-metal-to-gate-metal alignment measured optically vs. alignment measured by capacitance. A schematic illustrating the designed overlap, i.e., $a = b$, is shown in the lower right; misalignment, e.g., of the data line in the left direction decreases a and increases b. The capacitance value is calculated using a parallel-plate model. Representative error bars are indicated for one data point.

agreement between the two taper-width measurement methods demonstrates that the taper width can be monitored by rapid, low-cost electrical tests. Note that the taper width is nearly uniform across the plate, even though the gate-metal width varies by 1.2 μm. The taper width is an important parameter, because inadequate gate-metal taper can result in defects in the gate insulator coverage, leading to shorts, or poor step coverage by the data metal, resulting in high resistance for the data lines.

Electrical measurement of lithographic alignment

With a trilayer-type TFT, the critical layer-to-layer alignment is between the gate, IStop, and data levels. A combination of masking and back-exposure of the patterned gate metal through the glass plate is frequently used for self-alignment of the IStop level to the gate level [10]. Because of the TFT process flow, the typical resistive alignment monitoring structures [3] are not suitable. A novel capacitive alignment test site was used instead, consisting of an array of lines which are designed to partially overlap with one of the structures; the overlap a is to the left, and, for a second paired structure, the overlap b is to the right (see **Figure 5**, schematic at lower right). The difference in capacitance between the right and left structures, $C_r - C_l$, is proportional to the right-to-left alignment offset. For one level misaligned left with respect to the other, the value of one capacitor decreases and the value of the second paired capacitor increases. The nominal design width of the lines was 10 μm, with an overlap of 6 μm and a space between lines on the same level of 30 μm. Two-dimensional computer calculations of the capacitance, including the fringe fields, were performed as a function of overlap distance and dielectric thickness. It was found that for a given dielectric thickness, and overlaps between 2 and 8 μm, the fringe-field capacitance was nearly a constant and changed only slightly. Since the alignment offset is proportional to the

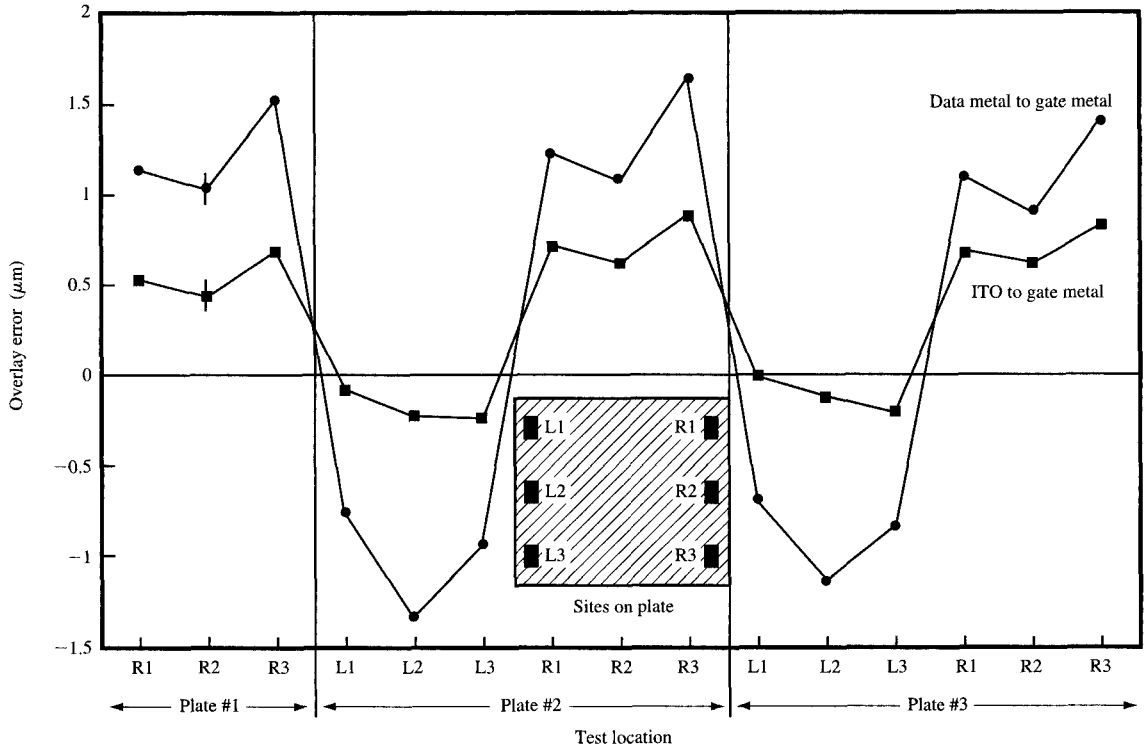

Figure 6

Plot of glass plate top-to-bottom alignment measured by capacitance as a function of test-site location and plate number. There is a systematic left-to-right variation for both the data-to-gate-metal and ITO-to-gate-metal alignments. The test-site locations are indicated schematically. Representative error bars are indicated for two data points.

difference in capacitance between the two paired structures, and the difference in overlap is generally less than 2 μm, the fringe-field terms cancel, and the alignment can be calculated using the parallel-plate approximation. Figure 5 shows the results of optical and capacitance alignment measurements for a right–left pair of data-to-gate-metal alignment capacitors. The correlation was excellent, R^2 = 0.98, with only a small offset from zero and a near-unity slope. The nominal overlap area was 54000 μm^2, and the overlap calculated from the average capacitance was about 3 μm (design overlap minus lithographic and etch bias for both gate and data metal). The electrical alignment measurement accuracy demonstrated in Figure 5 exceeds the accuracy needed for TFT process monitoring. A similar set of test structures can determine the IStop-to-gate-metal alignment, where the data-metal lines are each replaced by pairs of closely spaced IStop lines with a data-metal line centered on the gap between the IStop lines and partially covering the IStop lines. When a bias is applied to the gate lines, a conducting channel is formed in the amorphous Si layer under the IStop lines located above the gate lines to which the amorphous n^+ Si and data metal make electrical contact.

The next figure gives an example of using capacitive alignment measurements as a function of location on a glass plate to examine systematic overlay errors. Plotted in **Figure 6** is the top–bottom alignment error for indium–tin oxide (ITO) to gate metal and for data metal to gate metal for the indicated locations on three different plates. Of the six sites, three (L1–L3) were on the left side of the plate and three (R1–R3) were on the right side of the plate. These plates were processed with a different process sequence, in which the ITO is on top of the gate insulator and is patterned before the data metal. The results show a systematic variation between the left and right sides of the plates where the ITO or data metal is shifted down on the left side of the plate and shifted up on the right side of the plate relative to the gate metal. The total magnitude of the shift reaches about 3 μm for the data metal and about 1 μm for the ITO relative to the gate metal. These shifts can have a significant impact on device performance and perhaps indicate a plate rotation error.

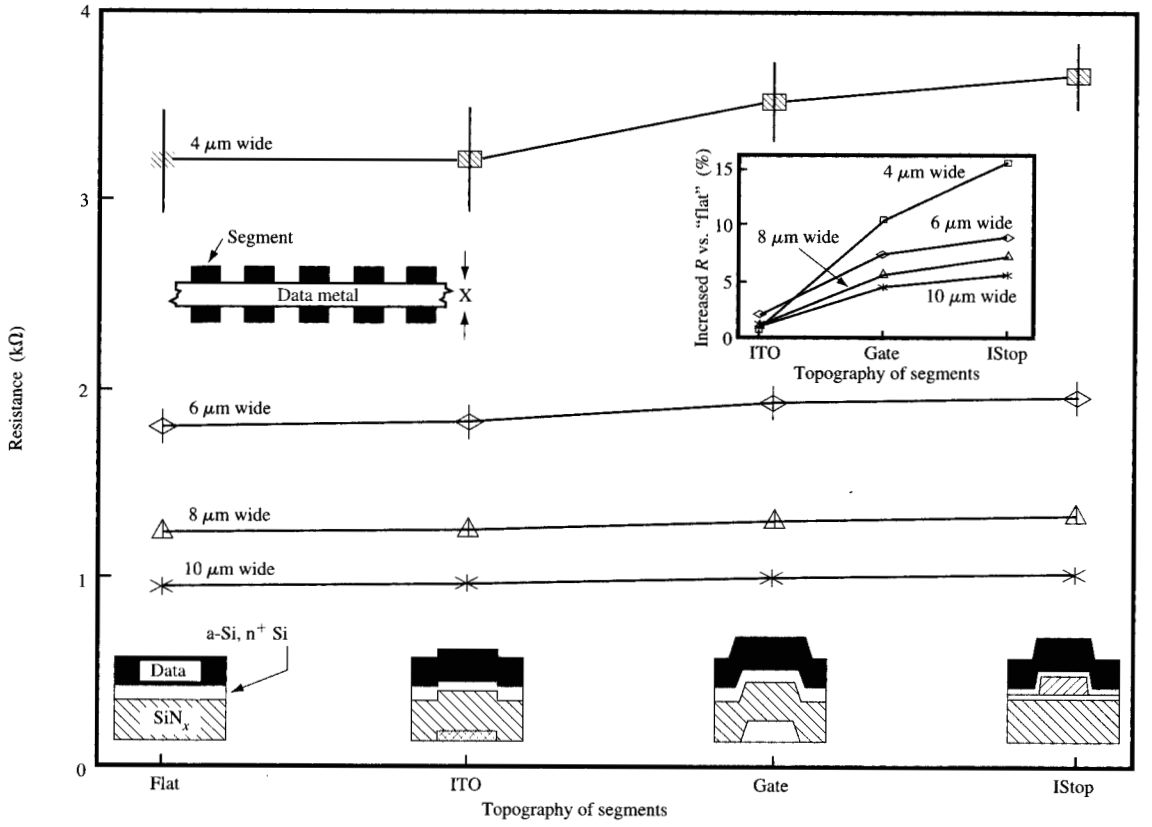

Figure 7

Plot of average resistance of a 40-mm-long data-metal line as a function of line width and underlying topography with a schematic of the test structure used shown at the top left. The underlying topography consists of patterned segments, as shown in schematics at the bottom of the figure. The vertical lines indicate the standard deviation of the measured values. The insert plot shows the percentage increase in resistance relative to the flat no-topography case as a function of line width and underlying topography.

Electrical measurement of metal coverage

When metal is deposited by sputtering over an edge or step, the coating is not completely conformal. If the step is tapered, the metal thickness is reduced only slightly, but with a vertical or near-vertical step of sufficient height, an open can result. **Figure 7** shows data-metal coverage, as monitored by resistance, as a function of underlying structure and nominal line width for 40-mm-long lines crossing 2000 patterned segments. The structure used is shown schematically, and drawings along the bottom of Figure 7 illustrate the structure of the segments. **Figures 8(a)–(c)** are oblique-angle SEM micrographs showing nominally 6-μm-wide data-metal lines crossing segments of different material. The segments were nominally 10 μm wide along the length of the wire. For the process used [6], a conformal amorphous n^+ Si layer deposited by plasma-enhanced chemical vapor deposition under the data metal reduces the resistance on steps. Plotted in an insert on Figure 7 is the percentage increase in resistance compared to the "flat" case for the different data-metal line widths as a function of underlying structure. In all cases, the increase in resistance when crossing the topography is small (less than 10%) for nominal line widths of 6–10 μm. The largest increase in resistance is for the IStop segments, which is consistent with the SEM micrographs, which show that the IStop step height is the largest and the taper angle is the steepest. The approximate step heights are 50 nm for ITO, 250 nm for the Mo/Al(X) gate metal, and 400 nm for the IStop. **Figure 8(d)** shows the IStop profile when a different set of process conditions is used, resulting in a near-vertical step. In this case, the resistance increased between 13% and 16% relative to the flat structure for the 6–10-μm-wide lines. For the more tapered IStop profile shown in

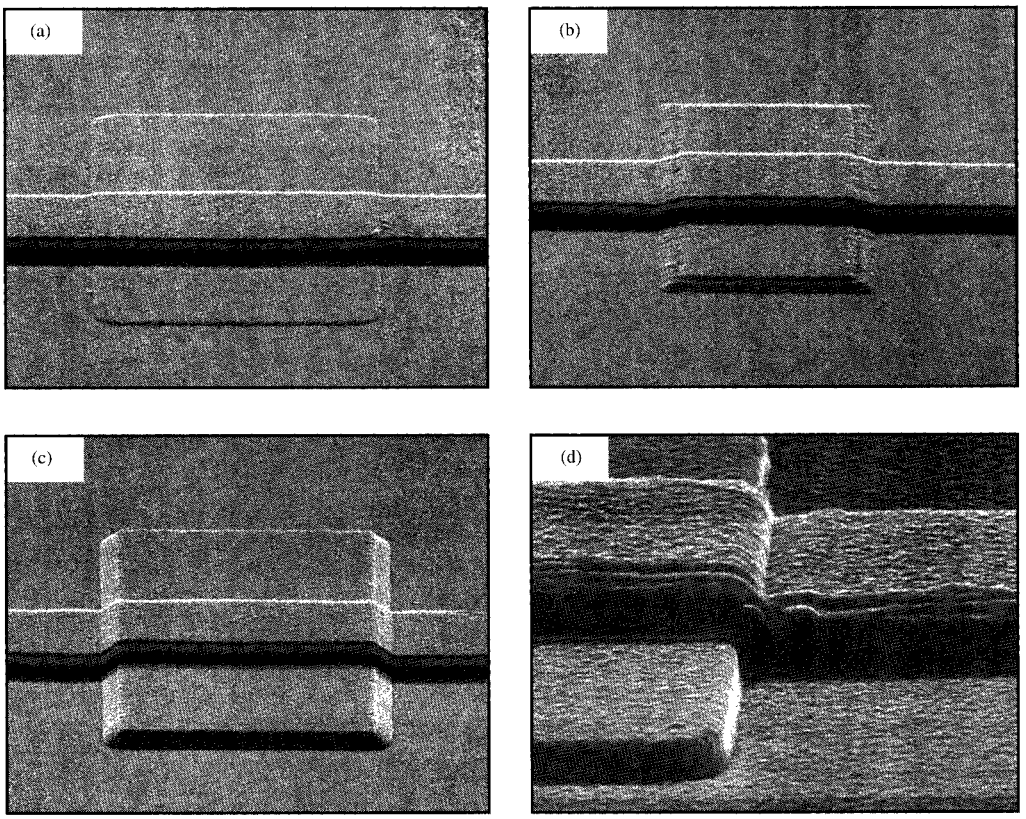

Figure 8

Oblique-angle scanning electron micrographs of a 6-μm-wide data-metal line crossing (a) ITO, (b) gate metal, and (c) IStop corresponding to the results in Figure 7. An 8-μm-wide data-metal line crossing IStop formed using a different process which resulted in a near-vertical edge is shown in (d). Note that all of the features are covered by a passivation SiN_x layer after the data-metal lines are patterned.

Figure 8(c), the corresponding increase was between 6% and 9% for the 6–10-μm-wide lines (Figure 7). Also, with the near-vertical IStop profile, the distribution of resistance values was much wider; typical standard deviations were 12–15% versus 3–4% with the tapered IStop. With a near-vertical IStop step, the increased data-line resistance and variation can significantly affect display performance. In the process flow used [6], an IStop segment is added where the data line crosses over the gate line to reduce capacitive coupling.

Summary

We have demonstrated the use of electrical test structures for monitoring key TFT array process parameters such as line width, gate-metal-taper width, layer-to-layer alignment, and data-metal step coverage. A novel capacitance method involving layer-to-layer alignment measurements was used. Comparisons were made between electrical test structures and traditional metrology methods, and in all cases the correlation was very good. For the structures used, the line width, edge-taper width, and layer-to-layer-alignment electrical measurements have uncertainties of less than 0.1 μm, which is sufficiently accurate for TFT fabrication process-control applications. In combination with test structures for monitoring material properties such as resistance and capacitance, and transistor performance, electrical testing provides a method of rapid, low-cost end-of-process metrology for statistical process control and design optimization. The test structures used are all compatible with typical thin-film-transistor array processing.

Acknowledgments

We are indebted to B. Rubin for assistance with the capacitance modeling work, J. Wilson, Y. Fujii, and K. Hayashi for test-site layout, R. Horton for test-stand

modifications, P. Fryer, E. Galligan, W. Graham, H. Ifill, K. Latzko, S. Libertini, and M. Rothwell for TFT array processing, and R. John, K. Araki, and M. Teruya for test-site recovery after glass cutting. We would also like to thank H. Kitahara, K. Schleupen, S. Wright, P. Alt, and F. Libsch for useful discussions.

References

1. D. J. Bartelink, "Statistical Metrology: At the Root of Manufacturing Control," *J. Vac. Sci. Technol. B* **12,** No. 4, 2785–2794 (1994).
2. M. G. Buehler, "Microelectronic Test Chips for VLSI Electronics," Chapter 9 in *VLSI Electronics: Microstructure Science*, Vol. 6, N. G. Einspruch and G. B. Larrabee, Eds., Academic Press, Inc., New York, 1983.
3. L. W. Linholm, R. A. Allen, and M. W. Cresswell, "Microelectronic Test Structures for Feature Placement and Electrical Line Width Metrology," pp. 91–118 in *Handbook of Critical Dimension Metrology and Process Control*, K. M. Monahan, Ed., *Critical Reviews of Optical Science and Technology*, Vol. CR52, SPIE Optical Engineering Press, Bellingham, WA, 1994.
4. D. R. Thomas, "Use of Two Resistors of Different Width to Measure Process Bias," U.S. Patent 3,974,433, August 1976.
5. D. Boning, T. Maung, J. Chung, K.-J. Chang, S.-Y. Oh, and D. Bartelink, "Statistical Metrology of Interlevel Dielectric Thickness Variations," *Microelectronics Manufacturability, Yield, and Reliability, Proc. SPIE* **2334,** 316–327 (1994).
6. E. G. Colgan, P. M. Alt, R. L. Wisnieff, P. M. Fryer, E. A. Galligan, W. S. Graham, P. F. Greier, R. R. Horton, H. Ifill, L. C. Jenkins, R. A. John, R. I. Kaufman, Y. Kuo, A. P. Lanzetta, K. F. Latzko, F. R. Libsch, S.-C. A. Lien, S. E. Millman, R. W. Nywening, R. J. Polastre, C. G. Powell, R. A. Rand, J. J. Ritsko, M. B. Rothwell, J. L. Staples, K. W. Warren, J. S. Wilson and S. L. Wright, "A 10.5-in.-Diagonal SXGA Active-Matrix Display," *IBM J. Res. Develop.* **42,** 427–444 (1998, this issue).
7. D. Awamura, T. Ode, and M. Yonezawa, "Color Laser Microscope," *Proc. SPIE* **765,** 53–60 (1987).
8. D. Awamura, T. Ode, and M. Yonezawa, "Scanning Color Laser Microscope," *Proc. SPIE* **921,** 388–394 (1988).
9. B. J. Rubin and S. Daijavad, "Radiation and Scattering from Structures Involving Finite-Size Dielectric Regions," *IEEE Trans. Antennas Propagat.* **1 (AP-38),** 1863–1873 (1990).
10. S. Kawai, N. Takagi, T. Kodama, K. Asama, and S. Yanagisawa, "Amorphous Silicon Thin-Film Transistor for Liquid Crystal Display Panel," *Digest of Technical Papers*, Society for Information Display International Symposium, 1982, pp. 42–43.

Received March 17, 1997; accepted for publication February 12, 1998

Evan G. Colgan *IBM Research Division, Thomas J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598 (ecolgan@us.ibm.com).* Dr. Colgan is a Research Staff Member at the IBM Thomas J. Watson Research Center in the Flat Panel Display Technologies area. He previously managed the Thin-Film Transistor Processing Department. Dr. Colgan joined the Research Division in 1995; he was previously an Advisory Engineer at the Semiconductor Research and Development Center in Hopewell Junction, New York. While at the Development Center, since joining IBM in 1987, he worked on aspects of metal silicide formation, selective chemical vapor deposition of tungsten, diffusion barriers, Al(Cu) microstructure evolution, and integration of both Cu- and Al-based metallizations for integrated circuits. Dr. Colgan received his B.S. degree in applied physics from the California Institute of Technology in 1982 and his Ph.D. in materials science and engineering from Cornell University in 1987. His thesis work involved the formation of aluminides from thin-film couples. Dr. Colgan has published more than seventy papers and has been issued eleven patents; he is a member of the MRS, IEEE, APS, Bohmische Physical Society, and Sigma Xi.

Robert J. Polastre *IBM Research Division, Thomas J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598 (polastr@us.ibm.com).* Mr. Polastre is a Staff Engineer working in the Advanced Array Processing and Test group. He joined the IBM Research Division in 1983 with an associate degree in electronic technology and a bachelor's degree from LaSalle University. Mr. Polastre received an IBM Outstanding Technical Achievement Award in 1990 and an IBM Corporate Award in 1993 for his work on a dynamic array tester. He is the author or co-author of several papers on TFT/flat-panel testing and is a co-inventor of patents in this area. Mr. Polastre is a member of the IEEE and an officer of the Mid-Atlantic Chapter of the Society for Information Display.

Masatomo Takeichi *IBM Japan Ltd., Display Technology, Display Business Unit, 800, Ichimiyake, Yasu-cho, Yasu-gun, Shiga-ken 520-23, Japan (y00898@jp.ibm.com, takeichi@yamato.ibm.co.jp).* Mr. Takeichi is a Staff Engineer in the LCD Operation Department of the Display Business Unit. He received a B.S. degree in applied chemistry from Tokushima University in 1980. He joined IBM in 1988, and, as a manufacturing engineer, has contributed to the installation of several plasma etching processes in the mass production of an 8-in. silicon wafer. Mr. Takeichi is currently working on AMLCD manufacturing engineering.

Robert L. Wisnieff *IBM Research Division, Thomas J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598 (wisnieff@us.ibm.com).* Dr. Wisnieff graduated from Tufts University in 1980 with a B.S.M.E. and from Yale University in 1986 with a Ph.D. in applied physics. He joined IBM in 1986, working in the research group developing amorphous-silicon-based active-matrix liquid crystal displays. He earned a Corporate Award for the development of array testing of thin-film transistors. Dr. Wisnieff is currently the manager of IBM's Advanced Display

Technology Laboratory. He holds four patents and has authored or co-authored 14 publications, and has given invited talks and seminars on active-matrix technology. Dr. Wisnieff has held the offices of Secretary, Treasurer, Vice Chairman, and Chairman of the SID Mid-Atlantic chapter. He has served on and chaired the SID Symposium Active-Matrix Subcommittee and has been the Seminar and Program Chair of the SID Symposium. He is a member of the ACM, IEEE, and SID.