Driving method for gate-delay compensation of TFT/LCD

by K. Kusafuka
H. Shimizu
S. Kimura

Gate delay is one of the biggest limiting factors for large-screen-size, high-resolution thin-film transistor liquid crystal display (TFT/LCD) design. To solve this problem, we have developed a new driving method which can achieve high image quality and reliability and reduce the power consumption with conventional processes, even if gate-line resistance and load capacitance are increased. The new method uses gate-pulse waveforms that separate the functions of feedthrough compensation, with pulse edge timing that greatly reduces errors due to gate delay.

Introduction

In recent years, attempts [1–7] have been made to greatly improve the display quality of active-matrix liquid crystal display devices, and many techniques have been proposed to solve such problems as flicker on the screen and image sticking (in which a fixed image remains immediately after its display as if it had been burnt in). Both flicker and image sticking, which cause the quality of the display to deteriorate, are caused by a dc voltage component that occurs unavoidably in some display pixels owing to anisotropy in the dielectric constant of the liquid crystal. On the other hand, techniques [8, 9] have been proposed for reducing the power consumption of active-matrix liquid crystal display devices to allow even a battery to drive them for a long time, so that they can be applied to a variety of portable apparatus such as notebook computers. A major limiting factor in the accomplishment of both objectives has been gate delay, which is exacerbated in conventional driving schemes by the larger loads of bigger and higher-density displays as well as by reductions in power. In this paper we describe a new driving method that compensates for gate delay in thin-film-transistor liquid crystal displays (TFT/LCDs).

C_S-on-gate structure

In a TFT/LCD, separate storage capacitors (C_S) are required because the liquid crystal pixel capacitance is small. These capacitors are of a particular type called C_S-on-gate, in which a pixel electrode is connected to the gate line immediately preceding the gate line that is connected to the pixel concerned, and a storage capacitor on a separate wiring line (storage capacitance line) is formed. **Figure 1** shows an equivalent circuit of the C_S-on-gate type. The drain electrodes of the TFTs are connected to data lines D1–D4, respectively, coming from the data-line-driving circuit. The gate electrodes of the TFTs are connected to gate lines G1–G3, respectively, which are connected to a gate-line-driving circuit. The source electrodes of the TFTs are connected to respective display electrodes, and a liquid crystal that is sealed between the display electrodes and a common electrode provided on an opposed substrate constitutes the liquid crystal capacitance C_{LC}. Each pixel electrode is also connected to the gate line of the immediately preceding scan line to constitute an auxiliary capacitor C_S. A parasitic capacitance C_{GS} exists between the gate and source of the TFT. In an

0018-8646/98/$5.00 © 1998 IBM

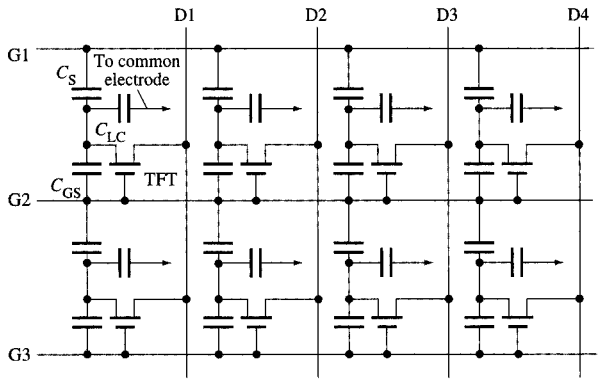

Figure 1

Equivalent circuit for a C_S-on-gate-type LCD.

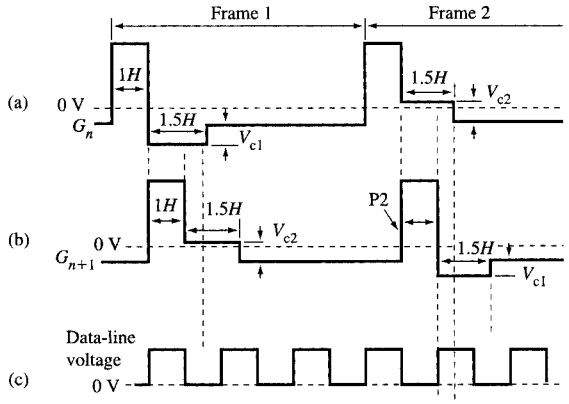

Figure 2

Row-inversion driving waveforms for the conventional driving method.

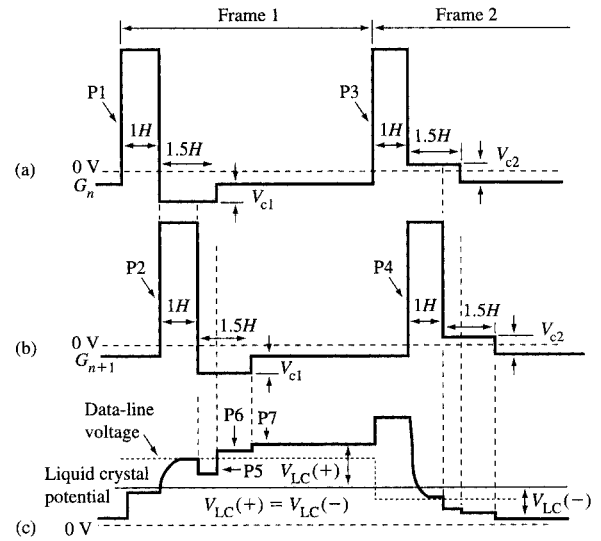

Figure 3

Frame-inversion driving waveforms for conventional driving method 1.

active-matrix LCD having the above configuration, it is increasingly required that the display screen have higher resolution and wider screen size. In association with these requirements, various technical problems have arisen. For example, Nanno et al. have reported methods [9] that can reduce the degree of flicker and the image-sticking phenomenon in the above type of LCD by compensating for a dc component that occurs unavoidably because of anisotropy in the liquid crystal, while reducing the power consumption. However, they did not consider the fact that miniaturization of the gate lines, an increase in the number of wiring lines, and an increase in display wiring length, which are associated with improved resolution of the display screen and an increased number of display pixels, will increase the resistance of the gate lines and the load capacitance, causing gate delay. The gate delay in turn causes a variation in the gradations and levels of any dc components in the horizontal direction of the display screen. Gate delay has been considered an unavoidable problem in achieving the improved resolution and high aperture ratio that are needed to increase the quality of liquid crystal displays. For example, gate delay may be reduced by making the gate lines wider, but this decreases the aperture ratio of the display pixels. In this case, to obtain sufficient display brightness, greater backlight intensity is required, and this increases power consumption.

Conventional driving method 1

With reference to Figures 2–6, we describe the conventional liquid crystal driving method [9] in a more specific manner. The following explanation assumes a normally white-type LCD, in which display brightness decreases as the liquid crystal application voltage is increased. Row-inversion drive waveforms (**Figure 2**) and frame-inversion drive waveforms (**Figure 3**) are adapted to compensate for both feedthrough voltage and effective value. Effective-value compensation means increasing the liquid crystal application voltage by adjusting the voltage applied to C_S (constituting the gate line and the pixel electrode) when the voltage supplied from the data line is relatively low. Effective-value compensation allows the

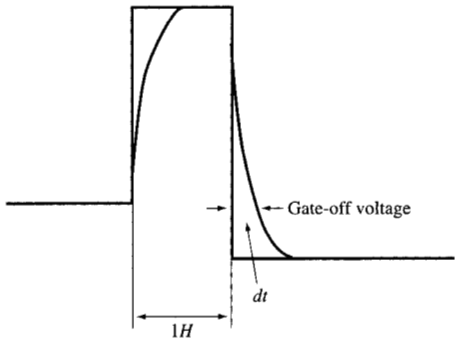

Figure 4

Gate delay.

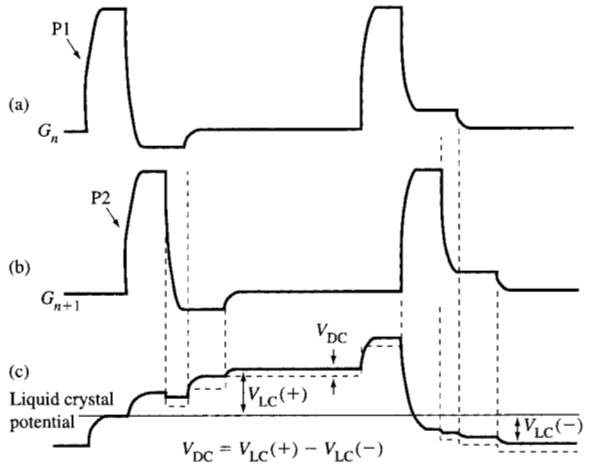

Figure 5

Waveforms for conventional driving method 1 at the terminal side.

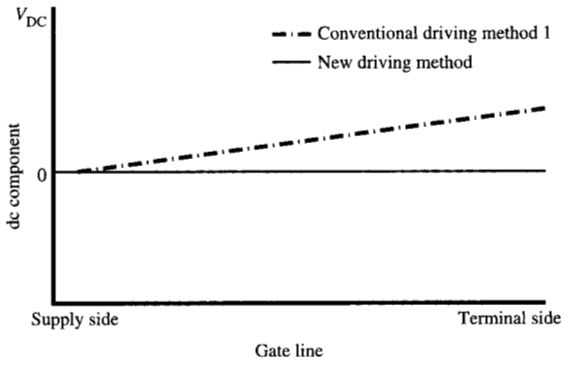

Figure 6

V_{DC} from supply side to terminal side.

liquid crystal to switch to the dark state with low data-line voltage. If effective-value compensation is not adopted, the voltage supplied from the data line must be larger. In that case, the power supply for the source-driver integrated circuit must be larger, and the source-driver circuit itself must have a wider voltage range. Without effective-value compensation, the power supply for the source-driver circuit requires $2(V + dV)$ when the voltage applied to C_{LC} is larger by dV than the voltage V supplied from the data line. Therefore, the power consumption of the source driver with effective-value compensation is smaller than that without compensation by $2dVI$, where I is the current applied to the data-line driver circuit from the power supply.

Figure 3 shows a case in which frame-inversion driving is performed on a C_S-on-gate LCD. Parts (a) and (b) show input waveforms, and part (c) a liquid crystal drive waveform on the side close to the gate driver, where no gate-line delay occurs. When gate pulse P2 is input to gate line G_{n+1}, the TFT connected to this gate line is turned on, so that a voltage is applied to the liquid crystal as shown in Figure 3(c). When the TFT is turned off, the feedthrough phenomenon at the falling edge of gate pulse P2 causes the charged voltage to the liquid crystal to decrease by a feedthrough voltage component P5, as shown in Figure 3(c). Thereafter, feedthrough voltage compensation and effective-value compensation P6 are effected by causing a previous gate line G_n to have a potential V_{c1} and applying this voltage to C_S. Further, final effective-value compensation P7 is effected by supplying a signal of V_{c1} to the gate line G_{n+1} after a lapse of about $1H$, where H is the width of a primary gate-line pulse. As a result, the liquid crystal potential is set at $V_{LC}(+)$ during frame 1. Next, to drive the liquid crystal in frame 2, feedthrough voltage compensation and effective-value compensation are performed by a process similar to that in frame 1 at a voltage level V_{c2}, so that the liquid crystal potential becomes $V_{LC}(-)$. As a result, a condition $V_{LC}(+) = V_{LC}(-)$ is established which enables the liquid crystal display to be free of a dc component and changes the effective value of the data-line voltage. However, when gate delay occurs, the gate pulse assumes waveform distortion (as shown, for instance, in **Figure 4**) at a position close to the gate-line terminal, and gate-off timing is therefore delayed by dt from $1H$. As a result, as shown in **Figure 5**, the feedthrough voltage decreases because, owing to the longer gate-on time, a source–drain

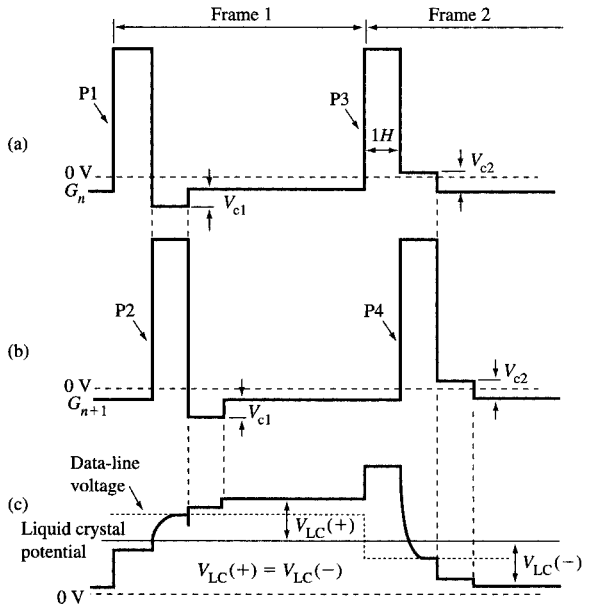

Figure 7

Frame-inversion waveforms for conventional driving method 2.

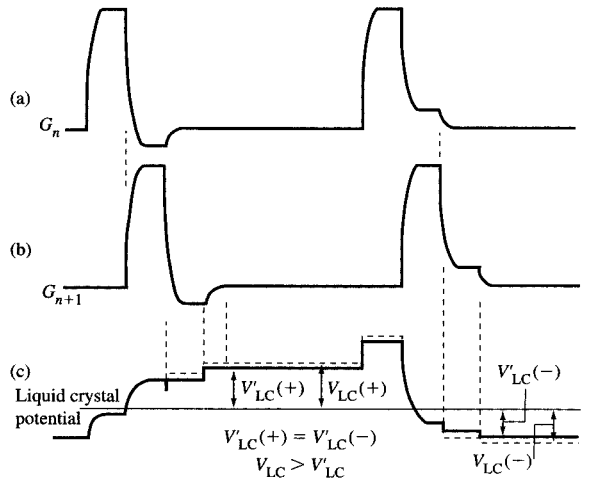

Figure 8

Waveforms for conventional driving method 2 at the terminal side.

current flows for a longer time than in the case of no gate delay. However, since the voltage levels V_{c1} and V_{c2} for the feedthrough voltage and effective-value compensation do not vary, the liquid crystal potential becomes higher than the desired value in frame 1 and lower than the desired value in frame 2. This creates dc component V_{DC} [$V_{DC} = V_{LC}(+) - V_{LC}(-)$], shown in **Figure 6**. While desired feedthrough and effective-value compensation are effected for pixels close to the gate-line-driving circuit, a dc component occurs for pixels closer to the gate-line terminal, and the compensating voltage becomes larger there.

Conventional driving method 2

To solve this problem, a case was considered in which drive waveforms are used. In the drive waveform shown in **Figure 7**, the fall timing of gate pulse P2 that is input to gate line G_{n+1} is made coincident with the time at which the potential level of previous gate line G_n is raised to V_{c1}. In this case, even if the gate delay causes the feedthrough voltage to be smaller at a position closer to the gate-line terminal, it also makes the compensation potential V_{c1} smaller. Thus, the liquid crystal potential is prevented from having a dc component. However, this driving method cannot provide sufficient effective-value compensation to change the amplitude of the liquid crystal potential, because the compensation voltage V_{c1} is smaller at positions close to the gate-line terminal. As shown in **Figure 8(c)**, although the liquid crystal potentials $V'_{LC}(+)$ and $V'_{LC}(-)$ have no dc component [$V'_{LC}(+) = V'_{LC}(-)$], they are respectively smaller than the desired values $V_{LC}(+)$ and $V_{LC}(-)$. As a result, as shown in **Figure 9**, while desired feedthrough and effective value compensation can be effected for pixels close to the gate-line driving circuit (supply-side pixels), the brightness increases at pixels close to the gate-line terminal, causing unevenness in brightness over the entire display screen. Hence, in either driving method, gate delay prevents feedthrough voltage compensation and effective-value compensation from being used at the same time. Therefore, it is impossible to reduce the degree of flicker and the image-sticking phenomenon while reducing the power consumption at the same time.

New driving method for gate-delay compensation

In an active-matrix LCD in which TFTs are used as switching elements, a potential variation dV_G in a gate pulse causes, via the gate–source parasitic capacitance, a feedthrough voltage $dV_G * C_{GS}/C_{all}$ in the negative direction with respect to pixel potential, where C_{GS} is the gate–source parasitic capacitance and C_{all} is the capacitance of the entire pixel. It is assumed that $C_{all} = C_S + C_{GS} + C_{LC}$, where C_S is the storage capacitance and C_{LC} is the liquid crystal capacitance. Since the capacitance of the liquid crystal varies owing to the anisotropy of its dielectric constant, the feedthrough voltage has different values for different liquid crystal application voltages.

According to the principle of compensating for the feedthrough voltage by applying two different compensation voltages $V_C(+)$ and $V_C(-)$ via C_S for positive- and negative-charge operations, respectively, pixel potential variations of $V_C(+) * C_S/C_{all}$ and $V_C(-) * C_S/C_{all}$ are superimposed. The occurrence of a dc component is suppressed irrespective of capacitance variations in the liquid crystal by satisfying Equation (1):

$$V_C(+) * C_S/C_{all} - V_G * C_{GS}/C_{all} = V_C(-) * C_S/C_{all} - V_G * C_{GS}/C_{all} = dV. \quad (1)$$

By making equal the amplitudes of the two compensation voltages, it becomes possible to make the liquid crystal application voltage larger by dV than the voltage supplied from the data line, as shown in Equation (1). Thus, it becomes possible to reduce the output voltage of the source driver and consequently the driving power. However, the above driving method has the problem of being influenced by any delay in gate voltage (signal delays in both the C_S line and the gate line in cases where C_S is on a separate line. Since the gate delay causes the feedthrough voltage to become smaller at the far end of the gate line, a voltage that is compensated via C_S becomes larger and causes a dc component. One method of solving this problem would be to make an adjustment between the gate-off timing and the timing of compensation-voltage output. Although this method can prevent the occurrence of a dc component, it is defective in that the liquid crystal application voltage varies if the amplitudes of the two compensation voltages are made too large. Therefore, dV cannot be made large, and it becomes difficult to reduce the driving power. The new driving method solves the above problems by outputting the compensation voltage at two different timings. That is, the first compensation voltage is output at the same timing as the gate-off timing so as to satisfy $dV = 0$, to thereby prevent the occurrence of any dc voltage due to gate delay. In other words, the first compensation voltage compensates only for feedthrough voltage and not for effective value, even if gate delay occurs because the output timing of the first compensation voltage is the same as the gate-off timing. Thereafter, the second compensation voltage is output so that dV becomes a target value. That is, in **Figure 10** Equation (2) is satisfied:

$$dV = V_{c1b} * C_S/C_{all} + (V_{c1a} + V_{c1b}) * C_{GS}/C_{all} = V_{c2b} * C_S/C_{all} + (V_{c2b} - V_{c2a}) * C_{GS}/C_{all}. \quad (2)$$

Since the second output is not influenced by gate delay, dV can be made large. That is, the new driving method is characterized in that the pixel signal of a data line is transmitted to a pixel electrode by turning on a TFT by applying a gate signal to the gate line, and that after feedthrough voltage compensation is effected by applying

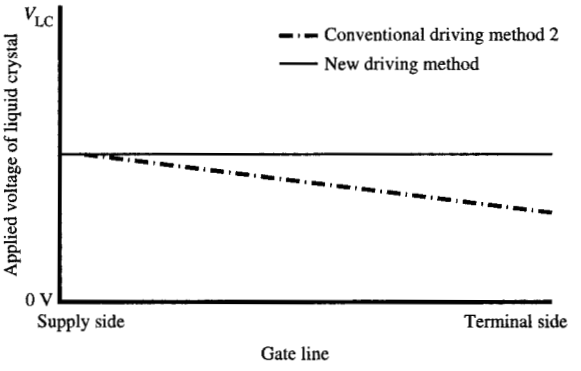

Figure 9

V_{LC} from supply side to terminal side.

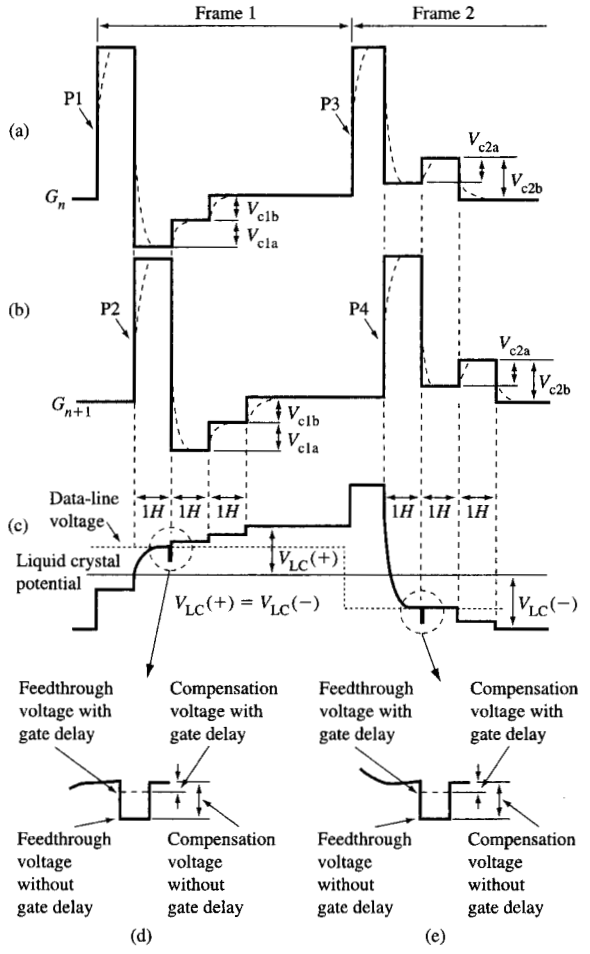

Figure 10

New driving method with gate-delay compensation.

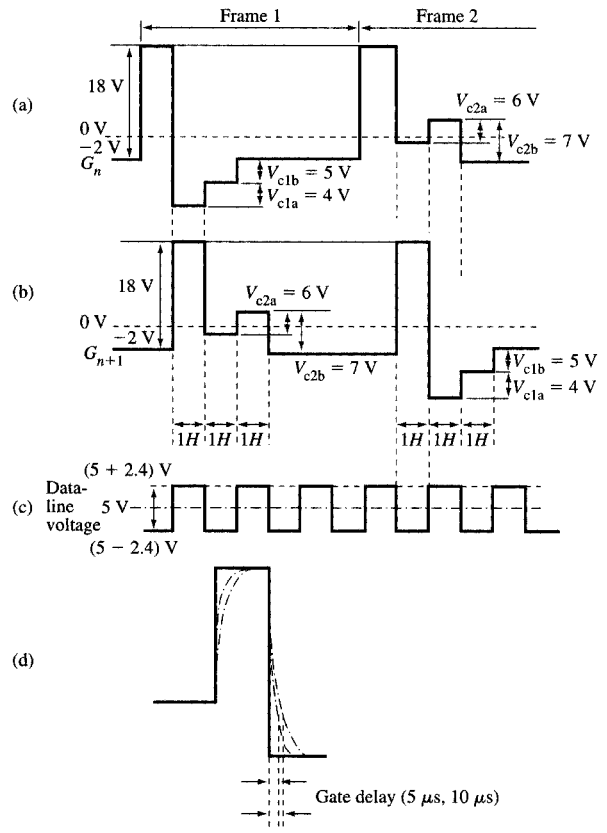

Figure 11

Actual row-inversion driving waveforms for the new driving method.

a feedthrough voltage compensation voltage to C_S, a given liquid crystal potential is applied to a liquid crystal in each pixel region by applying an effective-value compensation voltage. According to the new driving method, display quality and reliability can be improved and power consumption can be reduced by reducing drive power, suppressing the occurrence of any dc voltage that may be caused by the anisotropy of the dielectric constant of a liquid crystal, and preventing variations in liquid crystal application voltage caused by gate delay in the TFT/LCD driving and voltage-setting circuits.

Detailed explanation of the new driving method

The new driving method is described with reference to Figure 10, which shows two kinds of driving waveforms for gate lines. The waveforms drawn as solid lines are those on the side close to the gate-line-driving circuit, and are not distorted by gate delay. The waveforms drawn as broken lines are those on the side far from the gate-line-driving circuit, i.e., close to the gate-line terminal, and are distorted by gate delay.

First, we describe the case of no gate delay (solid-line waveforms). As shown in Figure 10(b), a TFT connected to the $(n + 1)$th gate line G_{n+1} is turned on by a gate pulse P2 (pulse width: $1H$, or one horizontal scanning period) that is input to that gate line, and a voltage is applied to the liquid crystal, as shown in Figure 10(c). When the TFT is turned off, the charged voltage to the liquid crystal is reduced by a feedthrough voltage because of a feedthrough phenomenon that is caused by the fall of gate pulse P2. However, feedthrough voltage compensation is effected by increasing the level of the previous gate line G_n by a potential V_{c1a}, as shown in Figure 10(a), to coincide with the fall of gate pulse P2 on gate line G_{n+1}. The potential V_{c1a} can be set at a level that compensates exactly for the feedthrough voltage, with no consideration of gate delay. Thereafter, after a lapse of $1H$, the potential of gate line G_{n+1} is raised by V_{c1a} and, at the same time, the potential of the previous gate line G_n is raised from V_{c1a} to V_{c1b}. Raising the potential level of gate line G_{n+1} to V_{c1a} provides feedthrough voltage compensation on the liquid crystal of a pixel connected to the next gate line, G_{n+2}. Final effective-value compensation is effected on the pixel that is connected to gate line G_{n+1} by increasing the potential of that gate line to V_{c1b} after a lapse of $1H$ [Figure 10(c)]. In this manner, in the new driving method, the feedthrough voltage compensation potential V_{c1a} and the effective-value compensation potential V_{c1b} are applied to C_S separately, i.e., in two steps. As shown in Figure 10, as a result of feedthrough voltage compensation and effective-value compensation, the liquid crystal potential is set at $V_{LC}(+)$ during frame 1. Next, in frame 2, to ac-drive the liquid crystal, the feedthrough voltage compensation is set at voltage level V_{c2a}, and then the effective-value compensation is effected at V_{c2b} by a process similar to that in frame 1, so that the liquid crystal potential becomes $V_{LC}(-)$.

We now describe the case for which gate delay occurs (broken-line waveforms in Figure 10). As shown in Figure 10(b), the TFT connected to the $(n + 1)$th gate line G_{n+1} is turned on by a gate pulse P2 that is input to the gate line as before, but is rounded by gate delay. A voltage is applied to the liquid crystal, as shown in Figure 10(c). When the TFT is turned off, the charged voltage to the liquid crystal is reduced by a feedthrough voltage that is caused by the fall of gate pulse P2. However, as shown in Figure 10(d), since the gate delay elongates the gate-on period during which a gate–source current flows, the feedthrough decreases from the case of no gate delay. However, since the fall timing of gate pulse P2 is made coincident with the increase in potential level of the

previous gate line G_n to V_{c1a}, the feedthrough voltage compensation potential V_{c1a} is also decreased by the gate delay, but the feedthrough voltage is smaller at positions closer to the gate-line terminal. Therefore, the feedthrough compensation voltage, which is supplied by the gate-line-driving circuit, can prevent the liquid crystal potential from having a dc component even without considering gate delay.

In this manner, in the new driving method, the feedthrough voltage compensation potential V_{c1a} and the effective value compensation potential V_{c1b} are applied to the C_S separately, i.e., in two steps. Since the effective-value compensation is applied *after* the feedthrough voltage compensation has been effected, the reduction in effective-value compensation near the gate-line terminal does not occur. In frame 2, the feedthrough voltage compensation is effected at a voltage level V_{c2a}, and then the effective-value compensation is applied at V_{c2b} in the same manner as in frame 1. As a result, as shown in Figures 6 and 9, the feedthrough voltage causes no dc component in the liquid crystal potential, and any variation in effective-value compensation causes no unevenness in the brightness of the display over the entire gate line. Thus, a TFT/LCD can be realized with low power consumption.

Experiment

Figure 11 shows driving waveforms for the case in which row-inversion driving is performed on a C_S-on-gate-type LCD. V_{LC} is the RMS voltage when a 2.4-V data-line (or signal) voltage is applied to the pixel. About 50% transmittance is obtained from this signal voltage. We chose this voltage because it exhibits the most sensitive transmittance variation.

The respective capacitance ratios and an effective-value compensation value [dV in Equation (1)] used in this experiment are

$$C_{GS}/C_S = 0.2,$$

$$C_S/C_{all} = 0.25 \qquad (C_{all} = C_S + C_{GS} + C_{LC}),$$

$$dV = 1.2 \text{ V}.$$

As shown in Figure 11(d), delays in terms of a time constant at the terminal end of the gate line were 5 μs and 10 μs. The driving voltages and timing were such that after a gate-on voltage of 20 V is output for 1H, feedthrough voltage compensation is effected by outputting a first compensation voltage (4 V in frame 1 and 6 V in frame 2) at the same time as the gate-off drop. Effective-value compensation is then imposed by outputting a second compensation voltage (5 V in frame 1 and 7 V in frame 2) after a lapse of 1H.

We now describe the occurrence of a dc component on the gate-line supply side and the change in that component

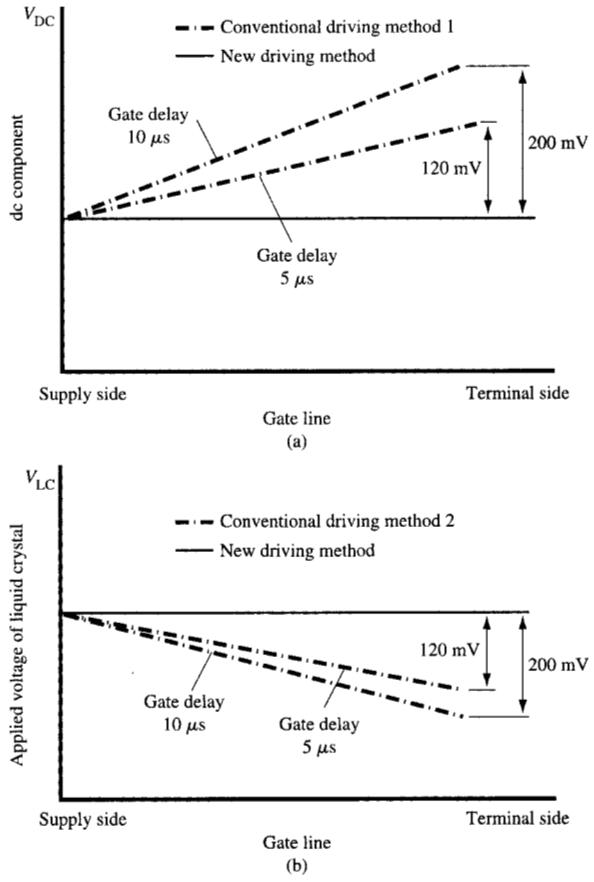

Figure 12

Actual V_{DC} (a) and V_{LC} (b) from supply side to terminal side for the new driving method.

on the terminal side due to gate delay. **Figure 12(a)** compares the driving method of this experiment with conventional driving method 1. Conventional driving method 1, shown in this figure, is similar to that shown in Figure 2. However, whereas in the driving method of Figure 2, V_{c1} and V_{c2} are output after a lapse of 0.5H from the rise of gate pulse P2, in the comparative example for this experiment they are output after a lapse of 1H from the rise of gate pulse P2. In conventional driving method 1, dc component variations of about 120 mV and 200 mV occurred with gate delays of 5 μs and 10 μs, respectively. With delay-compensation driving in the new driving method, it was confirmed that the dc component due to gate delay was about 20 mV and about 30 mV for gate delays of 6 μs and 10 μs, respectively.

Next, with reference to **Figure 12(b)**, we describe the brightness variation with the new driving method and

compare it with that of conventional driving method 2. The vertical axis of Figure 12(b) represents the variation of source-driver output voltage with a liquid crystal transmittance of 50%. Conventional driving method 2, shown in Figure 12(b), is similar to that shown in Figure 7. In this method, variations of about 120 mV and about 150 mV occurred with gate delays of 5 μs and 10 μs, respectively. With the delay compensation of the new driving method, it was confirmed that these variations could be suppressed to about 20 mV for gate delays of both 5 μs and 10 μs.

Discussion

In new driving method described in this paper, both the dc component and the variation of V_{LC} could be considerably reduced. About 30 mV of dc component error and about 20 mV of V_{LC} variation remain for a gate delay of 10 μs, but these errors are acceptable in our design specification because their magnitude is very small and the change is too gradual to be noticed.

We have confirmed that the new driving method is effective in reducing power consumption because it minimizes both major error-compensation problems, while permitting low power consumption in the driver circuits.

Conclusions

Conventional driving methods exhibit both reduced effective-value compensation and dc components due to gate delay in the pixel signal. We have developed a method which minimizes both problems simultaneously and have verified by experiment that the approach is sufficient for the design specification. We have found that the new driving method is very effective for large, high-resolution TFT/LCDs such as LCD monitors for desktop PCs and workstations.

Acknowledgments

The authors wish to express their gratitude to H. Suzuki for valuable discussions and encouragement throughout this work, and to M. Atsumi, M. Suzuki, M. Kodate, and K. Nagayama for experimental assistance and discussions.

References

1. S. Nagata, "Capacitively Coupled Driving Method of TFT-LCD," *Digest of Technical Papers*, Society for Information Display, 1986, p. 242.
2. T. Yanagisawa, "Compensation of the Display Electrode Voltage Distortion," *Proceedings of the Sixth International Display Research Conference (Japan Display)*, 1986, p. 192.
3. K. Suzuki, "A 220 × 240 Pixel a-Si TFT Matrix Transmission Liquid Crystal Display," *Proc. SID* **25,** 11 (1984).
4. K. Suzuki, "Compensative Addressing for Switching Distortion in a-Si TFTLCD," *Proceedings of the Seventh International Display Research Conference (Euro Display)*, 1987, p. 111.
5. E. Takeda, "Simplified Method of Capacitively Coupled Driving for TFT-LCD," *Proceedings of the Ninth International Display Research Conference*, 1989, pp. 580–583.
6. E. Takeda, "Capacitively Coupled TFT-LCD Driving Method," *Proc. SID* **28,** 87 (1990).
7. Y. Nanno, "Characterization of the Sticking Effects of TFT-LCDs," *Proceedings of the Tenth International Display Research Conference*, Society for Information Display, 1990, p. 404.
8. H. Kamiya, M. Yasui, T. Nakamura, and S. Aoki, "A Novel Driving Method of TFT-LCD with Low Power Consumption," *Proceedings of the International Workshop on Active Matrix Liquid Crystal Displays,* 1994, p. 60.
9. Y. Nanno, H. Maeda, E. Yamamoto, T. Tsukada, E. Takeda, and I. Yamashita, "An Advanced Capacitively Coupled Driving Method for TFT-LCDs," *J. SID* **2,** 143 (1994).

Received May 7, 1997; accepted for publication November 24, 1997

Kaoru Kusafuka *IBM Japan Ltd., Display Technology, Display Business Unit, 1623-14, Shimotsuruma, Yamato-shi, Kanagawa-ken 242, Japan (jl20306@jp.ibm.com).* Mr. Kusafuka studied physical chemistry at Tokyo University; he received his M.S. degree in 1988, joining IBM Japan the same year. He works on TFT/LCD design.

Hidehisa Shimizu *IBM Japan Ltd., Display Technology, Display Business Unit, 1623-14, Shimotsuruma, Yamato-shi, Kanagawa-ken 242, Japan (jl26275@jp.ibm.com).* Mr. Shimizu studied electrical engineering at Mriji University, graduating in 1992 and joining IBM Japan the same year. He has worked on LCD design of 12.1-in. XGA and 16.1-in. SXGA and is currently working on the design of large-scale LCD monitors.

Shinichi Kimura *IBM Japan Ltd., Display Technology, Display Business Unit, 1623-14, Shimotsuruma, Yamato-shi, Kanagawa-ken 242, Japan (jl04830@jp.ibm.com).* Mr. Kimura studied electrical engineering at the Science University of Tokyo, graduating in 1981. In 1983 he joined the IBM Fujisawa Development Laboratory to work in display development. He now specializes in TFT/LCD design.