

On-chip metallization layers for reflective light valves

by E. G. Colgan
M. Uda

The metallization layers required for a silicon-based reflective liquid crystal light valve have been developed and integrated with a medium-voltage CMOS process using standard microelectronic manufacturing tools. Unique requirements include the following: 1) shielding the Si devices from incident light so that electron-hole pairs are not formed; 2) high optical throughput and contrast, which are dependent on the mirror fill factor, reflectivity, and flatness; 3) pixel storage capacitance to maintain the voltage across the liquid crystal cell with sufficient accuracy to select the desired gray level until the data are updated; and 4) precise control of the liquid crystal cell thickness without spacers obscuring the mirrors. Wafers have been successfully fabricated to support a technology demonstration of a 2048×2048 -pixel ("four-million-pixel") projection display. The process is based on a medium-voltage CMOS process and uses six masks (for three metal levels, one via level, and two insulator levels) after Si device processing has been completed.

Introduction

Light valves (LVs) are used in projection displays, optical interconnects, holographic storage, and other applications

where light is modulated spatially and temporally by an array of data. There are a number of advantages to Si-based reflective LVs. With a reflective LV, a high optical throughput can be achieved even with small pixels, because the address lines and pixel storage capacitors do not block the light as in a transmissive display. With single-crystal Si, transistor switching speed is faster than with the amorphous or polycrystalline Si used for flat panels or transmissive projection displays, thus permitting the development of displays with a higher information content. Additionally, even older Si manufacturing facilities can support much finer feature sizes than are currently available with flat-panel manufacturing technology. Minimizing the pixel size is desirable, since the size of optical components scales with the LV.

The light valves described in this work were fabricated by taking advantage of an established medium-voltage CMOS process [1], which could provide the voltage required. The use of full wafer lithography tools permitted the patterning of $1.2\text{-}\mu\text{m}$ features and the use of a relatively large chip size. Furthermore, the presence of advanced tools and processes for current-generation products on the same manufacturing line facilitated planarization of the wafers. The ground rules permitted use of a pixel $17\text{ }\mu\text{m}$ on a side. A metallization-only test site was used to qualify the metallization and liquid crystal processes. Subsequently, a 2048×2048 active-matrix LV with integrated gate and external data drivers was fabricated as a technology demonstration. The LV chip

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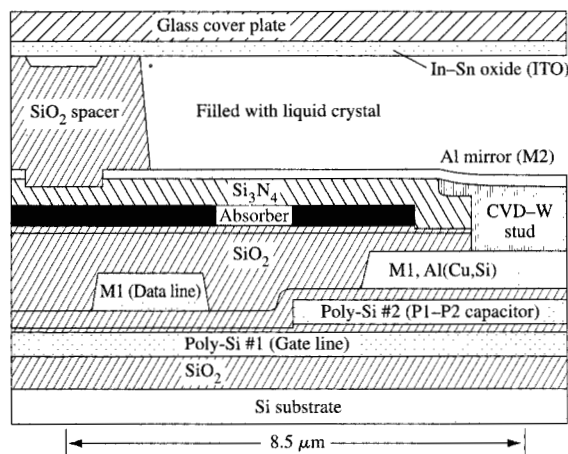


Figure 1

Schematic cross section of a pixel of the four-million-pixel light valve.

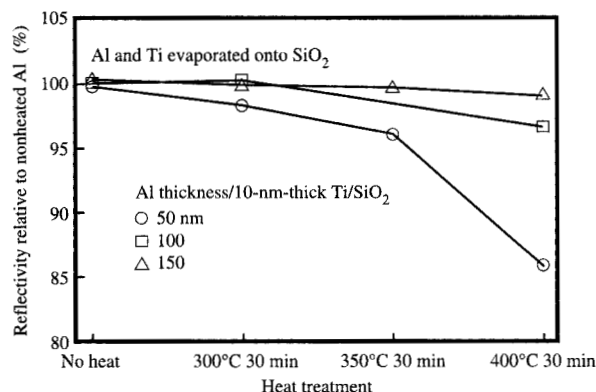


Figure 2

Relative average red, green, and blue reflectivity of 50-, 100-, and 150-nm-thick Al/10-nm-thick Ti/SiO₂ films vs. annealing temperature.

was 64 mm on a side, and its active array was about 35 mm on a side, the additional edge length being required for data-driver connections. In the metallization processing, extensive use was made of advanced process elements [2, 3]. In the next section, the complete metallization structure and how it functions are described. This is followed by a description of the metallization fabrication process.

Structure and function

A schematic drawing of a pixel cross section from the 4M-pixel LV is shown in **Figure 1**. The materials used and configuration were carefully chosen to simultaneously meet a variety of requirements. The functional requirements for a reflective Si-based LV include 1) shielding the Si from the incident light, 2) high optical throughput and contrast, 3) pixel storage capacitance, and 4) precise control of the liquid crystal (LC) cell thickness without spacers obscuring the mirrors.

With the structure shown in **Figure 1**, shielding the Si devices from light is accomplished by the combination of the M2 mirror layer and the absorber (AR) layer. Both the M2 and AR layers are sufficiently thick that they are optically opaque. Light incident between the mirrors would require multiple reflections between the top of the AR layer and the bottom of the mirror layer to reach the Si substrate. The top surface of the AR layer is TiN, which has a reflectivity range between 20% for blue light and 65% for red light. For red light incident at 7° off normal, nearly 100 reflections would be needed for the light to reach the opening in the AR layer around the stud, and the intensity would be reduced by more than 10⁻¹⁰. Outside the array region, a blanket AR layer is used to protect the Si devices from incident light.

Another key issue with an LV is its optical throughput. The optical throughput depends on the fraction of the area occupied by its mirrors, the reflectivity of the mirrors, and their flatness. The mirror fill factor is determined by the smallest space which can be reliably patterned into the mirror material and depends on the available lithography and patterning technology. For a 17-μm-square pixel with a nominal space of 1.7 μm between mirrors, the mirror fill factor is 81%. A reduced space is possible, but increases the probability of mirror-to-mirror shorts because of the very large array area. The M2 mirrors are made of Al films, since Al is one of the most reflective metals (92% on average for the wavelengths of interest in air [4]). Since Al(Cu) alloys are commonly used for semiconductor metallizations, the use of Al for M2 required no process development. (The copper is added to aluminum to improve the electromigration performance and reduce hillock formation.) Silver is slightly more reflective (93%) [4], but it oxidizes rapidly, and hence its use would require extensive process development work. A disadvantage of Al films is the formation of hillocks during thermal cycling due to the thermal expansion mismatch with the substrate. Hillock formation can be minimized by limiting the heat treatments after M2 deposition or by limiting the Al grain size. Typical processing temperatures reached after mirror deposition are 400°C, which might be reduced to 350°C. The Al grain size can be reduced by limiting the film thickness or with alloy additions [5]. Reducing film thickness too much can result in agglomeration after annealing,

which also reduces the reflectivity, as illustrated in **Figure 2**. On the basis of these results, a mirror thickness of 150 nm was chosen, with a 10-nm-thick Ti underlayer for improved adhesion and contact resistance. Alloying the Al with Cu reduces the reflectivity slightly with low-temperature annealing, but the reflectivity after annealing at 400°C is significantly better owing to the reduced hillock formation (**Figure 3**).

The flatness of the mirrors depends on the planarity of the surface on which they are deposited. The use of a chemical-mechanical-polished (CMP) insulator layer for planarized mirrors on a Si wafer containing the drive elements was previously described [6] and corresponding planarization demonstrated [7]. Since chemical-mechanical polishing has been used in advanced metallization processes for planarization of both insulator and metal layers [2, 3], this technique was adopted for planarization of the mirrors. The thick SiO₂ film deposited over the M1 layer is polished, resulting in a planar surface below the AR layer, as shown in Figure 1. The resulting mirrors are very planar, as indicated by the data of **Figure 4**. To obtain the data shown, a 150-nm-thick Al blanket mirror (M2) was deposited on regions containing no underlying topography, patterned absorber and studs, and patterned M1 segments, absorber, and studs; reflectivity was reduced by only about 1% by the presence of the underlying topography. This is probably due to the "dimple" formed by the mirror contact (Figure 1).

The contrast ratio of the LV can be degraded by light reflected from the exposed AR layer between the mirrors. This is an additional reason for reducing the reflectivity of the AR layer as much as possible. But note that the contrast also depends on the liquid crystal mode used and what electric fields are present between the pixels, since the reflected light must have the correct polarization to appear as part of the image.

To minimize Si device processing changes and pixel size, a significant portion of the pixel storage capacitance was included in the metallization structure described here. The AR layer is connected to a fixed potential, and the AR-to-M2 and AR-to-M1 overlap regions provide a portion of the pixel capacitor. A layer of Si₃N₄ is used as the insulator between AR and M2, since silicon nitride has a higher dielectric constant (about 7) than SiO₂ (near 4.1). It is necessary to have enough pixel storage capacitance to retain the voltage across the liquid crystal cell with sufficient accuracy to resolve the desired number of gray levels until the data are updated.

Precise control of both the absolute value and uniformity of the liquid crystal cell thickness is required for high contrast and good uniformity. The desired cell gap is determined by the liquid crystal material used, the liquid crystal mode selected, and the wavelength of the incident light. With flat-panel displays, plastic spheres

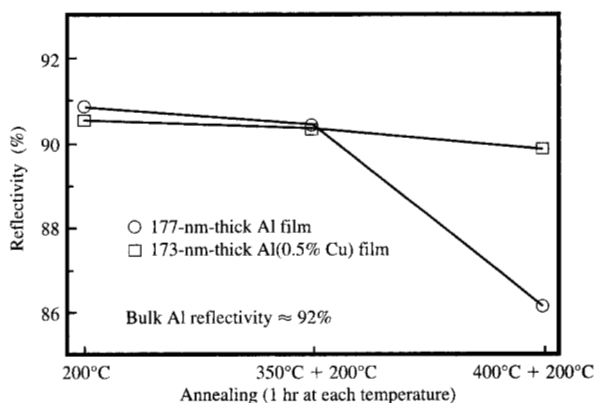


Figure 3

Average red, green, and blue reflectivity of 175-nm-thick Al and Al(0.5% Cu) films vs. annealing temperature.

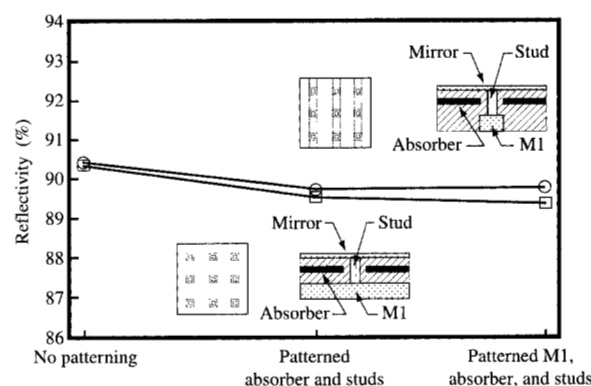


Figure 4

Average red, green, and blue reflectivity of blanket 150-nm-thick Al films vs. wafer topography on two test-site wafers. The topography is indicated schematically for the patterned cases. For comparison, the reflectivity of bulk Al is about 92%.

about 5 μm in size are randomly dispersed in the cell gap to serve as spacers. For the very small pixel size being used here, this is not practical, since a single spacer ball could theoretically block 6% of the area of a mirror; this is significant, since with a 4-bit gray scale the least-significant bit corresponds to a 6% change in brightness, and any clustering could cause more severe mirror shadowing. The use of rigid SiO₂ spacers built on the front glass was previously reported by Glueck et al. [8]. These have the serious disadvantage that with very small

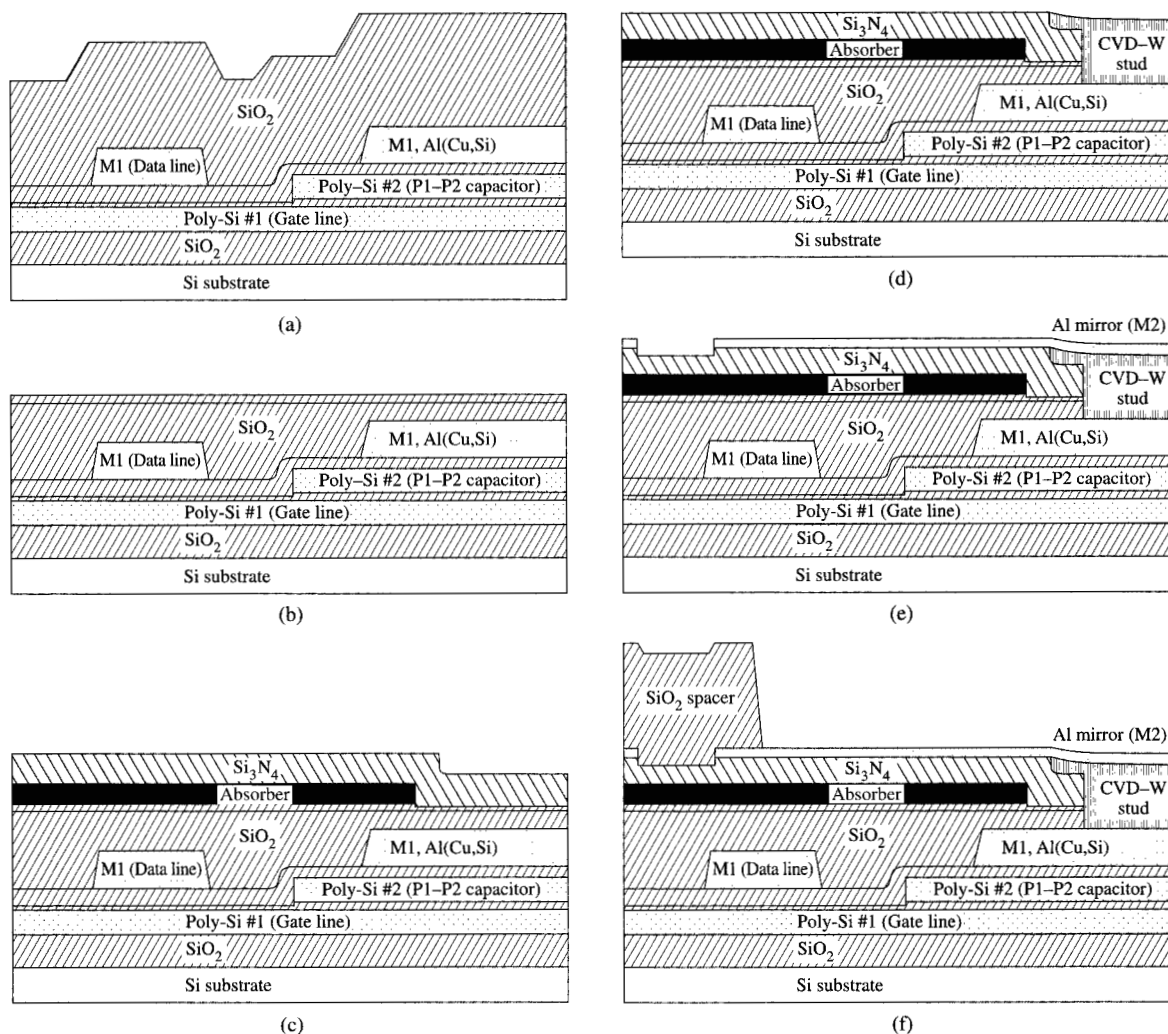


Figure 5

Schematic diagram of process flow for metallization layers for reflective light valve: (a) M1 liftoff and SiO₂ deposition; (b) SiO₂ CMP and SiO₂ deposition; (c) absorber deposition, patterning, and Si₃N₄ deposition; (d) stud etch, CVD-W deposition, and W CMP; (e) M2 deposition and patterning; (f) spacer SiO₂ deposition, patterning, and TV etch to expose contact pads.

pixel sizes, the cover glass must be very accurately aligned to the substrate to locate the rigid SiO₂ spacers between pixels. For transmission thin-film-transistor (TFT) displays, the use of a patterned black polymer as a light-blocking and spacer layer has been demonstrated [9]. The use of spacers fabricated by etching a uniform layer on a silicon wafer containing the drive elements was also previously described [6]. We have used a similar method: A uniform blanket layer of SiO₂ of the correct thickness was deposited over the mirrors and patterned to leave spacer posts at the corners of the mirrors. The density of spacer

posts needed was determined from finite-element modeling. (It is desirable to minimize the density of spacers, because they can degrade the contrast ratio.)

Process description

The metallization process used in LV fabrication is illustrated schematically in **Figures 5(a)–(f)**. After the Si device processing is completed, liftoff is used to pattern M1 [10]. A liftoff stencil is patterned by photolithography, a layer of Si and a layer of Al(Cu) are evaporated, and the liftoff stencil is removed with a suitable solvent,

leaving the metallization in the desired regions. The Si layer is needed to prevent dissolution of Si from the devices into the Al and spiking of the contact regions during subsequent thermal treatments. The Al(Cu) is alloyed with the Si after annealing. After the M1 liftoff is completed, a thick conformal oxide layer is deposited [Figure 5(a)].

The next process step is planarization of the SiO_2 by CMP to provide a flat surface for the mirrors. This is more difficult than the typical insulator CMP step for current-generation CMOS, because here the topography is greater and the chip size is relatively large. Typically [2, 3] a thick SiO_2 layer is deposited and planarized after Si device processing. A contact stud is then formed, the M1 level deposited and patterned, and an insulator deposited and planarized. This process flow uses two separate CMP steps to planarize the topography from the Si devices and M1. As shown in Figure 5(b), a single CMP step is used to simultaneously planarize the topography from both the Si devices and M1. The greater-than-usual topographic variation increases the difficulty of planarization. The large chip size causes two problems: a larger area which needs global planarization, and larger regions with different pattern densities. To clarify this, the chip contains regions such as the array with a high density of polysilicon 1 (poly1), poly2, and M1 regions, whereas the contact area contains a similar M1 density but only limited poly1 and poly2 regions; some regions contain none of these layers. Once these regions are sufficiently large, the polishing pad is unable to "bridge" over them, and global planarization is impossible. This problem was solved by adding "dummy" poly1, poly2, and M1 features during the chip design, so that the pattern density is uniform enough on a small enough scale that global planarization can be achieved. At the CMP endpoint, a SiO_2 layer about 500 nm thick remains over the highest M1 feature. Next, a 200-nm-thick SiO_2 layer is deposited on the planarized SiO_2 surface as protection against any M1 that may be exposed by scratching [Figure 5(b)].

The absorber (AR, which would be referred to as "M2" if it were used as a wiring level) layer is formed by sputter-deposition of a 10-nm-thick layer of Ti, a 100-nm-thick layer of Al(Cu), and a 50-nm-thick layer of TiN, followed by patterning by reactive ion etching (RIE). The AR layer is similar to a standard CMOS metallization layer, for which an underlying Ti layer is used for improved adhesion and contact resistance, a surface TiN layer is used as an antireflection coating, the bulk of the metallization is Al(Cu), and the metal layers are patterned by RIE. For typical CMOS metallization, an antireflection coating is needed on the Al(Cu) metallization to reduce reflections so that fine features can be patterned by photolithography. Titanium nitride was used on the surface of the AR layer, since the necessary process steps

were already available, although a lower red light reflectivity would have been desirable. After the AR layer is patterned, a 400–500-nm-thick layer of Si_3N_4 is deposited [Figure 5(c)]. This thickness is a compromise between the need for a thinner layer for greater AR–M2 capacitance and a thicker layer to reduce the probability of AR-to-M2 defects and shorts.

The next step is to pattern the Si_3N_4 layer and the SiO_2 down to the M1 layer using the via mask. The etching depth must be adequate to compensate for the variations in the SiO_2 thickness over the M1 layer. The tungsten studs are formed by the sputtering of a Ti and TiN liner layer, the growth of a chemical-vapor-deposited (CVD) W layer, and the removal of the excess W outside the features by CMP. This W stud fabrication has been adopted directly from current CMOS processes. Note that a "dimple" is formed which is nearly as wide as the AR opening due to the higher polishing rate of W compared to Si_3N_4 and the "dishing" which occurs during CMP [3]. This is illustrated in Figure 5(d).

The M2 mirror is formed by evaporation of a 10-nm-thick layer of Ti followed by a 150-nm-thick layer of Al. The Ti layer is used for improved adhesion and contact resistance. The photolithography is difficult because of the high reflectivity of the M2 layer, which is then patterned by RIE [Figure 5(e)]. The rigid SiO_2 spacers are formed by depositing a $>3\text{-}\mu\text{m}$ -thick oxide layer on the wafer. The photolithography process for patterning the spacers is complicated by the large variation in TiN and Al reflectivity for the ultraviolet light used in photoprocessing. Since the spacer height uniformity is of critical importance for liquid crystal performance, the SiO_2 deposition process was optimized to give a uniformity of better than 2% (1σ). The blanket SiO_2 layer is patterned by RIE, adjusted to produce a low Si_3N_4 etch rate so that the over-etching required does not expose the AR layer between the mirrors, as illustrated in Figure 5(f). The final process step is the terminal via (TV) etch, which removes the Si_3N_4 and SiO_2 layers over the M1 contact and test pads.

One detail not covered by the above description is how electrical contact is made to the AR layer. By using a combination of an AR feature and a stud feature that is larger than the AR feature, an M1- or M2-to-AR contact can be formed [since the AR layer contains a 100-nm-thick layer of Al(Cu), which acts as an etch-stop during the patterning of the stud opening]. The only difficulty with this approach occurs if the stud-opening etch does not stop in the Al(Cu) layer, in which case only an edge contact is formed. For this reason, the design rules for the LV chip call for redundant AR contacts; this has no impact on performance, since only a limited number of contacts to AR are needed.

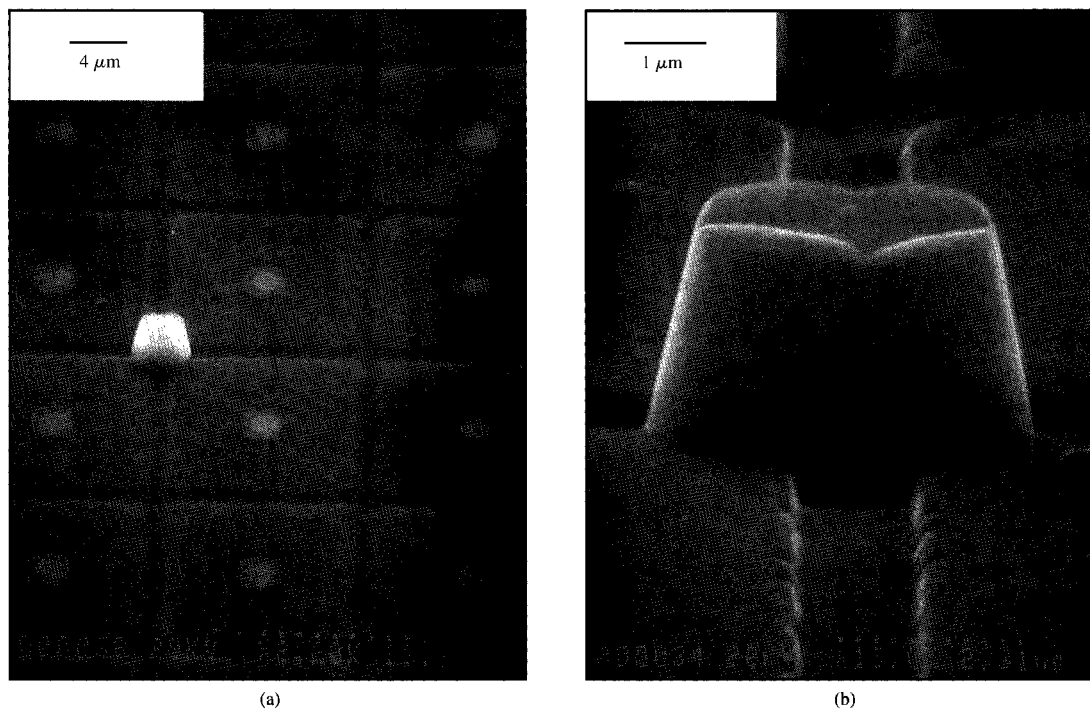


Figure 6

Scanning electron micrographs of portions of the completed four-million-pixel light-valve chip.

Scanning electron micrographs of the completed metallization structure that is thus formed are shown in **Figure 6**. Some Al hillocks are evident on the M2 mirrors. The structure on the top of the spacers, seen in Figure 6(b), is a replication of the topography from the patterned M2 which was present when the spacer SiO_2 layer was deposited. The dimple in the mirror from the stud contact is evident because of the increased electron scattering by the tungsten layer beneath the mirror. The brightest region corresponds to the W stud, and the surrounding slightly darker region to the AR opening reduced by the Si_3N_4 thickness [see Figure 6(a) and Figure 1].

Summary

A metallization process for a medium-voltage CMOS-based reflective liquid crystal four-million-pixel light valve has been developed and demonstrated. A six-mask process (after Si device processing) and standard manufacturing tools have been used to fabricate metallization structures which meet the unique requirements of a reflective light valve. These requirements include 1) shielding the Si from the incident light, 2) high optical throughput and contrast,

3) pixel storage capacitance, and 4) precise control of the liquid crystal cell thickness without spacers obscuring the mirrors.

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Evan G. Colgan IBM Research Division, Thomas J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598 (ecolgan@us.ibm.com). Dr. Colgan is a Research Staff Member at the IBM Thomas J. Watson Research Center in the Flat Panel Display Technologies area, and also works on projection display technology. He previously managed the Thin-Film Transistor Processing Department. Dr. Colgan joined the Research Division in 1995; he was previously an Advisory Engineer at the Semiconductor Research and Development Center in Hopewell Junction, New York. While at the Development Center, since joining IBM in 1987, he worked on aspects of metal silicide formation, selective chemical vapor deposition of tungsten, diffusion barriers, Al(Cu) microstructure evolution, and integration of both Cu- and Al-based metallizations for integrated circuits. Dr. Colgan received his B.S. degree in applied physics from the California Institute of Technology in 1982 and his Ph.D. in materials science and engineering from Cornell University in 1987. His thesis work involved the formation of aluminides from thin-film couples. Dr. Colgan has published more than seventy papers and has been issued eleven patents; he is a member of the MRS, IEEE, APS, Bohmische Physical Society, and Sigma Xi.

Mitsuru Uda IBM Microelectronics Division, Yasu facility, 800, Ichimiyake, Yasu-cho, Yasu-gun, Shiga-ken 520-23, Japan (udaman@jp.ibm.com). Mr. Uda is a Staff Engineer at the IBM Yasu facility. Since joining IBM in 1989 as a photolithography engineer, he has worked on the integration of process modules and defect reduction for a variety of CMOS products. He received his B.S. degree in mechanical engineering from Doshisha University in Kyoto, Japan, in 1983. Prior to joining IBM, he worked at Toppan Printing on the development of LCD color filters. Mr. Uda has been issued six patents.

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