

Advanced DUV photolithography in a pilot line environment

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As the critical path to increasing circuit density, deep-ultraviolet (DUV) lithography has played a key role in the development of new semiconductor products. At present, DUV refers to imagery at the 248-nm wavelength, with the introduction of 193-nm photolithographic systems anticipated in the next few years. This paper presents an overview of DUV lithography applications in the IBM Advanced Semiconductor Technology Center (ASTC). Since 1990, we have used DUV lithography for critical levels of advanced generations of DRAM (64Mb, 256Mb, and 1Gb) and associated families of logic products. We describe the means by which DUV capability and productivity have increased in a decreasing process window environment. Tooling, processes, and process control systems have undergone continuous improvement to accommodate increasing wafer starts and the rapid introduction of new products.

Introduction

The IBM Advanced Semiconductor Technology Center (ASTC) is a pilot line created in 1989 for the development and early manufacture of all advanced IBM semiconductor products. It has also been the site of recent development alliances among IBM, Siemens, and Toshiba, and is currently in the process of transferring products to

manufacturing sites throughout the world. ASTC acts as the common foundry for future generations of DRAM (64Mb, 256Mb, and 1Gb), associated CMOS logic, and various experimental chip designs and processes. The need to process a wide spectrum of products, spanning all stages from early exploration to fully qualified manufacturing, poses a unique challenge to the efficient operation of a lithography sector at ASTC.

Deep-ultraviolet (DUV) lithography has enabled ASTC to pursue aggressive circuit ground-rule migration in the early 1990s; it has been the primary means of reducing the *minimum* ground rule (G_{min}), as illustrated in **Figure 1**. The actual minimum ground rules achieved during the first half of the decade are displayed in two ways: 1) the lower, dashed curve shows the minimum ground rule processed successfully on integrated hardware in a given year, and 2) the upper, solid curve shows the weighted average ground rule across all hardware programs and DUV exposure levels processed successfully in a given year. The weighted average minimum ground rule processed in the ASTC DUV sector is projected to fall below 0.2 μm by the year 2000.

Also indicated in Figure 1 are key DUV lithography milestones associated with the decrease in the minimum ground rule. These are expressed as the increase in numerical aperture realized on production-worthy DUV optical imaging systems over the first half of the decade, and the decrease in wavelength from 248 nm to 193 nm anticipated for the latter half [1]. While essential to the achievement of this ground-rule migration, the evolution

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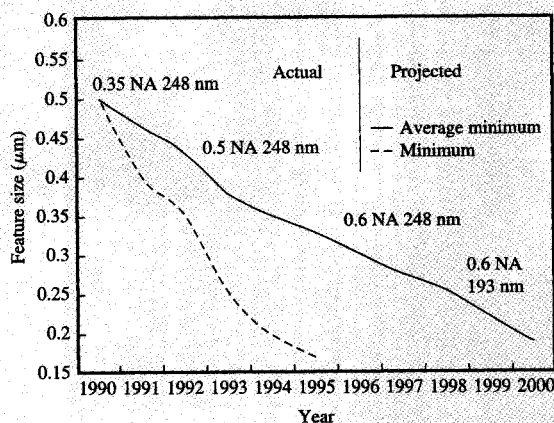


Figure 1

Actual and projected minimum ground-rule migration for development and manufacturing at ASTC during the years 1990–2000. The dashed curve shows the minimum ground rule processed in a given year. The solid curve shows the weighted average ground rule across all products and DUV exposure levels. Achieved and anticipated lithography tooling milestones (NA and wavelength) are also shown.

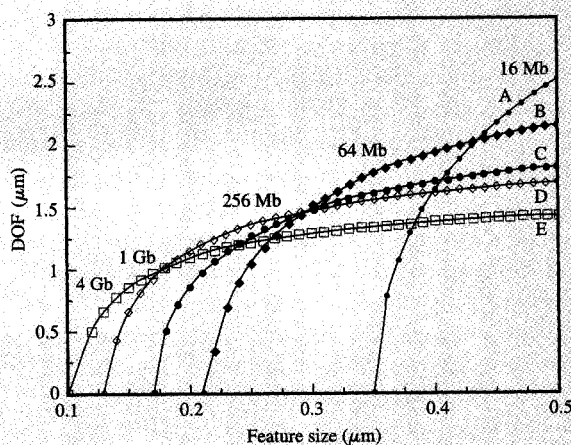


Figure 2

Change of the depth-of-focus characteristic with evolving ASTC lithographic conditions: Curve A, 248 nm, 0.35 NA, Apex-M; Curve B, 248 nm, 0.5 NA, Apex-E; Curve C, 248 nm, 0.6 NA, UV2HS; Curve D, 193 nm, 0.6 NA, Resist A; Curve E, 193 nm, 0.7 NA, Resist B.

of imaging systems is usually accompanied by a shrinking process window: namely, a decrease in the allowed depth of focus and exposure latitude to achieve the target

dimensions and tolerances, and a corresponding decrease in overlay tolerance.

The scaling of the process window with exposure equipment and photoresist improvements undertaken or anticipated at ASTC over the current decade is represented in **Figure 2**, where the simulated depth of focus (DOF) is plotted as a function of feature size for different exposure-tool and photoresist combinations. The solid curves A, B, C indicate existing 248-nm tool and resist options. The dashed curves D, E are extrapolations to future 193-nm tools and resists. Curve B in **Figure 2** corresponds to the current operating condition, a numerical aperture of 0.5 (0.5 NA) and imaging at a wavelength of 248 nm in Apex-E photoresist [2], for nearly all of the hardware being processed through the DUV sector in ASTC. At the 0.25- μm ground rules required by 256Mb manufacturing, the theoretical DOF is approximately 1.0 μm . In practice, the usable DOF is in the range of 0.6 to 0.8 μm . Curve A shows the resolution achievable with an earlier generation of tooling and resist (0.35 NA, Apex-M [3]) at ASTC. Resolution improvements are expected from the introduction of new exposure tools and resists to ASTC manufacturing. The migration of DOF as ground rules decrease with DRAM generation is shown by the labels (16Mb, 64Mb, ...) in **Figure 2**, given a plausible transition among DUV tooling and resist options. While it is possible to increase the DOF at a specific ground rule by the appropriate selection of NA/wavelength and resist combination (e.g., at 0.25 μm in **Figure 2**), the DOF continues to shrink from one generation to the next. Resist improvements and the employment of resolution-enhancement techniques, such as off-axis illumination and/or phase-shift masks, may counteract this effect to some degree, but the trend toward a smaller process window with a smaller ground rule is inexorable.

The challenge posed by the shrinking process window is exacerbated in ASTC by the need to work with current-generation tooling to pilot the next-generation products. This implies low k -factor operation, where k is the coefficient of the Rayleigh resolution criterion, defined in terms of the NA, wavelength λ , and minimum ground rule $G_{\min}$, by

$$k = NA \cdot \frac{G_{\min}}{\lambda}$$

The value of k provides an indicator of the degree of difficulty of the lithography. Higher values of k imply greater aerial image acuity due to the inclusion of more diffracted orders [4], so that lower requirements can be placed on resist contrast, pattern-dependent mask biasing, or resolution-enhancement techniques. To provide an adequate process window, historical k -factors have been greater than 0.5 during product development, and greater than 0.7 for effective manufacturing. As is evident in

Table 1, ASTC has already broken the development "rule" by operating at or below $k = 0.5$. As the limits of photolithography are extended, the manufacturing rule of k greater than 0.7 will be challenged as well. In particular, the exponential increase in tooling cost by generation [5] will drive the need to prolong the useful life of each generation in manufacturing. To date, the principal penalty for a low k -factor operation is the increased effort required for process optimization [6], and proximity correction [7, 8]. One important role of proximity correction is compensation for image shortening, as is described in the process development section below.

Against this backdrop of shrinking linewidths and latitudes, the objective of the DUV lithography photosector at ASTC is to maximize the production of high-quality product. Toward that end, many disparate functions are involved. Lithography must satisfy both its own technology requirements and the need to integrate its performance with other process sectors in the manufacturing line. Lithography can be viewed as a support for the various process sectors which define the overall manufacturing process. It is the structure of the lithography support, in a pilot line environment, which concerns us here.

The lithography constituents are materials (such as photoresist, developer, and antireflection layers), tools (stepper, track, metrology) and masks (product, test). ASTC specifies, characterizes, and melds these elements into a process. The development of a viable baseline process and its product-specific variations, the implementation of appropriate means of process control, and the integration from lithography to upstream and downstream process steps, constitute the principal missions of the ASTC.

Process constituents

The generic photolithographic process allows for a mask or reticle pattern to be transferred via spatially modulated light (the aerial image) to a photoresist film on a wafer. In cases where the wafer is already patterned, this exposure process must be preceded by an alignment step to ensure precise positioning of the new pattern level with respect to prior pattern levels. As practiced at ASTC, DUV lithography has two distinguishing attributes: 1) the delayed image formation process intrinsic to chemically amplified photoresist, and 2) the implementation of step-and-scan alignment and exposure equipment.

• Chemically amplified photoresist

In any photo-imaging process, those portions of the absorbed aerial image whose energy exceeds a threshold energy of chemical bonds in the photo-active component of the resist material act to form a latent image in the photoresist. The latent image marks the volume of

Table 1 DRAM development k -factors, actual and projected.

DRAM	Date	$G_{\min}$ (μm)	Wavelength	NA	k
64Mb	1990-1993	0.35	248	0.35	0.49
256Mb	1993-1996	0.25	248	0.5	0.50
1Gb	1996-1999	0.18	248	0.6	0.44
4Gb	1999-2002	0.13	193	0.7	0.47

photoresist material that either is removed during the development process (in the case of positive photoresist) or remains after development (in the case of negative photoresist) to create a three-dimensional pattern in the photoresist film.

The need for chemical amplification in the DUV imaging process is driven by the relatively low DUV light intensity available at the wafer plane from exposure tools [9]. The spectral intensity of mercury lamps, used in early generations of DUV tools, is roughly an order of magnitude lower at 248 nm than at 365 nm. Excimer sources can produce much higher intensities at 248 nm, but their pulsed operation, and the line narrowing required by chromatic correction in high-numerical-aperture imaging systems, constrains the light that can be delivered to the wafer. It is likely, therefore, that excimer-based systems will continue to require chemical amplification.

In chemically amplified DUV resists, the photo-active component is an acid generator. Each absorbed photon generates an acid molecule. The latent image is formed during a post-exposure bake (PEB). In the presence of heat, the photo-generated acid acts as a catalyst for a thermally activated reaction that cleaves the blocking group from the bulk polymer. The separation of the blocking group makes the exposed region of the resist soluble in the developer. Since the acid is not consumed in the reaction, each acid molecule causes many reactions as it diffuses through the resist, resulting in a photosensitivity gain of 10^2 - 10^3 [10]. Hence, DUV resists belong to a class of materials known as chemically amplified, acid-catalyzed photoresist.

Because of the delay in image formation between exposure and PEB, the DUV resist is vulnerable to airborne and/or substrate contaminants which alter the acid concentration. The contaminants are typically basic compounds that can neutralize the photo-generated acid, thereby inhibiting image formation. An increase in the exposure dose is then required to produce an image, and deformations occur in the developed image profile. In the case of airborne contamination, a lip forms at the top of the developed resist profile, popularly known as "T-topping" [11]. Extreme cases of T-topping cause bridging

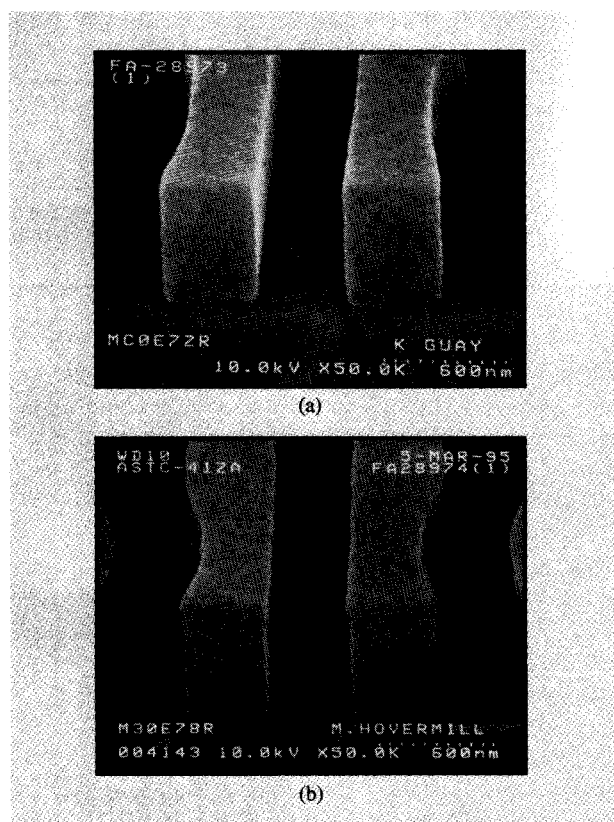


Figure 3

Subtle "T-topping" resulting from low levels of airborne contamination: (a) Uncontaminated resist profiles show straight sidewalls. (b) Low-level contamination causes the formation of a slight lip at the top of the profile.

between adjacent patterns. Even at low contamination levels, the slight T-topping evident by comparing the profiles in **Figures 3(a)** and **3(b)** can cause significant loss of process capability, as is discussed further in the section on process integration. In the case of substrate contamination, an undeveloped foot extends from the base of the profile. As with T-topping, the size of the foot and its effect on the process are dependent on the concentration of contaminant in the substrate contacting the resist and its ability to diffuse into the resist.

Various strategies are used to eliminate the undesired contamination. Given the need to process product with available resists, regardless of their contamination sensitivity, the approach at ASTC has been a combination of chemical air filtration in both the stepper and track tools, use of chemical barrier layers, and tight control of the exposure to PEB delay. As a result, observable effects of contamination have been limited to rare incidents when

basic chemicals were inadvertently introduced to the photocluster enclosure.

The ASTC process has been improved and simplified over time. In the 1991–1992 time frame, when our DUV process was Apex-M resist on the Micrascan® I expose tool, a topcoat layer was required to protect the resist from airborne contaminants. The higher exposure intensity of the Micrascan II tool in late 1992, combined with the availability of Apex-E (which traded photosensitivity for reduced contamination sensitivity) and improved filtration, enabled us to eliminate the need for a topcoat. Where required by the substrate materials, our bottom antireflection layer serves a dual purpose as a chemical barrier. In the meantime, newly available resists such as the IBM/Shibley UV2HS show greatly reduced susceptibility to contamination [12]. This is achieved by the appropriate selection of resist materials to enable a post-apply bake near the glass transition temperature of the bulk polymer. The resulting film densification prior to exposure inhibits the diffusion of contaminants into the resist film [13].

An important consequence of resist contamination was the early resolution of a longstanding debate regarding stepper/track clustering. Our initial experience in 1990 with unclustered DUV tools provided convincing evidence that automated wafer transport between exposure and PEB was required for adequate process control even at 0.5- μ m ground rules. The Micrascan I tools, brought on line in 1991, were directly interfaced with a PEB station. The Micrascan II tools and associated resist process modules, brought on line in late 1992 and early 1993, were configured as fully integrated (antireflection-layer coating through resist development) stepper/track photoclusters.

The stepper/track clustering poses the logistics problem of cascading lots, i.e., initiating a second lot while the first is still in process. (A lot is a set of wafers that receive similar processing.) Without cascading, significant stepper production time is lost while the last wafer of a lot is completed on the track (baked and developed) and the first wafer of the next lot is initiated (coated and baked). Fundamental to cascading is compatibility of process and track configuration from one lot to the next. The successful implementation of cascading at ASTC, where a large and diverse set of products is in process at any given time, has depended on the establishment of a baseline process, with a limited number of product-specific variations. The baseline process must accommodate the requirements of the most advanced product for which there is a significant number of wafer lots. At present, this is the 256Mb DRAM. All products not requiring minimum ground rules are fabricated with the same nominal process, and, consequently, higher process capability. Thanks to this commonality across programs, cascading has improved productivity. Our ability to sustain cascading

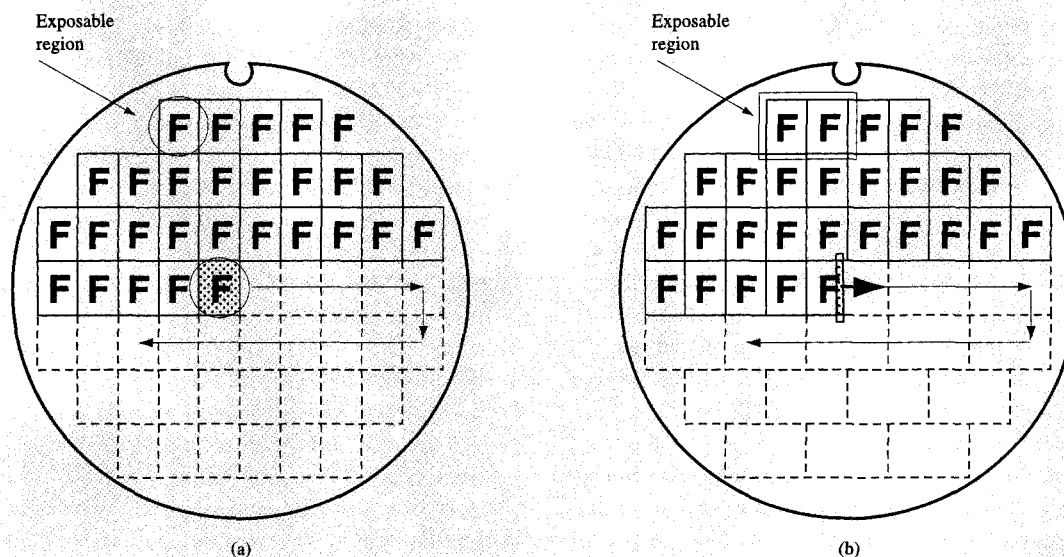


Figure 4

As seen on the wafer, (a) step-and-repeat exposure tools print an entire field (shaded) with each exposure. The achievable field size is limited by the lens diameter. (b) Step-and-scan exposure tools "paint" the field (shaded rectangle) by scanning the reticle and wafer through an imaging slit at each field location. The field size is limited by the slit height in one direction and the scan length in the other.

as new product generations start up will depend on our ability to migrate existing products to a more advanced process.

- *Step-and-scan exposure tool*

Coincident with the need to decrease optical wavelength to keep pace with resolution requirements is a need to decouple resolution and overlay capability from increasing field-size requirements [14]. The chip size growth from one DRAM generation to the next is currently about 50%. For estimates of field size, it is instructive to consider the area required by two chips, a so-called "twin-chip," both to realize productivity advantages in manufacturing and to accommodate the typically larger area of associated logic chips. The 256Mb DRAM generation twin-chip requires a resolution of 0.25 μm and overlay error less than 100 nm over an estimated field size of close to 600 mm² [15]. Given the constraints on optical aberrations implied by such capability, conventional refractive, full-field, step-and-repeat exposure systems become intractable. In anticipation of this field-size requirement, DUV lithography at ASTC migrated from excimer steppers to Hg-lamp-illuminated step-and-scan tools in early 1991. It appears that all tooling manufacturers will adopt step-and-scan technology for the DUV generation of production lithography equipment. To achieve the necessary intensity,

future tooling will contain excimer illuminators, using KrF emission to produce a wavelength of 248 nm and ArF to produce a wavelength of 193 nm.

The step-and-scan system circumvents the field-size versus image-control limitations of the step-and-repeat system by imaging only a section of the field at any given instant of time—much as the step-and-repeat system circumvented the limitations of the earlier scanning systems by imaging only a part of the wafer at a time. From the wafer viewpoint, the differences between the two systems are illustrated in **Figure 4**.

The step-and-repeat system patterns the wafer by moving it in increments of the overall field dimensions, exposing the full field (which must fit within the circular area of the lens) at each stepping location. A shutter between the light source and illumination system controls exposure time, and thus the light energy incident on the wafer, or "dose." The local wafer plane is matched to the image plane of the lens by leveling each field. The distance between the wafer surface and the lens is measured at three or more points, a best-fit plane is interpolated, and the wafer stage is moved (average distance to lens, tilt along two orthogonal axes) to match.

The step-and-scan system must also step the wafer in increments of the overall field dimensions. At each field location, however, the full mask image is "painted" onto

the wafer by scanning mask and wafer simultaneously in opposite directions, through a slit that illuminates and images only a narrow segment of the mask field at any given instant of time. For a reduction system, typically 4:1, the mask must scan four times faster than the wafer. The dose delivered to the wafer is controlled by a combination of illumination intensity and scan speed. The scanned image area is naturally rectangular, resulting in a more efficient match to chip designs than is possible with the circular lenses of step-and-repeat systems. The height of the field is limited by the height of the illuminated slit, defined by the optical system design. In principle, the width of the field is limited only by the length of the scan, defined by allowed reticle and wafer stage travel. In practice, the field width is limited by the size of the mask and the reduction ratio of the optical system. Nonetheless, the step-and-scan system has the intrinsic advantage that larger field sizes can be achieved: to date, field dimensions of $26\text{ mm} \times 33\text{ mm} = 858\text{ mm}^2$, on 4:1 reduction systems using standard 150-mm-square masks. This should be sufficient area to print a 1Gb twin-chip at 0.18- μm ground rules.

Scanning has other major advantages: the minimization of optical aberrations possible over a smaller image area, the inherent averaging of aberrations in the scan direction, and increasing the degrees of freedom for correcting both overlay and image quality over the field. In the latter case, for example, "on-the-fly" wafer leveling during the exposure scan results in a closer match of the wafer plane to the image plane across the field. This is a significant factor in our ability to stay within the smaller DOF that accompanies the more advanced product ground rules.

Of course, the step-and-scan system brings with it the added complexity of synchronized reticle and wafer stage motion during exposure. This is offset to some degree in the SVG Lithography Systems (SVGL) Micrascan design by a simplified, partially reflective optical system allowed by scanning in contrast to the all-refractive lenses in step-and-repeat systems. Nonetheless, on the manufacturing floor more errors can occur with a step-and-scan tool than with the mechanically simpler step-and-repeat tool. Learning to take advantage of the improved capability offered by step-and-scan's greater degrees of freedom, while eliminating its concomitant opportunities for error, has been one of the DUV lithography challenges at ASTC.

• Masks

The products currently fabricated in the DUV sector employ conventional pellicle-protected chrome masks. Various combinations of phase-shift mask and off-axis illumination techniques are being explored [16], but present-generation exposure tools are not well suited to the introduction of these techniques in manufacturing. It

is unlikely that we will see their full implementation until the next generation of exposure tools, equipped with flexible, computer-controlled illuminators, is available in the 1996–1997 time frame.

With more advanced ground rules, even conventional chrome masks must be considered an integral part of the lithography nonlinearities invoked by extending the resolution limits of exposure tools. Optimization of mask bias across the chip becomes a painstaking task, subject to subtleties in both the mask-making and imaging processes.

To date, the mask role of ASTC DUV lithography is principally one of qualification and management. The qualification task scales with the maturity of the product. For early development test sites, a simple visual check for pattern integrity often suffices. For shippable product, of course, stepper lithography brings with it the unenviable characteristic that a single mask defect can destroy every chip on the wafer. The avoidance and early detection of such "repeaters" is a critical responsibility that requires periodic, in-line inspection of the active area pattern on the wafer as well as bit-fail analysis after electrical testing.

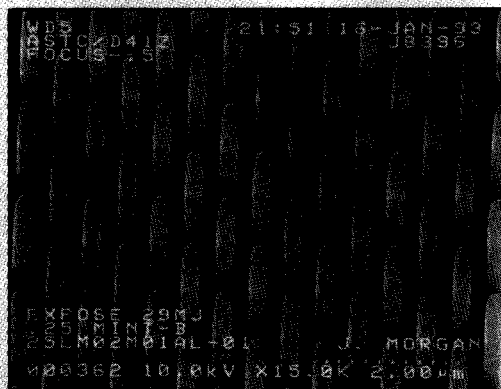
Equally formidable is the need to manage the multiple mask sets that accompany multiple products processed in the same line, and possible multiple mask revisions at any one product level, in a way that ensures the use of the correct mask on each exposure level of each lot being processed in the line. Toward that end, a system that coordinates the assignment of masks, photocluster recipes, and dispositioning specifications to each exposure level has been developed and implemented within the ASTC lithography sector.

Process development

The process development role of the ASTC DUV lithography sector is largely one of extending the limits of the critical dimension and overlay capability, provided by available exposure tool and resist combinations, in the context of early chip development. As noted above, this usually entails working within a small process window for initial product runs, and attempting to enlarge that window as the product matures. A notable recent example has been the implementation of a 0.25- μm process on the Micrascan II photocluster.

• Migration to 0.25 μm

As late as November of 1992, our working assumption was that some combination of phase-shift mask and off-axis illumination technology would be required to realize 0.25- μm lithography capability for early learning on the 256Mb program. Given the embryonic state of the resolution-enhancement techniques, both in mask-making capability and illumination control, this did not bode well for the required conversion to 0.25- μm ground rules. Consequently, with the installation at ASTC of the first



(a)



(b)

Figure 5

Confirming evidence of lithographic capability on the first 0.25- μm ground-rule lot processed at ASTC: (a) Array of elongated resist islands viewed at an angle. (b) Higher-magnification cross-section view of the same array. The distance between islands is 0.25 μm .

Micrascan II (a preproduction model) in December 1992, our first priority was to explore the limits of conventional chrome mask imagery.

The SEM photographs in **Figure 5** are of historical interest in that they show the results from the first integrated lot processed to 0.25- μm ground rules at ASTC, providing early evidence (January 1993) of our ability to produce high-aspect-ratio 0.25- μm images (the space between the resist islands) in Apex-E resist. The corresponding process window is characterized by the critical dimension (CD) variation with dose and focus shown in **Figure 6**. At a single point in the field, we estimated a DOF of 0.8 μm at 8% exposure latitude, assuming our ability to bias the length of the structure to achieve the correct spacing, as shown at the top of **Figure 6**.

The 0.25- μm process window is often limited by the "image-shortening" behavior of the pattern length evident in **Figure 6**. Image shortening belongs to a class of effects which cause pattern deformations as a function of pattern design and density [17]. For a line or space whose nominal length is greater than its nominal width, shortening describes a decrease in the imaged length-to-width aspect ratio. The shortening increases in magnitude as the resolution limit of the lithography tool is approached.

A top-down SEM photograph of the image-shortening effect is shown in **Figure 7(a)**. As the printed linewidth decreases from top to bottom of the photograph, the line ends deviate further from the parallel display cursors. Data showing the dependence of image shortening on the nominal width of both a line and a space are presented in

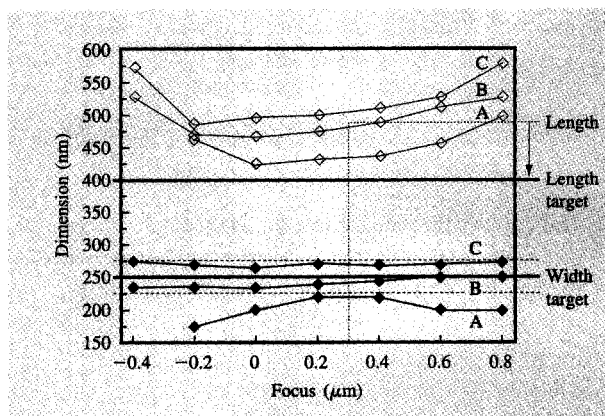


Figure 6

Initial characterization of the focus-exposure characteristics of the space between the resist islands shown in **Figure 5**. The labels A, B, C refer respectively to dose values of 22, 24, and 26 mJ/cm^2 . When the width of an island is exposed to its targeted size (250 nm), the length dimension (separation between adjacent islands) is too large, indicating the need for additional mask bias to compensate for the image shortening of the island pattern. For this process, the resist used was 0.95 μm Apex-E; the antireflection coating was 45 nm Barl-248; and the substrate was silicon.

Figure 7(b). The distance between adjacent patterns was measured rather than the actual length, where the nominal distance is 600 nm. As the nominal width decreases, approaching the resolution limit, the shortening magnitude increases. Several factors contribute to image shortening:

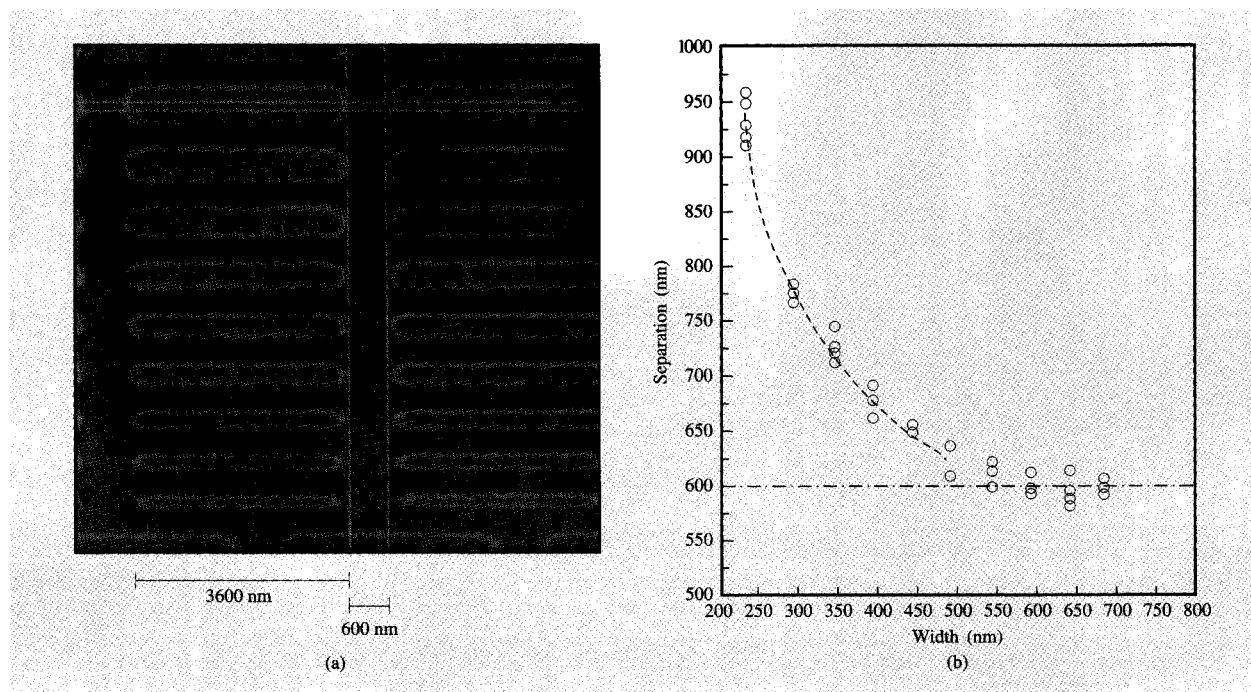


Figure 7

(a) Top-down view of pattern exhibiting increasing line shortening with decreasing nominal linewidth. Nominal separation = 600 nm; nominal length = 3600 nm. (b) Characteristic curve of line shortening.

1. The corners that must form the ends of the line/space contribute higher-spatial-frequency components than the middle of the line/space. The consequent corner rounding leads to shortening in the aerial image as the linewidth decreases.
2. The image-formation components of the resist can diffuse during exposure, PEB, and development steps. This diffusion enhances the shortening as the width of the line/space approaches the diffusion length.
3. The mask contributes to shortening due to the resolution/process limitations (similar to those listed above) inherent in mask fabrication. These effects are most severe for $1\times$ masks, but can also be significant on $4\times$ and $5\times$ masks in the form of corner rounding on the mask pattern, which enhances the shortening present in the aerial image of the lithography tool.

The characterization of mask-to-wafer pattern deformation, under product-specific conditions, including the subsequent etch as well as lithography, is the basis for mask-biasing algorithms to optimize the process window [18]. With correctly biased chrome masks, the 256Mb test site was converted from $0.375\text{-}\mu\text{m}$ to $0.25\text{-}\mu\text{m}$ ground rules by early August 1993. A snapshot of that conversion, as

reflected in critical dimension measurements on a level being processed through the DUV lithography sector, is shown in **Figure 8**. The downward spikes in dimensions prior to the target conversion are precursor experiments at the smaller ground rule. The first significant $0.25\text{-}\mu\text{m}$ electrical test structure yield was obtained in September 1993.

• Alignment improvement

Improvements in level-to-level overlay must be commensurate with reduced ground rules. Overlay performance is usually dominated by the alignment capability of the exposure tool. Consequently, much of the overlay-related development work at ASTC (such as alignment strategy, mark design, and kerf layout) centers on alignment optimization by product level. In the case of DUV lithography, a key component of this activity has been the evaluation and implementation of the AXIOM alignment system on the Micrascan II, as discussed below.

The sole alignment system on early Micrascan II tools was a dual-wavelength (488-nm and 514-nm lines of the Ar-ion laser), direct-reticle-reference, through-the-lens (TTL) system [19]. While direct referencing of the wafer mark to the reticle precludes the possibility of baseline

drift, the narrowband illumination characteristic of TTL laser systems makes them susceptible to process-induced alignment errors. One underlying source of error is optical interference in the neighborhood of the wafer alignment mark. Process variations that are insignificant with respect to product quality can change the optical signature of marks at the alignment wavelength, inducing significant variation in alignment. This process sensitivity on the part of the alignment system results in degradation of both overlay capability and sector productivity, in that it drives a greater use of send-ahead wafers (precursor wafers to establish settings unique to a given lot) to compensate for lot-to-lot alignment variation. Furthermore, it is a particularly insidious problem in that TTL alignment may work well on some product levels but not others.

The AXIOM alignment system was introduced to the field by SVGL in early 1994, as a retrofit to one of our Micrascan II tools at ASTC. In contrast to TTL, AXIOM is a broadband (400- to 700-nm lamp illumination), indirect-reticle-reference, off-axis (outside-the-lens) alignment system [20]. The broadband illumination makes the alignment less sensitive to process variations. Interference effects are averaged out, and alignment signal strength and shape show less variation over a wide range of process structures. On the other hand, the off-axis nature of AXIOM requires that the wafer be referenced to the reticle via a separate calibration mark on the wafer stage. This indirect reference allows the possibility of baseline drift, which can be compensated only by frequent calibration. Thus, the improved process invulnerability of AXIOM comes at the added cost of more frequent reticle-to-wafer reference updates on the Micrascan.

The AXIOM versus TTL trade-offs can be fully evaluated only in an environment such as ASTC, where impact on real product levels can be assessed. Data accumulated across the levels of a common product on two separate Micrascan II tools, nominally identical except that one used TTL alignment and the other AXIOM, are presented in Figure 9. We show the "corrected" alignment offsets of each lot. These are the x , y alignment offsets that, on the basis of modeling of the overlay measurements, should have been used to zero each lot. From the distribution of offsets by level and even within one level, the reduced process sensitivity of AXIOM is apparent. An approximately $2\times$ improvement in level-to-level mean offset control is apparent. The consequent reduction in send-ahead wafers more than makes up for the time expended in the more frequent reticle-to-wafer referencing.

Process control

Process window optimization, dependent as it is on timely advances in materials and tooling, cannot always deliver acceptable exposure and DOF latitudes for pilot line

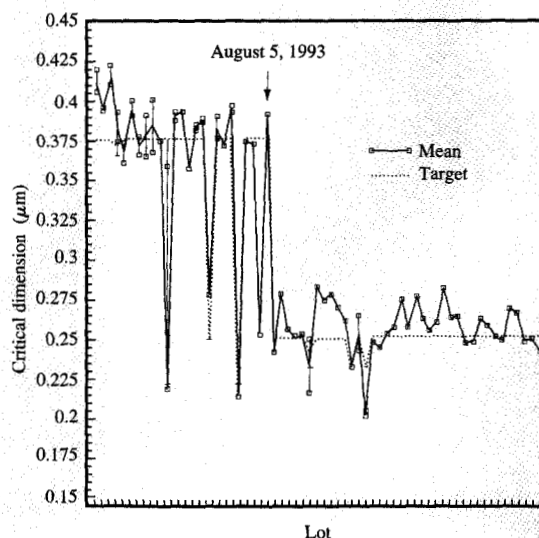


Figure 8

August 5, 1993 transition from 0.375- μm to 0.25- μm ground rule on a representative 256Mb DRAM level at ASTC. Each tick mark indicates one lot.

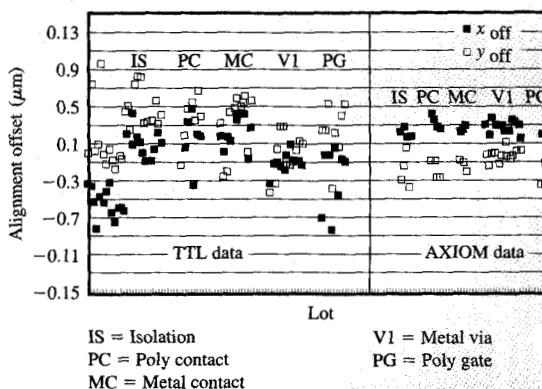


Figure 9

Decreased alignment sensitivity to process of AXIOM compared to TTL, evident in data from an ASTC DRAM product.

production. To ensure our ability to work within very limited latitudes at ASTC, we have invested heavily in process control automation. In particular, sustaining overlay and critical dimension performance requires the frequent updating of both tool baseline settings and those dependent on product, product level, and statistically

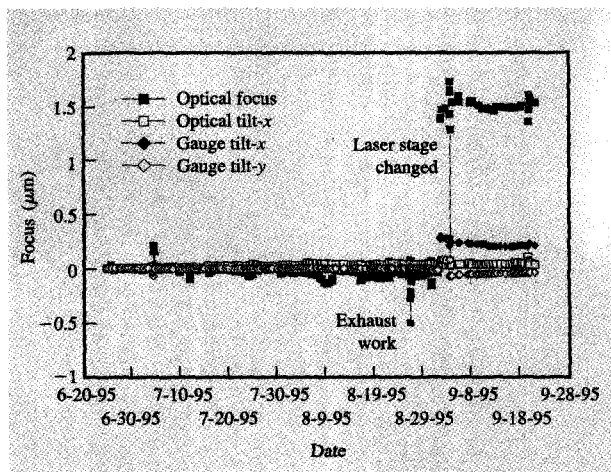


Figure 10

Example of autocalibration focus control. The Autocal system uses both optical and capacitive gauge measurement to monitor focus. Deviations from nominal focus correlate to both transient events, such as exhaust work, and permanent changes, such as a laser stage upgrade.

significant tool/process variation [21]. The operation of the photoclusters must be controlled in four ways:

1. *Tool baseline control* specifies the settings of the tools in the photocluster (stepper and track) independent of product. The settings are based on both *in situ* calibration and the processing of monitor wafers.
2. *Product logistics control* specifies the lots to be run by a given photocluster, and the mask(s), exposure tool product file, and track recipe to be used on a particular lot. Of particular importance to productivity is the identification of lots that can be cascaded. The lot-specific information is typically provided at the time the lot is released to the line.
3. *Product parameter control* specifies the settings for exposure (dose, focus) and the alignment offsets. These settings and offsets are typically tool-, product-, and product-level-dependent. They may be determined by prior lot data or send-ahead wafer data, on the basis of feedback from the metrology sector.
4. *Product statistical process control (SPC)* flags out-of-control conditions using control charts of measurements on product—most notably, critical dimension and overlay data and associated modeled parameters.

For the implementation of *tool control*, we rely heavily on the autocalibration feature (Autocal) of the Micrascan II tool [22]. The Autocal system uses a patterned artifact mounted on the wafer stage to enable the automated

determination of alignment and focus baseline settings. In the alignment case, the alignment system used on product is applied to a set of "ideal" marks on the artifact to zero the baseline offsets and intrafield parameters. As noted above, this becomes an integral part of the AXIOM alignment system because of the need for frequent reticle-to-wafer baseline updates. While the need is less frequent for the direct-reticle-referenced TTL system, Autocal is critical to reticle alignment and overall system maintenance. For focus setup, the Autocal system provides a reference between the absolute focal plane of the artifact, determined by sensing the peak actinic image acuity, and the plane sensed by the capacitive gauges used to maintain lens-to-wafer distance on product.

In both alignment and focus cases, the Autocal system is an *in situ* means of establishing product-independent baseline settings. Thus, it enables the rapid diagnosis of tool changes or instability. A specific focus example is shown in **Figure 10**, in which both the optically determined focus position and tilt-x and the electrically (capacitive gauge) determined tilt-x,y are plotted from one of our tools. The observed changes to the focus are directly traceable to tool changes: A subtle deviation of 0.5 μm occurred in the case where exhaust work was performed, and a dramatic shift of 1.5 μm when the laser stage was upgraded. The Autocal system enabled us to continue to run product with minimal interruption. For the most part, Autocal has eliminated the need to run regular monitor wafers.

On the other hand, *product control* at ASTC relies on bidirectional SECS-II interfaces [23] to both exposure and metrology tools for upload/download of tool settings, measurement, and logistics data. Exposure-tool and process-specific models are employed to predict dose, and alignment settings for each lot in queue at the exposure tool, on the basis of prior lot or send-ahead wafer metrology data. The alignment and exposure of each lot are then executed under host control, following the automated download of the appropriate settings.

Thus, the control of photoclusters while running product requires communication among (a) databases containing the logistics information, (b) the various metrology and exposure tools, and (c) an analysis and database system that stores and transforms measurement data into forms relevant to tool correction and lot dispositioning. The resultant ASTC lithography data system is diagrammed in **Figure 11** and described in the sections that follow.

The physical flow of lots through the photocluster and metrology sectors is shown in the shaded center of **Figure 11**. Where send-ahead wafers are required, they are split off as single-wafer lots. After processing through the photocluster, the patterned wafers proceed to metrology, where the lot is sampled (a subset of exposure fields on a

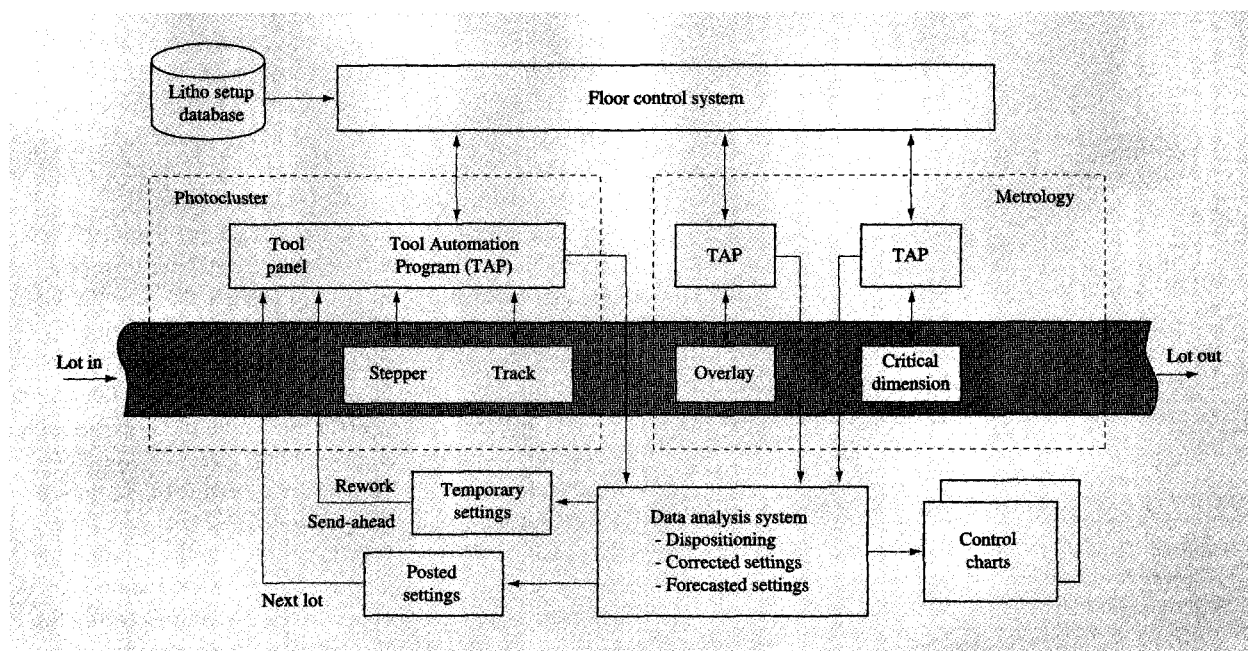


Figure 11

Block diagram of ASTC lithography product control system.

subset of wafers) for critical dimension and overlay performance relative to predetermined specifications. If the analyzed results are within specification, the lot is shipped to the next sector. If specifications are not met, the lot is reworked.

The surrounding flow of information among various systems and databases is designed to sustain and control the movement of lots, such that the quality of the output is ensured and the rework rate, use of send-ahead wafers, and overall transit time of the lots are minimized. In the photocluster, logistics data, from an in-house IBM software system called Floorworks, are merged with parametric data fed back from the metrology sector, via an IBM data analysis system called ASTEC. The complementary logistics and parametric data for a given lot come together at the stepper's Tool Automation Program (TAP), an IBM tool-specific communication and supervisory control program, which downloads the settings to the tool and initiates the processing of the lot.

At the start of tool processing, Floorworks transmits the lot, mask, and process data to the tool's controller, and logs the lot onto the tool. In its final step, Floorworks initiates the TAP communications channel between the tool's hardware controller and Floorworks. The TAP handles requests for data and/or function from either the tool or Floorworks, and transmits the sequence of messages to the tool that achieves the desired result. In

the case of the lithography sector, it also provides an interface between the data analysis system and the tool. For the metrology tools, it enables measurement data transfer to ASTEC for lot and/or wafer dispositioning (a pass/fail decision on lithographic quality). Part of the dispositioning process is to determine settings for future lots and wafers. The TAP then enables the feedback of overlay- and critical-dimension-performance-related tool settings on a per-lot basis.

ASTEC was built at ASTC within the environment of a commercially available statistical package (SAS®). ASTEC contains our modeling and lot-dispositioning algorithms, specification tables, and a summary database. In addition, it provides a rich environment for data review and engineering diagnostics. ASTEC resides both in the LAN OS/2® environment, for real-time interaction with lots as they move through the lithography sector, and in the mainframe MVS environment, for archival data analysis. This commonality across different platforms provides advantages in the speed with which problems can be resolved and data analysis improvements can be implemented on the production floor.

Lot and wafer dispositioning is the principal real-time function of ASTEC in the lithography sector. A flowchart of the dispositioning process is shown in Figure 12. After the CD and/or overlay data are imported via the metrology tool TAPs, the system selects specifications and

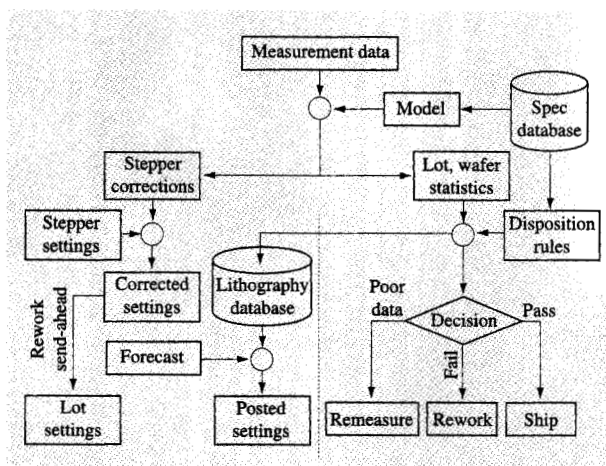


Figure 12

Flowchart of product dispositioning: The left side automates the feedback corrections for the exposure tool, and the right side automates the lot movement decision.

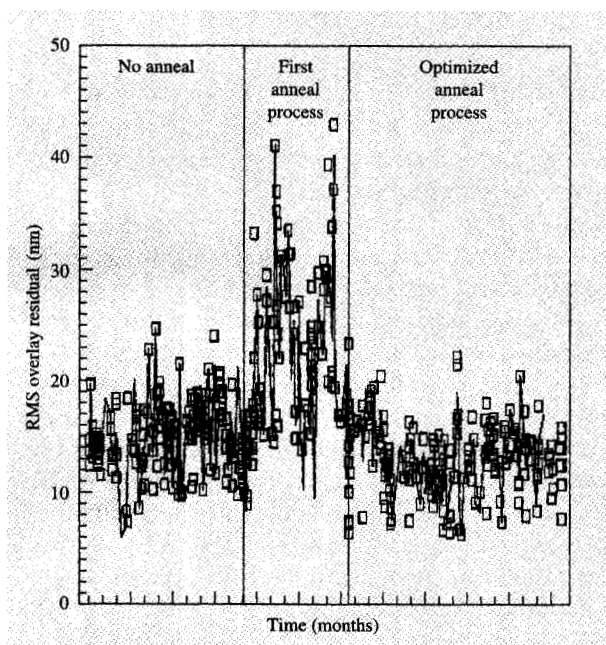


Figure 13

Impact of rapid thermal annealing on downstream lithography sector over an 11-month period.

process models specific to the product, level, and operation. The data analysis then computes the appropriate statistics and modeled parameters, which are compared to the specifications. Analysis reports are

prepared by sampled wafer and by lot, photocluster-specific SPC charts are updated to establish whether or not the lithography process at that photocluster is in control, and the dispositioning actions pertinent to the particular lot are recommended to the operator.

Regardless of the ship/rework decision, an additional function is performed by ASTEC at the time of dispositioning, as shown on the left side of Figure 12. Via the stepper TAP, ASTEC obtains the stepper dose and the alignment settings that were used at the time the lot was exposed. The models applied to the data during dispositioning determine the dose and alignment corrections that must be applied to minimize CD deviation from target and overlay error. Summing the dispositioning corrections with the stepper settings gives the so-called corrected settings that should have been used. In the case where a send-ahead wafer is used, or a lot is reworked, these corrected settings become the settings for exposing the lot. In the case where send-ahead wafers are not used, the trends apparent in the corrected settings become the basis for forecasting the tool settings for the next lot at that product and level. In this manner, ASTEC is able to feed back tool settings for lots that are at the tool or feed forward settings for lots to be processed by the tool in the future.

Process integration

The overall process has a profound impact on lithography requirements. For a given product, the lithographic process window must be consistent with the variations introduced in the rest of the process. For example, a key factor in extending the life of current photolithography generations has been the improvement of overall process planarity through the use of chemical-mechanical polish (CMP), relieving pressure on the shrinking DOF apparent in Figure 2.

Establishment of consistency throughout a product routing is the role of process integration. From the lithography viewpoint, process integration bridges lithography to upstream and downstream sectors in a product routing. While in-line measurements usually ensure self-consistent optimization within the lithography sector as described in the previous section, optimization between sectors cannot always be ensured.

One example of the unforeseen effect of an upstream process on lithography over an 11-month period is shown in Figure 13. A change to an anneal process caused an observable increase in the uncorrectable or "residual" overlay errors at subsequent lithography steps. A significant decrease in overlay capability resulted, even though lithography continued to optimize overlay by all available means. Ultimately, the cause of the problem was traced to wafer deformation introduced by the anneal step [24]. Owing to the terrain-following focus system of the

Micrascan, the effect on imagery performance was not readily apparent. The overlay residuals, however, proved a sensitive indicator of local wafer planarity. Using them as a diagnostic tool, the anneal process was then readjusted to meet both the product and lithography requirements.

Similarly, lithography process deviations can cause problems in downstream process sectors. Subtle variations in the resist profile shown in Figure 3, below the detection limit of in-line metrology, may be amplified by subsequent etch processes [25]. Figure 14 illustrates the effect of resist poisoning on two critical levels. In both cases in-line SPC charts indicated that the resist image sizes were in control, while there was an overall reduction in the process capability of the final etched image size. An unbalanced ANOVA (analysis of variation, where "unbalanced" refers to the fact that unequal numbers of lots were processed through the various tools in question) indicated that the lithography tools were a significant contributor to the overall variability in the process. It was found that a low level of alkaline material had been introduced during maintenance activity on one of the steppers, resulting in a slow poisoning of the resist over time.

Figure 14(a) shows the relationship between the gate length of a typical product measured in resist and measured after etch over a 12-month period. During the "poisoned" time frame, the etched image was consistently larger than the resist image. Providing a slightly different view of the same problem, Figure 14(b) shows the difference between the etched image size and the resist image size (bias) for a deep-trench process. The gradual degradation in profile is reflected in the downward trend in bias in the "poisoned" time frame. In both cases, the bias returned to nominal values after tool cleanup and filter replacement. The resist image size, as measured by top-down SEM, remained relatively constant throughout.

The above examples illustrate our approach to integration within ASTC. In both cases, the application of SPC to in-line measurements automatically flagged an out-of-control condition. Each flag initiated an investigation to determine and fix the basic cause of the problem.

Capability

Process capability is the performance of key process parameters against specifications established to ensure product quality, as embodied in the capability indices C_p , C_{pk} [26]. The capability index C_p is defined as the ratio of a wafer lot's specification width, $|USL - LSL|$, to the distribution width, 6σ (σ = standard deviation), where USL and LSL are the wafer lot's upper and lower specification limits, respectively. C_{pk} includes the effect of the difference between the mean and a design value. For lithography, the primary parameters are critical dimension and overlay. Representative control charts and capability

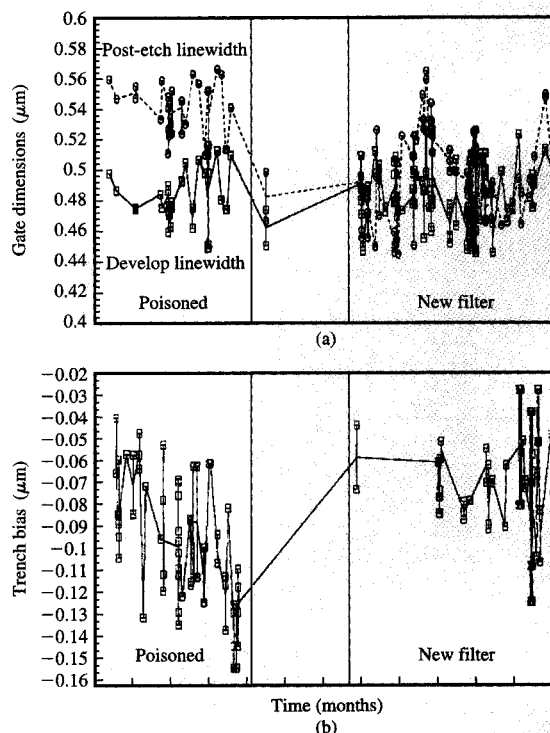


Figure 14

Resist poisoning impact on downstream etch sector: (a) Relationship between the gate length of a typical product measured in resist and measured after etch. (b) Difference (bias) between the etched image size and the resist image size for a deep-trench process over a 12-month period.

indices of integrated lots outgated from the DUV lithography sector for a 0.25-μm ground-rule level are shown in Figure 15. The mean + 3σ variation of critical dimension is less than 45 nm, and that of the X-overlay is less than 60 nm over the 44 lots shown.

This performance is not possible without the dynamic control of tool settings described in the process control section, as is shown by the trends of associated tool parameters for the same level over the same period of time. Among the three photoclusters in use, the forecasted values of dose, the principal driver of the critical dimension, and X-offset, the principal driver of the X-overlay, are presented in Figure 16. In other words, Figure 16 shows how the tool parameters were adjusted, on the basis of lot-dispositioning data, to achieve the capability illustrated in Figure 15. Significant differences among the tools as well as variation over time for a given tool were tracked. Our ability to sustain the in-control operation

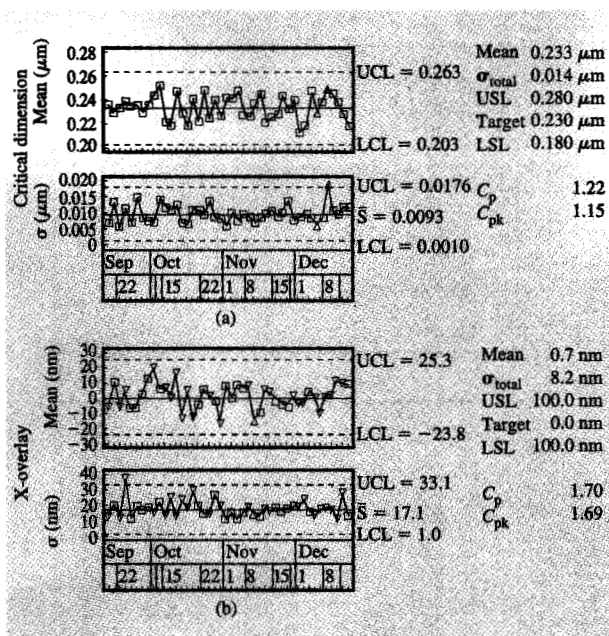


Figure 15

Representative control charts and capability indices of integrated lots outgated from the DUV lithography sector for a 0.25- μm ground-rule level: (a) Critical dimension. (b) X-overlay. σ represents within-lot variations; σ_{total} represents both within-lot and lot-to-lot variations. $\bar{\sigma}$ is the mean of all σ values. UCL and LCL are upper and lower control limits; USL and LSL are upper and lower specification limits. $\square$, nominal sampling plan; ∇ , missing data points; $\triangle$, more points than in nominal sampling plan.

shown in Figure 15 demonstrates the efficacy of our feedback control system.

Given the diverse product mix at ASTC, key indicators of this form of lithography capability (and detractors from productivity) are rework and send-ahead wafers. When product variation exceeds lithography capability, send-ahead wafers are required to preclude rework. Our objective has been to keep rework at an acceptably low level while reducing the need for send-ahead wafers. Our ability to improve is apparent in Figure 17. However, the complete elimination of send-ahead wafers is unlikely in a pilot line environment. Their use is economically justified when lot-to-lot variation in tool settings dominates. In these situations, the cost of added rework exceeds the cost of running send-ahead wafers to preclude rework.

In running without send-ahead wafers, the data from prior lots must predict the alignment and exposure conditions for future lots. The automated forecast algorithm employed in ASTEC is based on a vintage-weighted average of the last n lots. The analysis is conducted, and the posted settings for a particular product

level are updated as each lot is dispositioned. The success of forecasting is dependent on the stability of the tools, the maturity of the process, the number of lots processed and continuity of work for a given product, and, to a lesser degree, the specifications that must be achieved. Adiabatic trends in tool settings can be tracked successfully, whereas lot-to-lot fluctuations cannot. The magnitude of lot-to-lot fluctuations relative to the specifications will determine the level of rework incurred.

Productivity

DUV productivity must be viewed in the context of the ASTC pilot production mission and the leading-edge capability of DUV lithography. Only a small fraction of the ASTC capacity is devoted to what could be called

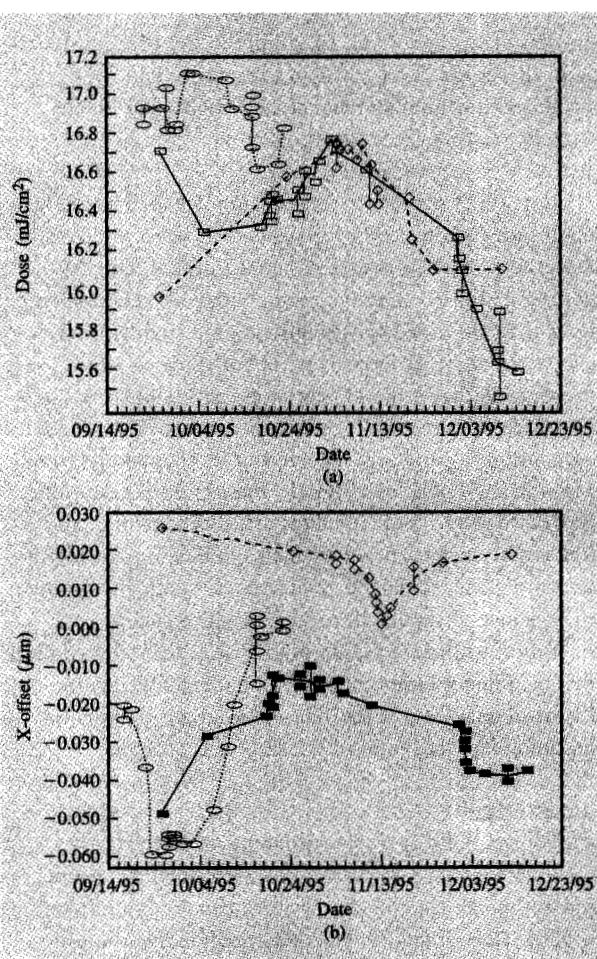


Figure 16

Forecasted tool settings among three photoclusters (boxes, ovals, diamonds) at the same 0.25- μm level as shown in Figure 15: (a) Dose. (b) Post-alignment correction in X (X-offset).

manufacturing—namely, integrated lots free of process splits. Most of the ASTC capacity is consumed by development lots: approximately half integrated (a complete process routing through to electrical test) and half engineering experiments (deviated routings, short loop test runs, etc.). Since nearly all of the so-called critical levels, those having the most advanced ground rules, are patterned by DUV, the DUV lithography sector sees the preponderance of process splits, early development lots, deviated routings, and engineering experiments.

For an ASTC process sector, such as DUV lithography, productivity encompasses a set of specific measurements. Most notable among these are number of lots processed successfully (lot outgates) per photocluster, which we want to maximize, and time to process a lot (cycle time or turnaround time) through the sector, which we want to minimize. The two must be considered simultaneously to obtain a true picture of productivity. For a fixed photocluster throughput, outgates are maximized by ensuring sufficient lots in the queue that the tools are never idle; however, by definition, queued lots cannot achieve the minimum cycle time. Thus, as the throughput is increased, productivity improvement requires a balance between effective throughput and the amount of product at the tool. Our progress in productivity improvement over an approximately three-year period is summarized in **Figure 18**, where we show the lot outgates and turnaround time (TAT) trends, normalized to their values in the first month. Over the period shown, lot outgates have increased by 3.5 times as TAT has decreased by 2.5 times. The fluctuations in the two curves, most evident in TAT, signify instances of imbalance between capacity and loading in the DUV lithography sector. That balance is especially difficult to maintain in a pilot line environment. Nonetheless, the overriding trends are encouraging, particularly when the coincident decrease of ground rules shown in Figure 1 is considered.

The productivity gains of Figure 18 took place during a period of relative stability in DUV lithography. Over that two-year period, the photoclusters at ASTC had a common configuration and similar capability. Productivity improvement could become the focus of engineering activity once the prerequisite phases of process development, control, and integration had coalesced into a capable DUV process.

Summary

We have described the diverse activities of a lithography operation in a pilot line production environment. The overview and examples reveal the underlying structure of the ASTC DUV lithography sector. At present, step-and-scan 248-nm exposure tools and chemically amplified resists are the basic constituents of our process. Attention

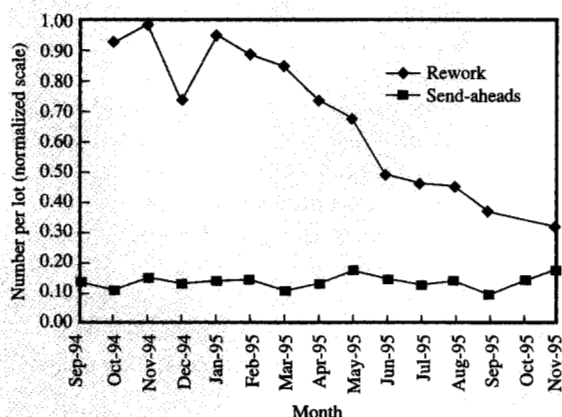


Figure 17

Trends in rework and send-ahead wafers for all DUV lithography products at ASTC.

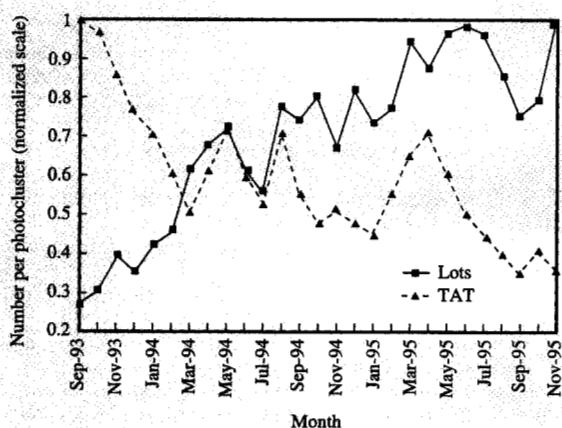


Figure 18

Trends in lot outgates and turnaround time (TAT) for all DUV lithography products at ASTC.

to integration and process control has enabled us to increase the productivity of our 248-nm process, even as ground rules shrink. Projections of chip density indicate that DUV photolithography at ASTC must migrate from 248-nm to 193-nm exposure wavelengths in the near future. Thus, our efforts to improve DUV lithography remain critical to our continued success in developing semiconductor products.

Acknowledgment

The broad scope of work described in this paper, undertaken over a period of more than five years, has had many participants. We especially wish to recognize our current and former colleagues in the ASTC and SRDC lithography projects. While we have attempted to present the ASTC lithography perspective, it is often impossible to separate lithography activities from those of related process sectors, systems support, and product integration teams—all of whom have been partners in the progress demonstrated. Furthermore, many valued colleagues have been employees of Siemens and Toshiba during this period. We acknowledge our indebtedness to them for their contributions.

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OS/2 is a registered trademark of International Business Machines Corporation.

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