

Charge-metering sampling circuits and their applications

by E. S. Schlig

Charge-metering sampling circuits comprise a new CMOS circuit class for sampled analog data applications. They avoid some drawbacks of conventional sampling circuits without the use of operational amplifiers. They lightly load their inputs, may be cascaded without buffering to provide analog pipelining, and avoid charge injection errors. Application to linear and nonlinear digital-to-analog converters (DACs), particularly for active matrix display data line drivers, is detailed. In the display application, the nonlinear charge-metering DACs provide a predetermined nonlinear relationship between digital input and display luminance down to the least significant bit, avoiding compromising color reproduction by the use of a piecewise-linear response. Experimental verification of this new circuit class has included the design and fabrication of a cross section of an integrated CMOS six-bit digital-analog data line driver. Experimental results are presented.

Introduction

Charge-metering sampling circuits are a new CMOS circuit class for sampled analog data applications. They

are distinguished by the transfer of measured amounts of charge to or from a capacitor under the control of a MOSFET (or MOSFETs) operating in the saturation region. They were originally conceived as a way to overcome the well-known limitations of the conventional CMOS sampling switch without the use of operational amplifiers, particularly in digital data line driver circuits for active matrix display panels [1]. Among the applications that have been explored are analog sampling, linear and nonlinear digital-to-analog conversion, analog buffering, charge summing, dc level setting, and correlated double sampling. The operation and advantages of charge-metering circuits have been verified by design studies, simulation, and by designing, fabricating, and operating experimental CMOS chips.

A charge-metering circuit reduced to its bare essentials is shown in **Figure 1**. An n-FET, by way of example, has its source connected to a capacitor and its drain connected to a voltage source V_D which is sufficient to keep the transistor in its saturation region. An input signal is applied to the gate. With the input in an initial state, a precharging circuit (not shown here) charges the capacitor to a sufficiently negative voltage to turn on the transistor. The precharging circuit is turned off and the capacitor voltage rises because of conduction through the transistor. When the gate-to-source voltage falls to the transistor threshold voltage, the transistor cuts off. At this time, the

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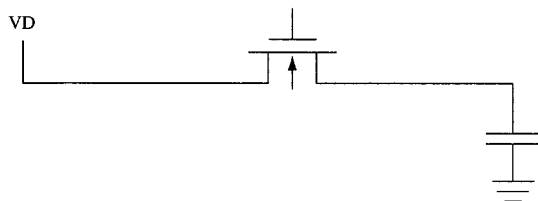


Figure 1

Rudimentary charge-metering sampling circuit.

capacitor voltage is equal to the gate voltage less the threshold voltage. A positive change in the input voltage applied to the gate will cause further negative charge to be spilled from the capacitor, so the capacitor voltage follows the input. When the positive step in gate voltage is applied, the transistor turns on and conducts a current from the drain to the capacitor. Using the familiar strong inversion drain current equation, and assuming that the drain voltage is approximately constant (or that the channel length is approximately independent of the drain voltage),

$$i = \frac{KW}{2L} v^2,$$

where K is the transistor's normalized transconductance, W is its channel width, and L is its channel length. The voltage v is the gate-to-source voltage minus the transistor threshold voltage. Since the gate voltage and (to a first approximation) the threshold voltage are constant after the step, v mirrors the capacitor voltage and is a convenient variable for this analysis. Current i charges the capacitor, increasing the source voltage and reducing v from its initial value after the step, V_i :

$$v = V_i - \frac{1}{C} \int_0^t i d\tau,$$

$$v = V_i - \frac{KW}{2LC} \int_0^t v^2 d\tau,$$

where C is the capacitance and t is time. Differentiating, we obtain a differential equation for v :

$$\frac{dv}{dt} = -\frac{KW}{2LC} v^2.$$

Solving for v ,

$$v = \frac{V_i}{\frac{KWV_i}{2LC} t + 1}. \quad (1)$$

Since $2L/KWV_i$ has the dimensions of a transistor channel resistance, $2LC/KWV_i$ represents a time constant.

The response represented by Equation (1) consists of a rapid initial voltage change followed by a slow tail, approaching $v = 0$. This result is useful for initial design studies, but the design must be refined by simulations using a detailed MOSFET model. As the MOSFET approaches cutoff, the strong inversion analysis used above becomes invalid because diffusion current becomes important. A given final voltage is reached faster than the simple model predicts, and the capacitor voltage continues to change after nominal cutoff is reached because of subthreshold conduction, which must be accounted for in the design and in clock timing.

Returning to Equation (1), the time t_f required for v to decay to a final value v_f (neglecting diffusion current) is

$$t_f = \frac{2LC}{KWv_f} \left(1 - \frac{v_f}{V_i} \right).$$

A simple physical interpretation of this result is the difference between the initial and final values of the product of the channel resistance and the load capacitance as the channel charge decays. The final value of v is related to the required precision and accuracy. When v_f is small compared to V_i , the time required is approximately independent of the initial voltage step V_i , depending mainly upon v_f , C , and the MOSFET technology and dimensions. In terms of our physical interpretation, the approximate required time is equal to the product of the final channel resistance and the load capacitance.

As a broadly generalized comparison between charge-metering circuits and CMOS sampling switches, the former require larger channel widths to achieve the same speed but avoid the use of operational amplifiers in applications that would otherwise require them for the same functionality and accuracy.

Attributes of charge-metering circuits

Charge-metering circuits as a class have the following important attributes:

- The input is applied to a MOSFET gate electrode and thus is not loaded by the load capacitance. Similarly, stages may be cascaded without loading each other or sharing charge. This contrasts with the conventional sampling switch, in which the sampling capacitor is charged by the input signal unless buffering is provided.
- The charge-metering MOSFET operates close to cutoff in equilibrium, so that there is very little mobile charge

in its channel to produce charge injection errors. In conventional sampling switches, at turnoff part of the mobile channel charge is injected into the sampling capacitor. In high-speed applications, the channel is large and the sampling capacitor is small, so the injected channel charge can cause significant signal-dependent errors. These are normally avoided by the use of dummy switches and operational amplifiers to cancel the error [2].

- The conventional sampling switch also introduces an error by coupling the sampling pulse to the output through the gate-drain capacitance. Charge-metering circuits can use a sampling pulse applied to the source, which couples less strongly to the output.
- In charge-metering circuits, the final output is virtually independent of absolute component values.
- They have no quiescent current or power dissipation.
- The capacitors they require have a common terminal at a fixed potential. In typical practice the common terminal is the silicon substrate, the active terminal is a polysilicon gate, and the dielectric is the thin gate oxide. This provides a high area density of capacitance, which may be further enhanced by providing a second, top common electrode formed by a second polysilicon layer.
- In a track-and-hold mode of operation, they require a monotonically changing input. This is a limitation compared to conventional circuits, but there remains a broad class of amenable applications, notably those employing tracking and holding ramp or staircase waveforms. However, charge-metering does not compete effectively in very high bandwidth sampling of arbitrary analog signals.
- They are capable of summing samples obtained sequentially or simultaneously from one or multiple signal sources.

Charge-metering circuits are inevitably compared to charge-coupled devices (CCD) and bucket-brigade devices (BBD). They are distinguished from both by the fact that stages are coupled by voltage, not charge. They are further distinguished from CCD in that signal charge resides in the polysilicon capacitor plates rather than in the silicon substrate, and in that they may be, and in fact have been, built from discrete components. They are further distinguished from BBD in that their input is to a gate rather than a source, and they do not require capacitive coupling from gate to drain for their operation.

Inverting charge-metering circuits

In inverting charge-metering circuits, the charge transferred from the capacitor of Figure 1, caused by a change in input voltage applied to the gate, is collected by a second capacitor in the drain circuit. The voltage change on the second capacitor is the circuit output. Since a

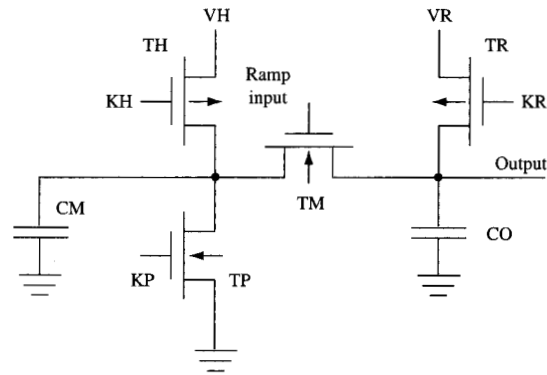


Figure 2

Practical inverting charge-metering circuit.

change in the input voltage is required, the inverting circuit inherently operates as a track-and-hold. Inversion is an unusual attribute for a sampling circuit. This circuit preserves the integrity of the input by fixing the initial output voltage at a value equal to a reference voltage source and by having a gain precisely determined by the ratio of the values of two integrated capacitors. This operation may be seen as a form of correlated double sampling.

A practical inverting circuit configuration is shown in **Figure 2**. Using an n-FET as the charge-metering transistor TM, the circuit of Figure 2 produces a negative-going output change in response to a positive input change. For a negative-going input, a p-FET charge-metering transistor would be used, with corresponding changes in the other MOSFETs and the signal and voltage levels. **Figure 3** shows a timing and waveform diagram for the circuit of Figure 2 as applied to tracking and holding a monotonic nonlinear ramp or staircase waveform of the sort used in a nonlinear DAC in the display data driver circuit application [1] which is detailed later in the paper.

At the start of an operating cycle the ramp, which is applied to the gate of n-FET TM, is at its initial low level, which is above the TM threshold voltage. Since the ramp is applied only to the gate electrode, it sees a moderate and relatively constant load. Initially, n-FET TP, p-FET TH, and p-FET TR are off. KP rises at time T1 to precharge capacitor CM through TP to ground potential. CO will also receive negative charge. KP falls to turn TP off and KR falls to turn on TR at T2. While TR is on, CO charges to high potential VR and CM spills charge through TM until its voltage rises to equilibrium with the channel potential of TM, which is below the initial level of

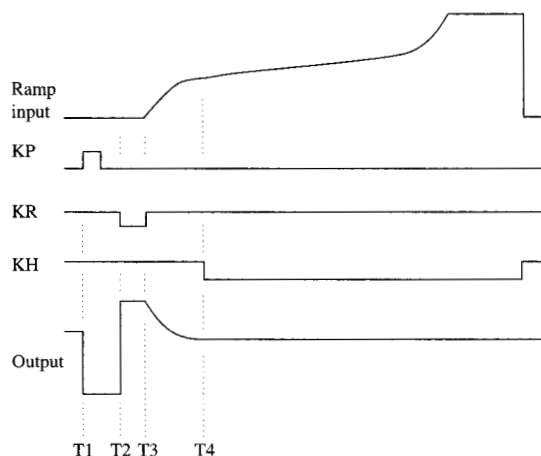


Figure 3

Waveform and timing diagram for the circuit of Figure 2.

the ramp input by the threshold voltage of TM. The charge spilled from CM is absorbed by the VR source, so the voltage across CO remains at VR. VR is large enough that TM is pinched off, in other words in its saturation region, throughout its range of operation. At T3 KR rises to turn TR off and the ramp begins to rise. A step in voltage with an amplitude of about 30 mV at the start of the ramp avoids the small output nonlinearity that would otherwise result from subthreshold current flowing through TM1 during the time that TR1 was turned on.

As the ramp rises, negative charge is transferred from CM to CO, reducing the output voltage across CO accordingly so that the output tracks the input in inverted sense. Since the size of TM is chosen so that it operates very near cutoff during the rise of the ramp, there is little mobile charge in the channel. The value of VR is high enough that TM remains pinched off as its gate voltage rises and its drain voltage falls. The ratio of the voltage change across CO to the input voltage change is the gain, which is approximately $-C_M/C_O$. The gain may be very accurately established through inherent tracking of the values of closely spaced capacitors in a semiconductor chip, particularly when they are designed with a common centroid. The gain will be taken here as -1 for clarity and convenience.

The requirement that TM operate in its saturation region implies that VR must be at least the sum of the highest input ramp voltage and the output voltage range. An advantage of higher gains is that the input ramp amplitude is smaller so VR may be lower.

T4 marks the end of the time interval corresponding to the tracking mode. At T4, the hold mode is initiated by dropping KH, which turns on TH to charge CM to high potential VH so that TM turns off hard, even though the ramp may continue to rise. Thus, the voltage across CO at time T4 is held until the end of the operating cycle.

Since TM is turned off by raising its source voltage instead of lowering its gate voltage, and because there is little residual mobile charge in its channel when it is turned off, the charge injection error inherent in the usual type of sampling switch is avoided. Also, since the output is determined by the change in the channel potential rather than its absolute value, there is no error due to threshold voltage tolerance. Body effect in TM influences the stage gain slightly, but this contribution is minimal if the source voltage of TM is kept at least a volt above the substrate. This effect has been found empirically to be essentially constant even among wafer runs, and so may be compensated by the capacitance ratio. It is conceivable that the changing drain voltage of TM during tracking of the input might influence gain by affecting the threshold, particularly if the TM channel is short and VR is large. We have not tried to separate out any such influence on gain and have observed no nonlinearity attributable to it.

TH is turned off by raising KH before the beginning of the next operating cycle.

The ramp input is coupled to the output terminal through the gate-to-drain capacitance, potentially introducing an error. The error would be small due to capacitive attenuation, and independent of the sampling point because there is no back conduction path from the drain to the source of TM in either the track mode or the hold mode. More significantly, when the ramp voltage returns to its original value at the end of the operating cycle, as shown in Figure 3, the net coupled voltage is virtually zero. This also is true because there is no back conduction path from the drain to the source.

It is sometimes useful to have a step in the output equal to the difference between VR and the held output. This can be obtained at the end of the operating cycle by lowering KR to turn on TR, restoring the output voltage to VR.

It is clear that because output capacitor CO must track CM for good control of the gain, the inverting charge-metering circuit is not suited to driving directly remote loads with substantial capacitance relative to CO. The noninverting charge-metering circuit, to be described next, is an effective buffer between the inverting circuit and a remote capacitive load. This two-stage configuration has been found to be the most generally useful.

Noninverting charge-metering circuits

In noninverting circuits, the only capacitor used is the output capacitor CO. The gain is approximately $+1$, reduced slightly by body effect, which is minimal when the

output voltage range is well above the substrate voltage, and which varies little from chip to chip, as has been noted above. The output dc level does vary with the threshold voltage of the charge-metering transistor in the noninverting circuits. Correction of this dependency is discussed below. The noninverting circuit can either sample a fixed input voltage or track an input voltage change.

A practical noninverting circuit is shown in **Figure 4**. The output is taken across capacitor CO. Charge is metered from CO by charge-metering n-FET TM and collected by voltage supply VH, which is large enough to keep TM in its saturation region throughout its operating range. The load capacitance CO does not contribute to the gain in this case, so it may be the capacitance of a remote load.

Initially the input to the gate of TM is at some level above the threshold of TM. KP rises to turn on the n-FET TP, precharging CO toward ground. Then KP falls to turn off TP. CO discharges through TM until its voltage is in equilibrium with the channel potential of TM. Charge spilled through TM is collected by VH. The output voltage across CO at equilibrium represents the initial input minus the threshold voltage of TM. Any positive change in the input produces an approximately equal output change. If the circuit is required to follow negative input changes, TM becomes a p-FET, and corresponding changes are made to TP and signal and voltage levels.

Figure 5 shows a practical two-stage charge-metering circuit as used in our experimental D/A converters, which are described below. The first stage is an inverting ramp sampler, as described above. The second stage is noninverting; it samples the output of the first stage at the time of completion of the ramp input.

The addition of CMOS series switch TS2 to the second stage, as shown in **Figure 5**, is often useful. Turned off before TP2 turns on and then turned on after TP2 turns off, it avoids direct conduction between VH2 and ground when TP2 is on. It also can isolate the load capacitance from TM2, so the gate input to TM2 can change without affecting the output. This provides for analog pipelining, permitting previous stages to operate on the next datum while the output of the previous operation is held constant. This is important in the display data line driver application. The dimensions of TS2 must be small enough to avoid significant charge-injection errors when it turns off.

It has been stated that the output of a noninverting stage has a dc level which depends upon the threshold voltage of TM2. In the common case having an inverting charge-metering stage precede the noninverting stage, that dependency may be corrected by generating the voltage VR1 used in the inverting stage with an on-chip circuit that makes VR1 vary directly with MOSFET threshold voltage. This may be done on a circuit-by-circuit basis, by

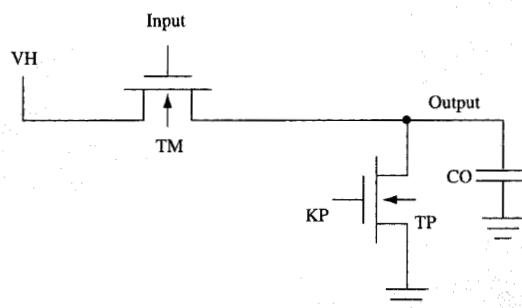


Figure 4

Practical noninverting charge-metering circuit.

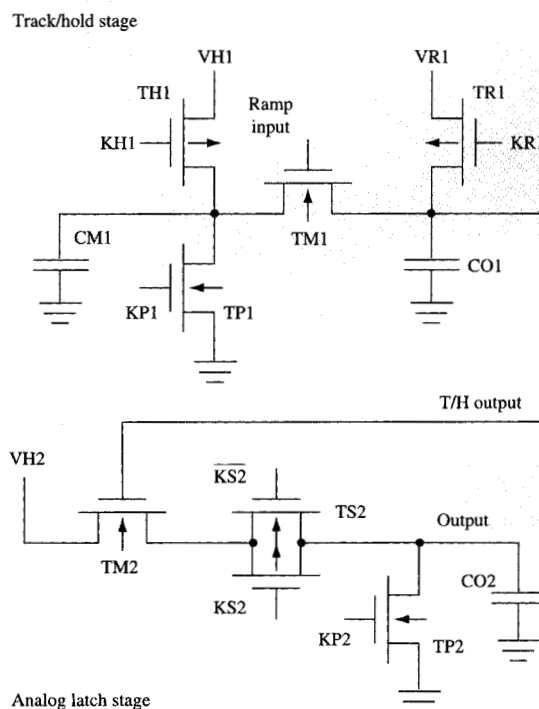


Figure 5

Two-stage charge-metering circuit with analog pipelining, for the nonlinear sampled-staircase DAC application.

groups of circuits on each chip, or on a chip-by-chip basis. Most of the variability in threshold voltage is that from chip to chip, which is typically hundreds of millivolts compared to tens of millivolts within a chip.

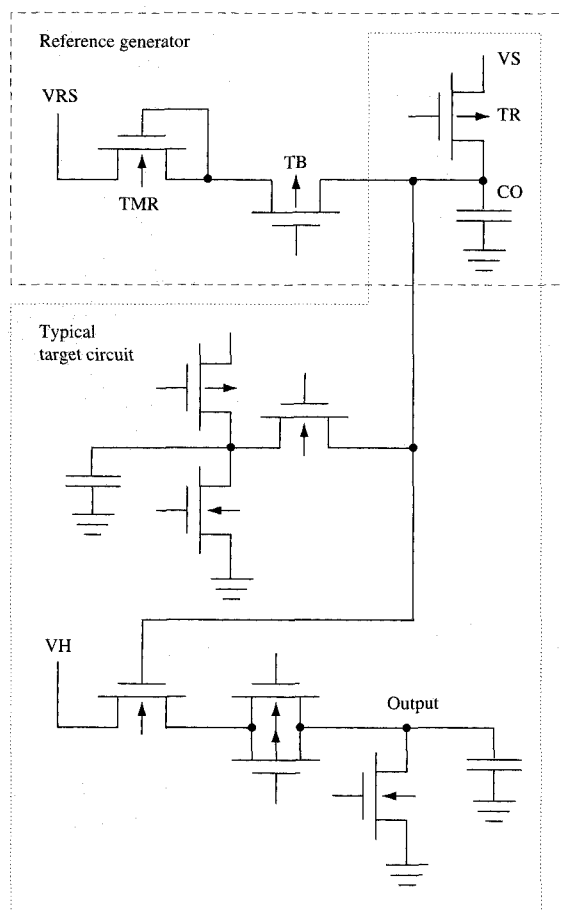


Figure 6

Threshold-correcting reference voltage generator serving a single target circuit.

Liquid crystal displays are driven by an alternating voltage relative to their counter electrode, and their luminance is controlled by the rms value of that voltage. The rms value is sensitive to the peak-to-peak amplitude of the voltage, but much less sensitive to its dc component. The threshold variability contributes only to the dc component. Thus, depending upon the required precision, the tens of millivolts variability in the dc component introduced by the threshold variability within a chip may not be detrimental. On the other hand, detrimental effects such as image sticking are caused by larger dc components, so the hundreds of millivolts variability in dc component from chip to chip needs correction. In our experimental display data line driver circuits, we derive VR1 with a single on-chip threshold compensating voltage source, and distribute it to all data

line drivers on the chip. This voltage source is also a form of charge-metering circuit.

Compensating reference voltage generator

Figure 6 shows a threshold-compensating reference voltage generator circuit which serves a single charge-metering target circuit. The target circuit consists of an inverting stage followed by a noninverting output stage. The function of the reference generator is to cause the dc level of the output of the first stage of the target circuit to vary directly with threshold voltage, canceling the inverse dependence of the output of the second stage.

The reference generator is merged with the first stage and may be seen as sharing p-FET TR and capacitor CO with it. The reference generator operates at the time in the operating cycle of the first stage when TR is turned on to charge CO to reference voltage VR (from T2 to T3 in the diagram of Figure 3). In the merged circuit, TR initially charges CO to VS, a voltage which is higher than the maximum voltage required across CO, which in turn is the value needed to compensate for the largest expected voltage drop due to threshold voltage in the second stage. For practical reasons, VS may be the same voltage source as VH of the target circuit second stage. During this operation, a blocking p-FET TB is kept off to avoid direct conduction between voltage supplies VS and VRS.

VRS is the voltage supply from which the reference output is derived. It has a value which is the difference between the minimum required voltage to which CO is to be charged by the reference generator, and the minimum expected threshold voltage of the metering transistor TMR of the reference generator. The minimum required voltage from the reference generator is determined by the need to keep the inverting-stage metering transistor in its saturation region for any valid output excursion.

After CO is charged to VS, TR is turned off and TB turned on. CO begins to discharge through TB and TMR into VRS. Since the gate of TMR is connected to its drain, which in equilibrium is at the potential of CO, the voltage across CO settles to a value VR, which is above VRS by the threshold voltage of TMR. TB is then turned off and the normal operation of the target circuit continues. In each operating cycle of the charge-metering circuit, the initial output level of the inverting stage depends directly upon the threshold voltage of TMR. Subsequent output changes from the initial level, resulting from input changes during an operating cycle, are essentially threshold-independent. Thus, the dc level of the output of the inverting stage depends directly upon the threshold of TMR. Since the output dc level of the second stage depends inversely upon the threshold voltage of the second-stage metering transistor, to the extent that the thresholds track, the effect of threshold variation on

the output level is canceled. TMR is designed and placed to augment tracking.

A threshold-compensating reference voltage generator serving several target circuits simultaneously is shown in **Figure 7**. Each target circuit, shown only in part, consists of an inverting stage followed by a noninverting output stage, as in Figure 6. With multiple target circuits each must have a separate p-FET TR to provide isolation, and the reference generator must also have a p-FET TVS to control charging from VS. The capacitance across which the compensated reference voltage is developed is the parallel combination of the capacitors CO of all the target circuits, which may be seen as shared between the reference generator and the target circuits. Operation is essentially the same as that of the circuit of Figure 6, with TR and TVS turning on together but TR turning off first. TVS must be designed with a wide channel to minimize its influence on charging time. Isolating TVS from CO by turning TR off first avoids the larger charge-injection errors which would otherwise result from the turn-off of TVS.

Applications: Nonlinear sampled-staircase DAC

This application uses the two-stage configuration of Figure 5: an inverting track-and-hold with a noninverting output buffer, to track a nonlinear monotonic staircase waveform and hold its value at a time determined by the value of a digital input. Thus, the digital input is converted to an analog output voltage according to a nonlinear transfer function determined by the envelope shape of the staircase waveform [3]. This type of DAC is very suitable for use in data line driver chips for active-matrix display panels, in which some 200 such circuits are typically placed on each chip along with the associated digital subsystem. The details of this application have been described elsewhere [1].

We have verified the use of charge-metering track-and-hold circuits in this application by means of several track-and-hold designs fabricated with a conventional 2- μm CMOS technology, and with chips containing a four-circuit cross section of a six-bit data line driver chip, including the digital subsystem and a single threshold-compensating reference voltage generator circuit serving the four two-stage track-and-holds. The track-and-hold circuits were designed with a gain of about -1 , with first-stage capacitors CM and CO with capacitances of 11.1 and 8.2 pF, respectively. The largest applied voltage is VS to the reference voltage generator; 8 V was used. The capacitance of a display data line is the normal load capacitor of each output stage. For testing, this was simulated by 133-pF load capacitors. A CMOS series switch is provided at the output of each output buffer stage to provide for analog pipelining, so each output is

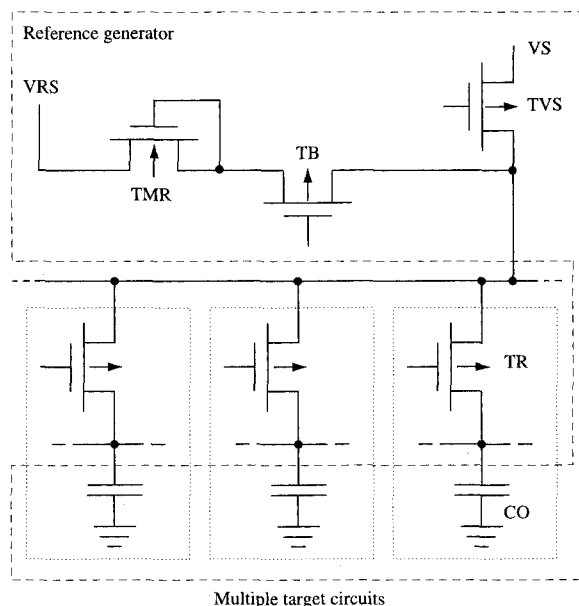


Figure 7

Threshold-correcting reference voltage generator serving multiple target circuits.

held on the data line capacitance for most of a display line time (18.3 μs for the tests) while the next datum is being processed simultaneously in the preceding stage. The nonlinear transfer function of the DAC compensates for the nonlinearity of the optical transducer of the display and provides the required gamma correction of the displayed image.

The experimental circuits provide a precision better than one half of a least-significant bit for six bits. A measured response curve of a six-bit design with a linear input ramp is shown in **Figure 8**. Extension of the technique to eight bits appears to be straightforward.

Applications: Linear charge-summing DAC

Charge-metering circuits are capable of summing analog charge packets in a capacitor, which may be useful for analog functions such as addition, averaging, and interpolation. Application to digital-to-analog conversion is outlined here.

Digital-to-analog converters of the sampled-staircase type described above, and the resistor-string type which is common in the display data driver application, have the advantage of providing nonlinear transfer functions when required. They have the disadvantage of requiring as many reference inputs or states as the number of states that can be represented by the digital data: 2^n states for n -bit

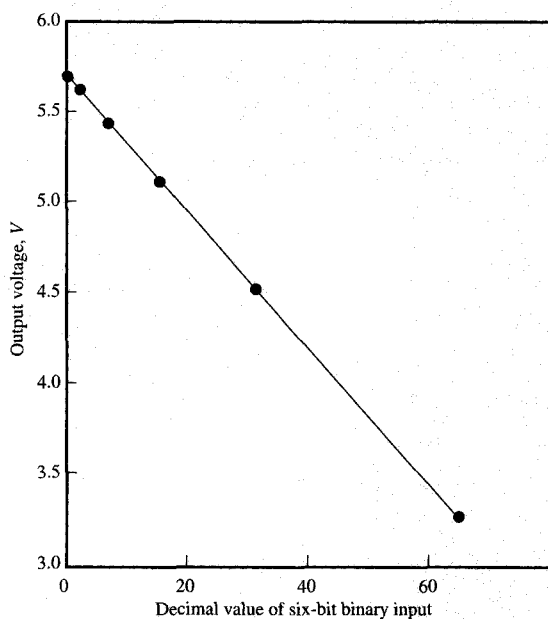


Figure 8

Measured response of an experimental six-bit sampled-staircase DAC with a linear staircase waveform.

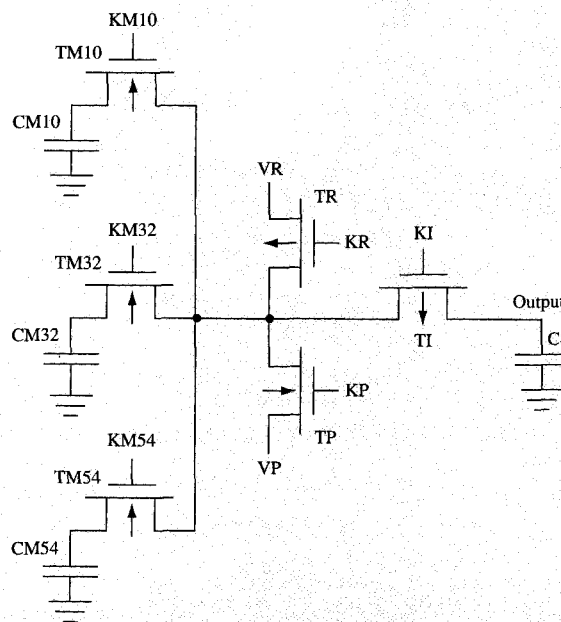


Figure 9

Simplified schematic of a hybrid (parallel and sequential) six-bit charge-summing DAC.

digital data. In the former type, the reference states are supplied sequentially at a single input, while in the latter they are applied simultaneously at separate inputs. In six- and eight-bit systems, some of the references are typically generated internally by linear interpolation between pairs of externally supplied references, but this introduces considerable complexity and compromises the nonlinear transfer function.

In such systems, extension to large numbers of bits is complicated by the fact that the number of references needed doubles with each additional bit. For that reason, high-precision DACs for general applications are often implemented by generating a reference quantity for each bit rather than for each state, selecting or rejecting each according to the value of the corresponding bit, and summing those selected to obtain the analog value. This type of converter is inherently linear because of the summation, but nonlinearity can be obtained by providing for more bits of precision in the DAC than are present in the system input data, and interposing a lookup table incorporating the nonlinearity between the system digital input and the DAC digital input.

The classical choice for electrical representation of the reference quantity has been binary weighted currents, but in MOS converters charge is often used. Both are

designed with operational amplifiers to provide a virtual ground at the current- or charge-summing node, a questionable requirement in applications using hundreds of DACs on each chip. Those using charge, typified by charge-redistribution DACs, incorporate complex networks of switches and binary weighted capacitors which have neither terminal at a common potential. A charge-summing DAC using bucket-brigade techniques has also been described [4].

Charge-metering charge-summing DACs would seem to have potential advantages. Charge-metering circuits can sum analog charge packets in two ways, simultaneously and sequentially. These may be combined in a practical hybrid DAC to good advantage. By way of example, a somewhat simplified schematic of a first stage of a six-bit hybrid DAC is shown in Figure 9 and its timing diagram in Figure 10. In the display application, a second noninverting stage would follow the charge-summing stage. This example illustrates the principle while avoiding complicating the discussion with practical details, such as the application to the circuit of the digital inputs, and the avoidance of data-dependent errors due to subthreshold conduction.

Three circuit branches contribute signal charge simultaneously to a common charge-summing capacitor

CS. An isolating switch TI allows the charge placed on CS by a first operating cycle to remain undisturbed until a second operating cycle is complete and contributes additional charge to the sum. Sequential operation incurs a small charge-sharing error each time TI turns on, so the number of sequential operations is best kept small. Quantifying this error and determining what limits it may impose on the use of sequential operation would require detailed design studies, taking account of the details of the CMOS technology used.

The charge contributed by each branch to the sum is equal to the product of the charge-metering capacitance CM_x of the branch and the voltage change at the gate of the charge-metering transistor TM_x of the branch; thus, by using different gate voltage changes in the two operating cycles, each branch is able to contribute different binary weighted charges to the sum in the two cycles. By means of hybrid operation and because both capacitance and voltage change enter into the determination of the binary weighted charges, both excessive capacitance ratios and extremes of voltage change can be avoided. Charge-metering transistors with narrower channels can be used with the smaller capacitors.

Digital inputs determine which of the three branches are able to contribute charge to the sum by gating the weighted voltage changes to the charge-metering transistor input gates (for binary 1 input) or blocking them (for binary 0 inputs). The binary input gating circuits are not shown, but are straightforward. In the example in Figure 10, the input 101111 produces the analog output 47. Among several alternatives to this method of controlling the binary inputs, it is worth mentioning that of applying the weighted voltage changes to the input gates unconditionally and raising the source voltages of the charge-metering transistors which receive a binary 0 input to prevent charge transfer.

At this writing, only elementary circuit experiments have been performed which do little more than verify the concept. These used a breadboard circuit with discrete components. They verified simultaneous operation of a three-branch first stage which simulated the three least significant bits of an eight-bit converter for the AMLCD application. Correct operation was obtained with a least-significant-bit contribution to the output of 7 mV.

Conclusions

We have found charge-metering circuits to be useful additions to the circuits tool kit. They can perform a variety of functions in analog sampled data systems with high accuracy and precision, avoiding the use of linear buffering, operational amplifiers, series capacitors, and high-precision components. Most of our work has focused on their application to digital-to-analog data line driver

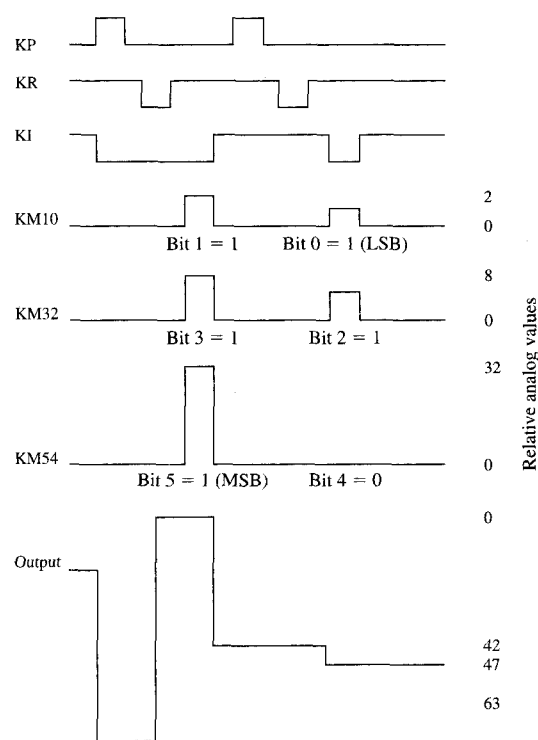


Figure 10

Timing diagram for the circuit of Figure 9 for the example of a 101111 digital input.

circuits for active-matrix liquid crystal displays. Experimental six-bit systems exhibit precise nonlinear response, not just piecewise-linear, and incorporate analog pipelining so that data signals can be applied to data lines for most of the display line time. We project that eight-bit circuits of this type can be an important element in future liquid crystal displays capable of competing with CRT in high-quality color monitor applications.

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