Preface

Today's hardware designers are required to balance requirements for performance and special features against steadily increasing pressure on design-cycle time, flexibility, and cost. Rapid advances in technology, library design, and design automation have made application-specific integrated circuit (ASIC) technology an increasingly viable choice for many applications. An ASIC is designed using a predefined set of elements (logic functions, I/O circuits, memory arrays, and selected complex functions) called a design library, together with a suite of design tools that are used to perform logic design, analysis, and physical layout. The underlying technology, the library built on top of it, and the design tools all contribute to the effectiveness of ASIC technology for a given application. The papers in this issue describe some of the methodologies and tools recently developed by IBM for use in ASIC design, as well as some applications to actual product design for both IBM and IBM customers.

A successful ASIC library design allows the ASIC designer to take advantage of the performance and circuit density benefits available in the underlying technology, while making maximum use of design automation tools in both logic design and layout. In addition, it must be possible to quickly develop a new ASIC library whenever new technology becomes available, because the library is the means by which the ASIC designer accesses the technology. The paper "Technology-migratable ASIC library design" by Bednar et al. describes the process of defining, designing, and qualifying an ASIC library.

While the library is the means for accessing the technology, design automation tools are the means for accessing the ASIC library. In the paper "Design methodology for IBM ASIC products," Engel et al. describe a design methodology that uses design automation tools to produce high-performance, high-density, and highly testable ASIC designs. This design methodology is a major factor in the ultimate performance and density that the ASIC design team is able to achieve. The effectiveness and ease of use of the methodology also contribute significantly to reducing the length of the design cycle.

Four key design automation tools supporting logic design, physical design, and the ASIC sign-off methodology are also described in this issue. One common theme of these four papers is the way in which the tools support the design of a high-performance ASIC chip in a production environment, with varying details in algorithm description. ASIC design examples are presented to illustrate the quality of results obtained using these tools. There is also a heavy emphasis on describing the tool methodology.

The paper "BooleDozer: Logic synthesis for ASICs" by Stok et al. describes the IBM logic synthesis tool BooleDozer, including its organization, its principal algorithms, and its relationship to the ASIC design process.

The paper "Design planning for high-performance ASICs" by Sayah et al. introduces a paradigm shift centered on design planning for sub-half-micron ASIC design. A comprehensive implementation of the concept is embodied in the Hierarchical Design Planner (HDP), which serves as a link between logic synthesis and physical design, passing design and timing constraints downstream hierarchically while concurrently launching multiple physical design activities. Rapid timing closure has been achieved in real production designs using the area and timing planning capabilities within the context of the HDP timing-closure methodology, exploiting its tight integration with incremental timing analysis.

The paper "Circuit placement, chip optimization, and wire routing for IBM IC technology" by Hathaway et al. describes the increasing importance of chip optimization tools, including scan and clock tree optimization on-chip, as well as the application of performance-driven placement and wiring to actual ASIC designs.

On the subject of testing, the paper "Test methodologies and design automation for IBM ASICs" by Gillis et al. describes the wide spectrum of ASIC chip testing techniques used inside IBM, the ASIC testing sign-off process, and the various stages of ASOK (ASIC Sign-off Kit) implementation.

The final three papers in this issue describe three products based on the IBM CMOS 5 ASIC technology. Two papers represent OEM products designed outside IBM, and one paper describes an IBM product.

Product design teams must evaluate performance, cost, time to market, and a number of other product-specific criteria when selecting the technology to be used in their products. The design team has at its disposal full custom, semi-custom, and ASIC technology, as well as several possible combinations of the three. The paper "IC technology and ASIC design for the Cray J90 supercomputer" by Poli et al. describes the process of selecting and implementing ASIC technology for the Cray Research J90 supercomputer, which contains ten different high-performance ASICs. The design decisions and implementation process used in designing Digital Equipment Corporation's PowerStorm graphics processor are described in the paper "Design considerations for Digital's PowerStorm graphics processor" by Gianos and Hobson. Finally, the paper "PowerPC AS A10 64-bit RISC microprocessor" by Bishop et al. describes the design of a new IBM microprocessor in ASIC technology.

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