Critical charge calculations for a bipolar SRAM array

by L. B. Freeman

The critical charge, Q_{crit}, of a memory array storage cell is defined as the largest charge that can be injected without changing the cell's logic state. The Q_{crit} of a Schottky-coupled complementary bipolar SRAM array is evaluated in detail. An operational definition of critical charge is made, and the critical charge for the cell is determined by circuit simulation. The dependence of critical charge on upset-pulse wave shape, statistical variations of power supply voltage, temperature gradients, manufacturing process tolerances, and design-related influences due to word- and drain-line resistance was also calculated. A 2× range in Q_{crit} is obtained for the SRAM memory array cell from simulations of normal ($\pm 3\sigma$) variations in manufacturing process tolerances, the shape of the upset current pulse, and local cell temperatures. Using SEMM, a 60× variation of the soft-error rate (SER) is obtained for this range in Q_{crit}. The calculated SER is compared to experimental values for the chip obtained by accelerated testing. It is concluded that a range in values of the critical charge of a cell due to normal manufacturing and operating tolerances must be considered when calculating soft-error rates for a chip.

Introduction

As storage cells for memory array chips become smaller and more numerous, the power per cell decreases and the write and read performance improves. This has led to reduced cell stability and an increased susceptibility to transient noise effects in the circuits.

The effect of one form of transient noise, soft errors due to high-energy particles traversing p-n junctions in silicon, is considered in this paper. The high-energy particles come from the natural radioactivity of the materials used in manufacturing the integrated circuits and from external sources such as cosmic rays. The particles traversing the silicon create electron–hole pairs that, under appropriate conditions, can deposit charge onto storage cell nodes and cause temporary (soft) circuit malfunctions.

Soft-error-rate information must be obtained in a timely manner so that its implications can be evaluated and appropriate alterations made to latch and cell designs. Analysis after a chip has been designed is not sufficient, since chips have been found to be failure-prone after it was too late to easily modify their design.

To generate useful design data, a readily implementable standard way to calculate and interpret soft-error effects must be developed. The method should use the usual tools available to the chip designer for the solution of other circuit operation and performance problems. It should give design information, such as what can be done to affect the cell stability and how cell stability can be affected by other

0018-8646/96/$5.00 © 1996 IBM

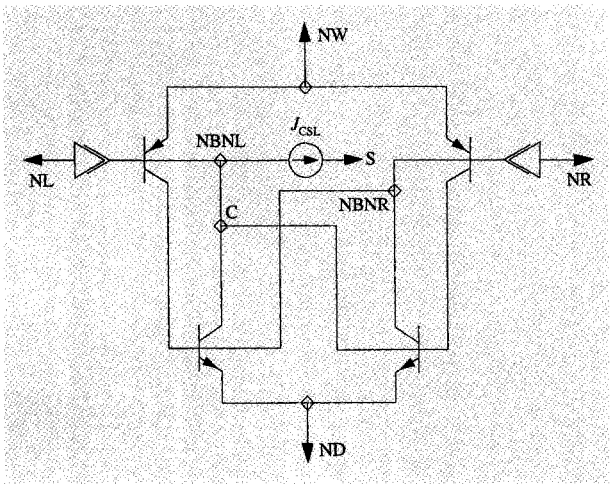

Figure 1

CTS storage cell circuit schematic. Shown is the complementary transistor switch (CTS) storage cell analyzed in this paper. An array of cells is formed by connecting adjacent cell word-line and drain-line terminals together (horizontal lines), and left and right bit-line terminals (vertical lines). The circuit notation is as follows: NW, external word line; ND, external drain line; NL, external left bit line; NR, external right bit line; NBNL, internal left cell node; NBNR, internal right cell node. The current source J_{CSL} connected from collector (C) to substrate (S) represents the charge injection point for the cosmic-ray-induced charge burst.

performance considerations. Most important, it should give quantifiable results which can be used to predict error rates that can be validated by experiment.

Many attempts have been made to analyze soft errors due to high-energy particles in electronic devices. Soft-fail-rate studies in satellite electronic chips and systems are very advanced but have been of limited value for determining terrestrial SER values for memory arrays and whole systems, since the radiation which most affects satellite electronics is very different from the particle flux found at sea level [1]. For terrestrial electronics, many attempts, experimentally [2–4] and by circuit simulations [5–13], have previously been made to determine values for the charge causing circuit failure. A circuit failure criterion has been incorporated into these studies by means of a phenomenological parameter called the critical charge, Q_{crit}. The critical charge is defined as the maximum amount of charge that can be deposited on a specific device junction without causing circuit failure. Circuit failure typically involves the erasure of or change to information stored in a memory cell or latch. The critical charge is a function of the design and operation of the circuit and is calculated by a product designer using circuit simulation tools and models.

At IBM, the soft-error-rate problem for bipolar logic arrays has been under continual investigation by product design and device groups for more than a decade. The semiconductor physics aspects of the problem have been addressed and incorporated into a simulation tool called SEMM (Soft-Error Monte Carlo Modeling) [14]. SEMM calculates the probability that specific amounts of charge are deposited on semiconductor junctions for particular circuit and device structures in different radiation environments [15]. Circuit failure rates are then predicted from the charge deposition rates. The circuit failure criterion is incorporated into SEMM by means of the critical charge parameter, Q_{crit}.

SEMM provides a quantitative method to predict failure rates in a natural or man-made radiation environment. Circuit sensitivity to the injection of spurious charge is determined, the spurious charge generated in a particular device and circuit by a specified radiation environment obtained, and the failure rate calculated.

Using a 64Kb array chip with Schottky-coupled complementary bipolar transistor switch (CTS) cells as an example, the critical charge for SEMM calculations is determined. The method is offered as a model of a standard way of calculating critical charge. The results emphasize that the critical charge for a chip is not necessarily single-valued, but can be affected by charge pulse shape, circuit position on the chip, power supply voltages, temperature, and manufacturing device parameter variations.

Discussion

The analysis is broken into two parts. First, the storage cell is studied in isolation. The connection between the isolated cell and its environment is contained in the cell standby current. For the isolated-cell studies, the standby current is considered an independent parameter. Then, the peripheral circuits such as the word-line driver and array structure such as line length and resistance are studied with regard to their effects on cell standby current. The range and variation of cell standby current are calculated and combined with the isolated-cell variations in order to arrive at the final critical charge values. The cell critical charge thus contains the effects of both the cell parameters and the chip operating environment.

- *Storage cell*

The complementary transistor switch (CTS) array cell [16] shown in **Figure 1** is a bipolar, static, high-density, high-speed random access storage element. Data are stored in cross-coupled vertical npn and lateral pnp transistors physically formed into a four-layer npnp, or SCR (silicon-controlled rectifier) structure. The two storage states are distinguished by one pair of npn/pnp transistors conducting while the other pair is turned off. The cell npn transistors are unclamped (saturated), resulting in a relatively stable cell. The storage mechanism of the CTS cell, using

Schottky barrier diodes (SBDs) for bit-line connections, is similar to the related Harper pnp cell that connects to the bit lines with npn transistors. The initial state is with the left side of the cell "off" and the right side "on." A current pulse can turn off the "on" transistors and turn on the "off" transistors, switching the cell.

There are several p-n junctions in the cell—base-to-emitter, base-to-collector, and collector-to-substrate. The collector-to-substrate junction, with the largest area, is the dominant one for soft errors and is the junction considered in this paper. The current source, J_{CSL}, is connected from the collector to the substrate of the npn transistor on the "off" side of the cell and is used to model the transient charge pulse caused by high-energy particles traversing the junction. Pulse charge effects at the other junctions may be analyzed in a similar manner.

An array of cells is formed by connecting adjacent cell word-line and drain-line terminals together horizontally, and left and right bit-line terminals together vertically. The cells are powered, in standby, by the word-line-to-drain-line voltage. This is a low-power operation. A cell is powered during read and write by current flowing from the bit line coupling SBDs into the drain line. This is a high-power, fast operation. The cell consists only of diode and transistor junctions with exponential I/V characteristics. There is no current-limiting resistor in the cell that can linearly absorb voltage differences. This affects the results of the analysis through line resistance and device and temperature tracking variations.

An array of cells is formed with several hundred parallel cells between the word and drain lines associated with each word decoder. An active cell, one with an npn/pnp pair on, clamps the word-line-to-drain-line voltage to a value of ($npn\ V_{ce\,sat} + pnp\ V_{be}$). The clamped word-line-to-drain-line voltage is insufficient for inactive cells to become active. The cells which happen to have the smallest voltage drops, due to manufacturing and other variations, use a disproportionate amount of word-line current, depriving the active cells with higher intrinsic voltage drops. This effect can cause relatively large variations in the cell standby current. It also results in large cell initialization times and large cell recovery times (from SER perturbations) when the only power available to set the cell comes from the word-line-to-drain-line voltage.

Two sets of circuits define a cell's operating characteristics—the cell itself and the peripheral circuits and array organization surrounding the cell. The standby state of the cells is of interest for the soft-error-rate (SER) calculations, because most cells are in this state most of the time. During standby operation, the peripheral circuits of interest are those generating the word-line and the drain-line voltages. The coupling between the cell circuitry and the peripheral circuits is in the cell standby current.

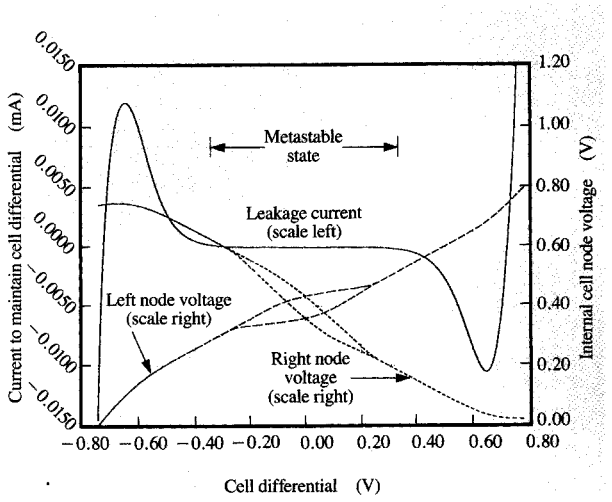

Figure 2

CTS cell static switching characteristics. Shown are plots of the current required to disturb the cell from equilibrium and the corresponding left/right cell node voltages. The cell's stable states are the leftmost and rightmost conditions of zero leakage current (cell differential voltages of −0.75 and +0.75 V). In the center of the plot is shown the metastable region of the cell operation, in which the leakage current is zero for a range of cell differential voltages. This plot assumes a word-line (NW)-to-drain-line (ND) bias current of 4 μA. The left and right cell node voltages are complementary and range from 0 to 0.75 V.

Significant information can be obtained by studying the cell operation as a function of the isolated-cell standby current. The peripheral circuits and array organization can then be studied independently in order to understand the causes and the magnitudes of the cell current variations. The peripheral circuit current effects, combined with the cell current sensitivity, result in a complete description of the cell operating characteristics.

For a cell, the soft-error rate is established as a function of the critical charge, Q_{crit}. The critical charge is obtained as a function of a circuit design parameter, the cell current. The cell, peripheral circuits, and array design required to achieve the necessary current and Q_{crit} in order to meet the required soft-error rate may thus be determined.

- *Characteristics of the isolated cell*

The low-speed (static) switching characteristics of the cell are shown in **Figure 2**. Plotted here is the (leakage) current required to perturb the cell from equilibrium by a voltage source connected between the left internal cell node and the substrate as a function of the resulting cell differential voltage, along with the corresponding internal cell node voltages. The cell's stable states are the left and right

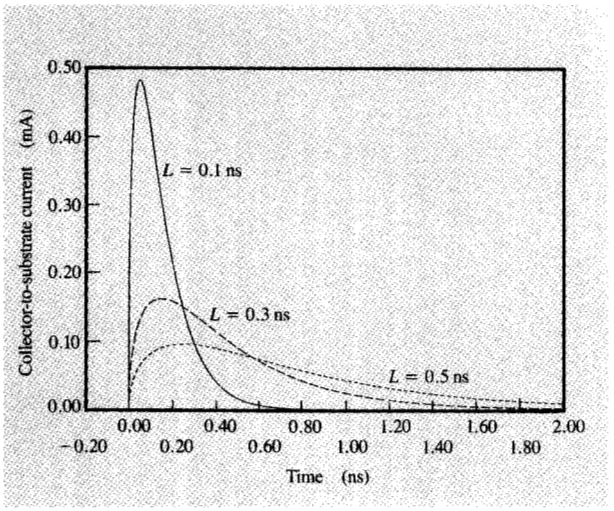

Figure 3

Collector-to-substrate charged particle current pulse shapes. Shown is a plot of charge pulse shapes used in this paper, as defined by Equation (1), with time constants L = 0.1, 0.3, and 0.5 ns. All pulses are normalized to 100 fC total charge. These currents are assumed to enter the cell at position J_{CSL} (Figure 1). From [17], reproduced with permission; © 1994 IEEE.

crossings of the zero-current line. The cell will flip with 10 μA of dc leakage current, as shown by the right negative current peak, when operating with 4 μA of bias current.

The CTS cell is characterized by an extended metastable operating region in the center of the characteristic curve where there is insufficient word-line-to-drain-line voltage (power) to switch the cell. The internal cell nodes float. Cell information is lost if the cell is switched into the metastable region, since it is in neither a "one" nor a "zero" state. Subsequent reading of the cell would return random data. This third, or metastable, state has subtle implications for design and experimental verification. A high-energy particle knocking the cell into this state will cause a solid failure from a circuit design and operational point of view. However, when the cell is experimentally checked after such a perturbation, there is only a 50% chance of finding anything wrong. Although the information in the cell is completely destroyed and can never be trusted, there is a random chance that the correct data may be read out.

The high-energy particles causing the soft fails produce short transient charge pulses when they interact with the silicon atoms in the collector-to-substrate junction area. Depending on the incident particle energy, angle, and position, charge pulses of various amplitudes and durations are generated. The pulses are characterized by a total charge, measured in femtocoulombs, and a time constant, measured in nanoseconds, as shown in **Figure 3**. Here, current is shown as a function of time for 100-fC pulses for three different pulse time constants (L). The current source is connected between the collector (C) and substrate (S) of the cell npn transistor in Figure 1. The equation for the pulse current from collector to substrate (J_{CSL}) as a function of L is

$$J_{CSL} = KQ\sqrt{t}\,\frac{e^{-t}}{L}, \tag{1}$$

where

t = time/L, time ≥ 0,
L = 0.1, 0.3, and 0.5 ns (pulse time constant),
Q = 100 fC (total charge),
K = constant to make pulse shape integrate to unity (typically 0.00112838).

The pulse shape described in Equation (1) is typical for SER transient charge pulses (see [17]).

The critical charge, Q_{crit}, is the largest charge that can be injected into a cell without changing the state of the cell. In order to obtain numerical values, we require an operational definition of critical charge. This definition must be meaningful from a physical point of view, quantifiable in a repeatable manner, and calculable by a

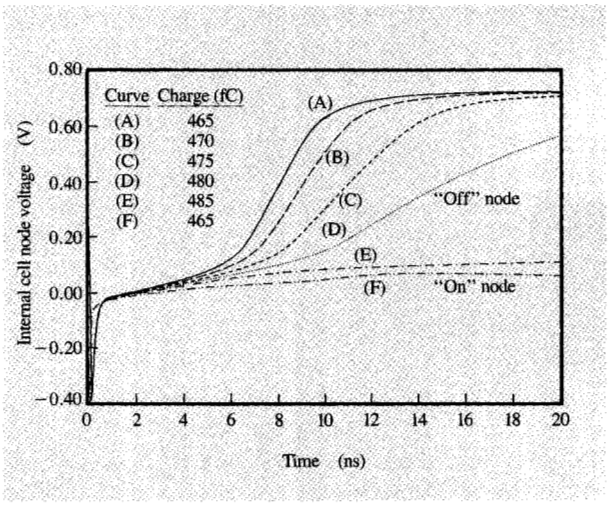

Figure 4

CTS cell recovery from a collector-to-substrate 0.1-ns charge pulse. Shown are plots of cell node voltages following the injection of a charge pulse, J_{CSL}, as described in Figure 1. The injected charge in all cases is assumed to have a time constant of 0.1 ns (see Figure 3). Four plots show increased time for recovery of the "off" node, based on the total charge of the pulse, varying from 465 fC to 480 fC as indicated. The recovery time is very nonlinear with injected charge. A fifth charge of 485 fC injected into the "off" node switches the cell to the opposite state. The injected charge has no effect on the cell if injected into the "on" node (see text for definitions of "on" and "off").

circuit simulator. The statement "without changing the state of the cell" requires a definition of cell recovery. Cell recovery depends on the cell node voltages and the times at which they are measured after being hit with a current pulse.

The response of the cell to current pulses depends on both the total charge and its duration. The effect of varying the charge is shown in **Figure 4**, where the internal cell node voltages, obtained from a circuit simulation, are plotted as a function of time. The recovery from pulses perturbing the cell from equilibrium for five different charge-level cases (465, 470, 475, 480, and 485 fC) for the "off" side node and one charge-level case (465 fC) for the "on" side node are shown. Only the "off" side node pulses affect the cell state. The cell is unbalanced with a 0.1-ns time constant collector-to-substrate current pulse. The analysis conditions are nominal device parameters with the cell powered by a word-line-to-drain-line voltage that establishes a 4.0-μA cell bias current. The node voltage values are referenced to the drain line. All but the 485-fC case recover, but at different rates.

The effect of varying the charge pulse time constant is shown in **Figure 5**,* where the internal cell node voltages are replotted. The cell is unbalanced with a 485-fC collector-to-substrate current pulse. Three cases are shown, with pulse time constants of 0.1, 0.3, and 0.5 ns. Both the "off" and "on" side node voltages are shown for the three cases. Two cases recover; one case (0.1-ns) eventually switches to the other state.

*This figure, obtained from the present work, was reproduced in [17].

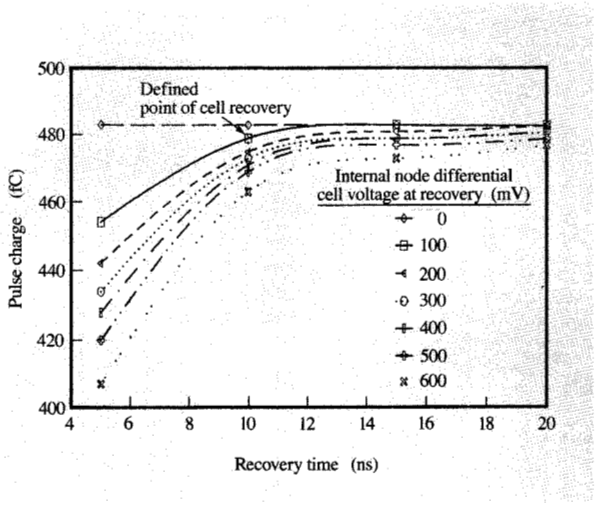

Figure 6

Definition of critical charge Q_{crit} in terms of cell recovery. This chart allows the designer to understand the relationship among pulse charge, recovery time, and differential cell voltage. Plotted is the charge pulse that results in the cell recovering to a specific differential node voltage in a specified time. For example, for a recovery to 100 mV differential cell voltage, within 10 ns, the injected charge must be below 475 fC. From this, we define Q_{crit} as the charge that results in the cell recovering to 100 mV within 10 ns. This definition of Q_{crit} is used henceforth in the paper.

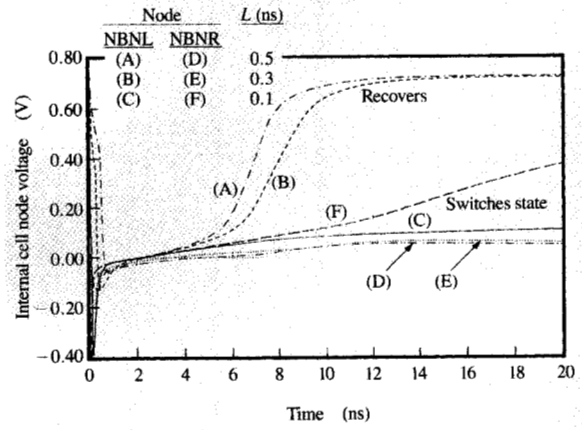

Figure 5

CTS cell recovery from a collector-to-substrate 485-fC charge pulse. Shown are plots of cell node voltages following the injection of a charge pulse, J_{CSL}, as described in Figure 1. The injected charge in all cases is assumed to have a total charge of 485 fC with varying time constants (pulse shapes). Three cases are shown, with time constants of 0.1, 0.3, and 0.5 ns. Shown are the NBNL and NBNR voltages for each case (see Figure 1 for definitions). The cell recovers following the 0.3-ns and 0.5-ns pulses, but switches for the 0.1-ns pulse, indicating that *pulse shape* (within acceptable ranges) is an important parameter to SER calculations. From [17], reproduced with permission; © 1994 IEEE.

The cell recovery characteristics are summarized in **Figure 6**. The charge pulse that results in the cell recovering to a specific differential internal node voltage in a specified time is plotted. The pulse time constant is 0.1 ns for these cases. Considerations of cell recovery then lead naturally to a definition of critical charge. Stating that the cell has recovered to a certain differential voltage in a specific time results in the range of possible values for Q_{crit} shown in Figure 6.

The considerations in selecting a definition for Q_{crit} are that the cell recovery should be checked at a physically reasonable time, the cell differential voltage should cover imbalances due to processing variations and device defects, it should be a relatively stable point insensitive to outside variations, and it should be obtained with reasonable computer simulation (run) time. From this, we select as the working definition for cell recovery in this calculation of critical charge, the charge that results in the cell recovering to a 0.100-V cell differential at 10 ns.

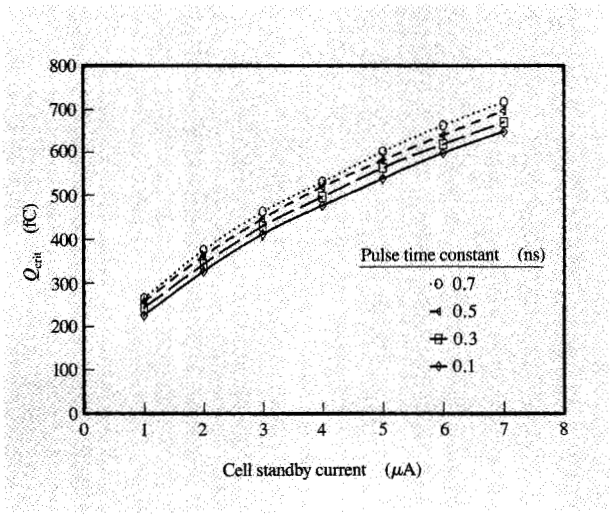

Figure 7

Critical charge as a function of standby current and pulse shape. Shown is the critical charge, Q_{crit}, of the cell as a function of the standby current and pulse time constant (pulse shape). Each point represents a current pulse that results in the cell recovering to a cell differential node voltage of 100 mV at 10 ns (see Figure 6).

This method of obtaining a definition of critical charge should apply to other logic and memory cell types. However, the specific values used are dependent on such factors as the cell speed and recovery characteristics, and could be unique for each design.

The critical charge for the CTS cell is now calculated for a number of different conditions. The critical charge for the cell as a function of cell standby current and pulse time constant is shown in **Figure 7**. Each point represents a current pulse that results in the cell recovering to a cell differential node voltage of 0.100 V at 10 ns. The cell is simulated with nominal device processing parameters, and powered with a word-line-to-drain-line voltage that establishes the indicated cell standby bias current. The disturb pulse shapes are shown in Figure 3. There is a large variation in Q_{crit} with cell standby current. A relatively small sensitivity to charge pulse time constant is observed. This is because the cell response time is long compared to the range of pulse time constants. Since all of the pulses occurred before the cell could respond, they had similar effects. A standard pulse time constant of 0.3 ns is used in the remainder of this discussion.

A faster-responding storage cell or logic latch could discriminate between the different pulse widths and cause a much larger pulse time constant sensitivity. This would then need to be explicitly handled in the SER calculations by passing the pulse time constant dependency to the SEMM program. In this case the dependency would be specified by the linear equation

$$Q_{crit}(L) = Q_{crit}(0.3) + (L - 0.3)\frac{Q_{crit}(0.7) - Q_{crit}(0.1)}{0.6}, \quad (2)$$

where the time constants are given in Figure 7.

The sensitivities of critical charge to variations of the independent device processing parameters and temperature are shown in **Figure 8**. Each of the twelve most important independent parameters is perturbed to its low and high limit, and the corresponding variation in critical charge is tabulated and plotted. All other independent parameters are set to their nominal conditions. The cell is unbalanced by a collector-to-substrate current pulse with Q_{crit} charge and a time constant of 0.3 ns. The cell is powered with a word-line-to-drain-line voltage that establishes a 4.0-μA bias current. The sensitivities of critical charge to variations of the independent process parameters are unique to this design and cell type. The cell transistors operate in a saturated state, and the sensitivities reflect the importance of those parameters associated with the inverse and saturated transistor, such as stored charge. Also, the cell has a lateral pnp transistor with characteristics noticeably affecting critical charge.

The most important parameters affecting critical charge are not those that manufacturing typically monitors and closely controls. This results in the large tolerances observed and has negative implications for the precision of the critical charge predictions. While we are concerned with soft-error rates and unintentional changes of the state of the cell in this paper, the parameters affecting these unintentional changes are the same as those that affect intentional writing. This question of accuracy and tolerance has a direct bearing on the ordinary write performance of the chip.

The 3σ statistical and worst-case variations of the critical charge are found by analyzing the sensitivities of Q_{crit} to variations in the independent process and temperature parameters. **Figure 9** shows the critical charge, at a 4.0-μA cell current, as a function of the independent parameter variations, where the independent parameters are varied simultaneously in the directions that produce the largest change in the critical charge. This determines the total range that might be seen for Q_{crit}, from 247 to 1306 fC. The extreme values are unlikely to occur, because this would require several device parameters to be simultaneously at their worst-case limits. A more probable range of variation for Q_{crit} is given by the 3σ tolerances, obtained from the individual parameter sensitivities and plotted in Figure 9.

The Q_{crit} tolerance calculations are now repeated for different cell currents (1.0, 2.0, and 4.0 μA) in order to relate the isolated-cell calculations to the behavior of the complete storage array. **Figure 10** shows a plot of the 3σ

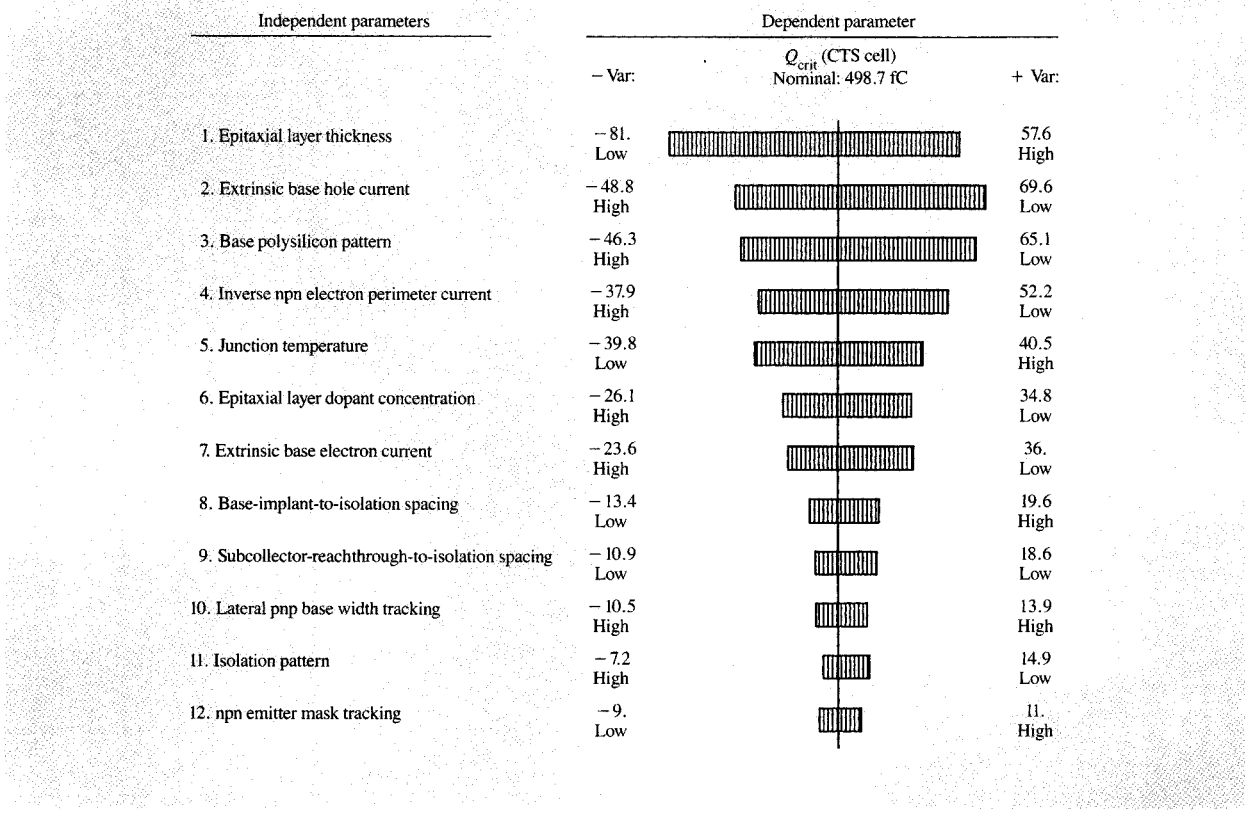

Figure 8

Variations in Q_{crit} depending on VLSI process variations. Using the definition described in the text and Figure 6, we show the variation of Q_{crit} for the cell within normal ($\pm 3\sigma$) manufacturing tolerances. The normal Q_{crit} of this cell is calculated to be 498.7 fC. The bipolar epitaxial layer thickness variation (which occurs in normal manufacturing) causes Q_{crit} to range from −81 fC to +57.6 fC from this value. Other accepted tolerances add changes as indicated. The ends of the Q_{crit} bars shown are 3σ variations for each independent parameter.

critical charge range as a function of cell standby current for the standard 0.3-ns pulse time constant and cell recovery definition of 0.100 V at 10 ns. This Q_{crit} variation is combined with the cell current variation produced by the array peripheral circuits in order to obtain the final value of the predicted critical charge distribution.

- *Cell currents in the array*

Although the cells in a storage array are similarly designed, they can have dissimilar operating characteristics because of differences in the electrical and thermal environments they experience. The cell physical position, represented by varying word-line, drain-line, and bit-line resistance, has a major effect on the current through individual cells. Chip temperature gradients, caused by circuit and power density variations, are also found to have a major effect because of device junction temperature differences. Such effects must be known at the time the chip is physically designed so that they can be incorporated into the chip architecture and assembly decisions in order to prevent unexpected failure modes and reduced operating windows.

Figure 11 illustrates the relationship between array cell locations and the peripheral circuits. The bit decoders and bit selectors, vertical on the left side of the figure, dissipate 3.0 W. Word decoders, horizontal through the center of the array, dissipate 1.5 W. The ends of the word and drain lines are at the top and bottom. The whole array of cells dissipates only 0.2 W. This results in temperature gradients throughout the chip (see **Figure 12**). The maximum chip temperature gradient is 6.8°C, and the worst temperature gradient along a word line is about 4.1°C. The temperature gradient between the cells results in current variations due to device V_{be} differences and the attendant nonuniform current distribution among various parallel cells.

The line resistance and the 4.1°C temperature gradient are incorporated into a cross-section simulation of the

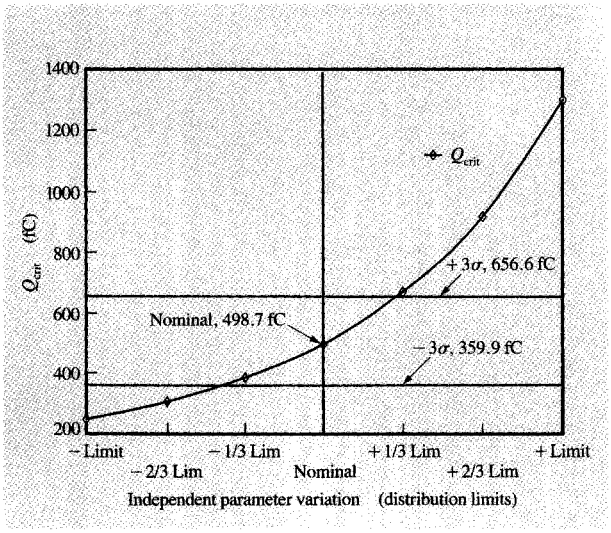

Figure 9

Worst-case collector-to-substrate critical charge variation. This plot of Q_{crit} is based on the range of values shown in Figure 8. It shows the critical charge at a 4-μA cell current as a function of the independent process variations. The extremes of possible Q_{crit} values occur at the far left and right of the above plot, where each independent parameter from Figure 8 is allowed to vary 3σ from its nominal value. The resultant Q_{crit} of the cells will vary from about 250 fC to 1300 fC. The $\pm 3\sigma$ variation of Q_{crit} from its nominal value is designated by horizontal lines at 359.9 fC and 656.6 fC.

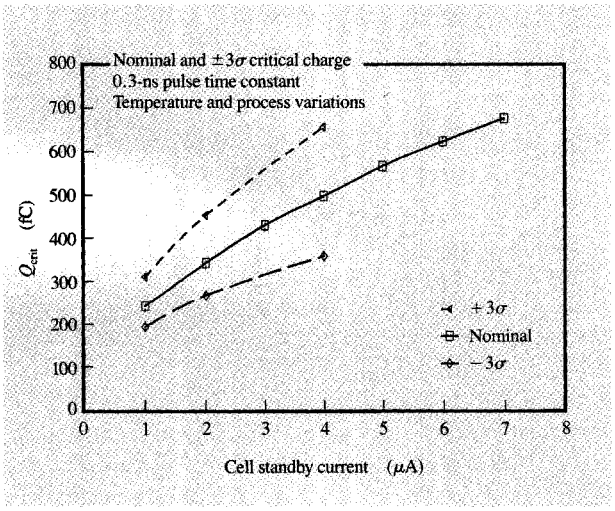

Figure 10

Cell critical charge as a function of standby current. The large differences in possible cell Q_{crit} which were shown in Figure 9 must be repeated for different cell currents to estimate the behavior of the complete storage array. Shown are variations in Q_{crit} for cell standby currents of 1, 2, and 4 μA for the standard 0.3-ns upset pulse, and standard recovery. These current variations add about $\pm 30\%$ to the previously described constant current values.

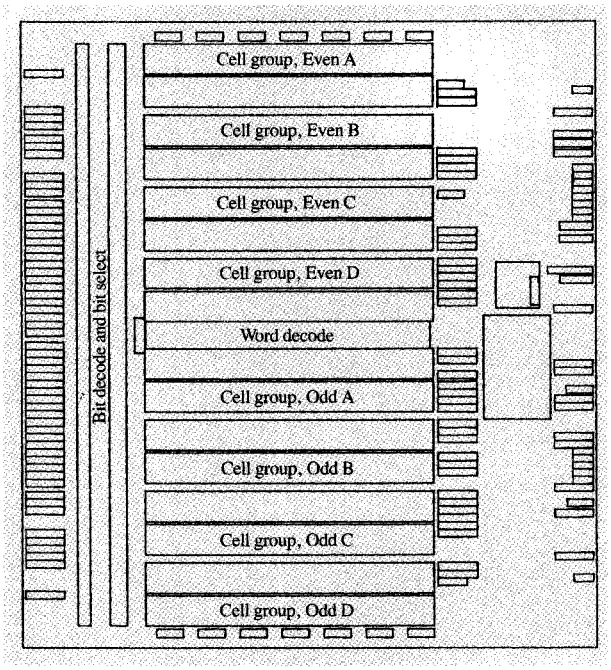

Figure 11

Placement of cells and circuits on the chip. This figure shows the array cells and the peripheral circuits on the actual chip layout (a 64Kb bipolar SRAM). Different circuits have different power dissipations, resulting in temperature gradients across the chip. This then can make differences in the temperature of cells in parallel along the word and drain lines. The above array is used to calculate the chip temperature gradients shown in Figure 12.

array in order to determine the individual cell currents. The nominal cell standby current as a function of position along a word line is shown in **Figure 13**. The 3σ tolerances calculated from sensitivities to variations in the independent device, power supply voltage, and temperature parameters are also shown. This cell current variation is used for the calculation of critical charge.

- *Cell critical charge*

The critical charge for the isolated cell (discussed in the subsection on isolated-cell characteristics and shown in Figure 10) is combined with the cell current variation (discussed in the subsection on cell currents in the array and shown in Figure 13) in order to generate the critical charge as a function of position (see **Figure 14**). The critical charge is obtained for a 0.3-ns current pulse flowing through a current source connected between the "off" internal cell node and substrate that results in the cell recovering to a 0.100-V differential voltage at 10 ns. The 3σ tolerances in cell critical charge are calculated from the sensitivities of the critical charge and the bias current to variations of the independent power supply voltage, temperature, and process parameters. This includes the

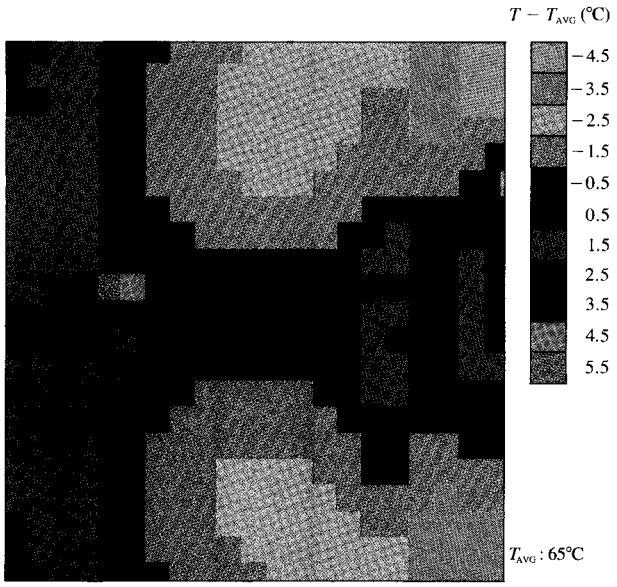

Figure 12

Chip temperature variation caused by circuit power dissipation. This plot shows a calculated temperature map of the chip based on the circuit power differences and the cell locations. The various shadings indicate *differences* from the average chip temperature (65°C) which range between +5.5°C and −4.5°C. The entire chip is assumed to dissipate 4.7 W.

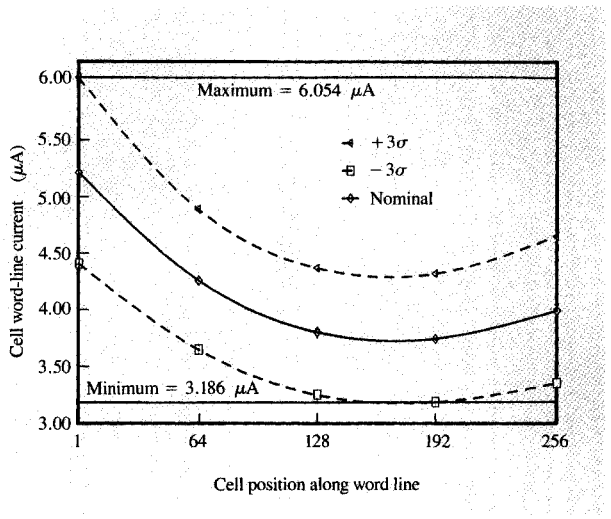

Figure 13

Cell standby current as a function of position along the word line. The cell standby current is a function of its position along the word line, where the abscissa value of "1" indicates the cell nearest the word decoder, and 256 is the cell farthest away. Including the 3σ manufacturing tolerances and the voltage and temperature variations discussed previously, this plot shows the cell current variation used in the calculation of the chip's critical charge, Q_{crit}.

effects of word-line and drain-line resistance and a 4.1°C temperature gradient. The largest Q_{crit} is produced at the cell nearest the word decoder with the highest temperature and lowest line resistance. The predicted spread in critical charge is from 340 to 755 fC.

The tolerances are calculated in this study by statistical operations on the sensitivities of the dependent parameters, such as critical charge and cell standby current, due to variations of the independent power supply voltage, temperature, and device parameters. One check on this method, for the cell standby current, gave results indistinguishable from those obtained by a Monte Carlo statistical circuit simulation.

A plot of the chip error rate, calculated by the Soft-Error Monte Carlo Modeling program for different critical charges, is shown in **Figure 15**. This curve is calculated from the cell physical design and the high-energy particle interactions. It shows the conversion of critical charge into the soft-error rate per bit for 150-MeV protons, normalized to a flux of one proton per square centimeter for one storage cell. The 3σ critical charge tolerance results in a 60× SER variation. This is both good and bad news. It leads to a better understanding of the physics involved, and to better experimental agreement. However, it shows that large variations in SER are to be expected. We need

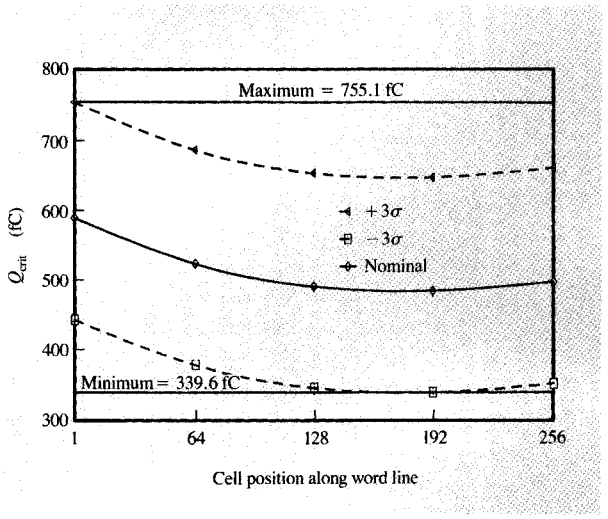

Figure 14

Critical charge variation for cells along the word line. This plot shows the variation of cell critical charge as a function of its position along the word line, where the abscissa value of "1" indicates the cell nearest the word decoder, and 256 is the cell farthest away. Also shown are the possible values for a $\pm 3\sigma$ manufacturing tolerance variation.

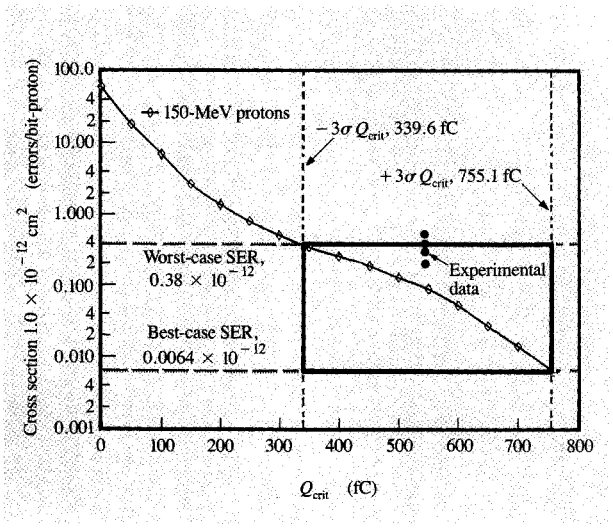

Figure 15

Cosmic soft-error rate (SER) as a function of critical charge. This plot shows how the variation of Q_{crit} from all the variations discussed previously transforms into a chip soft-error rate, SER, using the program SEMM [14,15]. The line through the diamond points indicates the SEMM soft-fail results for this cell as a function of Q_{crit} (SER is calculated for 150-MeV protons). The cell Q_{crit} varies over a range from 340 to 755 fC; hence, the theoretical SER cross section varies from 0.0064 to 0.38 $\times$ 10^{-12} cm^2 (see accentuated box in plot). Also shown are experimental SER data points from testing of this chip using 150-MeV protons (horizontal position of dots is arbitrary). A number of chips were tested, and the dots show that the experimental range is at the upper edge (highest fail rate) of the calculated values, and about 10$\times$ from the chip's nominal value, which is in the center of the accentuated box of possible SER values.

to understand these implications. This predicted error rate as a function of critical charge can be compared to the measured error rate, as shown in Figure 15.

Conclusion

The critical charge, a parameter intimately associated with cell stability, is calculated for a bipolar SRAM storage array chip using the CTS cell. The connection between a particular cell and the rest of the chip is described in terms of the cell bias current. The critical charge of a single cell is calculated in terms of the pulse shape, the cell device parameters, the temperature, and the cell current. The cell current is calculated in terms of the cell and peripheral circuit device parameters, the temperature, and the power supply voltages. Applying the cell current range to the isolated-cell critical charge calculations results in a prediction for the critical charge for cells at various locations on the chip. A large variation in critical charge is found that implies, in turn, a large variation in chip soft-error rate. The sensitivities of soft-error rate are obtained in terms of the chip physical and electrical parameters so that this effect may be factored into the basic design decisions for the product. Modeling techniques were subsequently used to successfully design the bipolar SRAM chip with a high critical charge and a very low sensitivity to soft errors.

Acknowledgment

The author wishes to thank Philip C. Murley and Huntington W. Curtis for the soft-error-rate cross-section calculations and Walter J. Ramsey for the chip temperature map.

References

1. J. F. Ziegler, "Terrestrial Cosmic Rays," *IBM J. Res. Develop.* **40,** 19–39 (1996, this issue).
2. R. L. Woodruff and P. J. Rudeck, "Three Dimensional Numerical Simulation of Single Event Upset of an SRAM Cell," *IEEE Trans. Nucl. Sci.* **40,** 1795–1803 (1993).
3. S. Satoh, R. Sudo, H. Tashiro, N. Higaki, S. Yamaguchi, and N. Nakayama, "CMOS–SRAM Soft Error Simulation System," *Proceedings of the International Workshop on Numerical Modeling of Processes and Devices for Integrated Circuits: NUPAD V*, Honolulu, June 5–6, 1994, pp. 181–184.
4. J. Schwank, "Basic Mechanisms of Radiation Effects in the Natural Space Environment," presented at the IEEE Nuclear and Space Radiation Conference Short Course, Tucson, AZ, 1994.
5. W. A. Kolasinski, J. B. Blake, J. K. Anthony, W. E. Price, and E. C. Smith, "Simulation of Cosmic-Ray Induced Soft Errors and Latch-up in Integrated Circuit Computer Memories," *IEEE Trans. Nucl. Sci.* **NS-26,** 5087 (1979).
6. E. L. Petersen, P. Shapiro, H. H. Adams, and E. A. Burke, "Calculation of Cosmic Ray Induced Soft Upsets and Scaling in VLSI Devices," *IEEE Trans. Nucl. Sci.* **NS-29,** 2055–2063 (1982).
7. W. E. Price, D. K. Nichols, P. R. Measel, and K. L. Wahlin, "Single Event Upset Sensitivity of Low Power Schottky Devices," *IEEE Trans. Nucl. Sci.* **NS-29,** 2064–2066 (1982).
8. J. A. Zoutendyk, "Modeling of Single-Event Upset in Bipolar Integrated Circuits," *IEEE Trans. Nucl. Sci.* **NS-30,** 4540–4545 (1983).
9. W. A. Kolasinski, R. Koga, and D. L. Chenette, "Heavy-Ion Induced Single Event Upsets in a Bipolar Logic Device," *IEEE Trans. Nucl. Sci.* **NS-30,** 4470–4474 (1983).
10. J. A. Zoutendyk, L. S. Smith, G. A. Soli, P. Thieberger, and H. E. Wegner, "Single-Event Upset (SEU) Model Verification and Threshold Determination Using Heavy Ions in a Bipolar Static RAM," *IEEE Trans. Nucl. Sci.* **NS-32,** 4164 (1985).
11. J. A. Zoutendyk, E. C. Secrest, and D. F. Berndt, "Investigation of Single-Event Upset (SEU) in an Advanced Bipolar Process," *IEEE Trans. Nucl. Sci.* **35,** 1573–1577 (1988).
12. R. Belt, D. Berndt, and G. Harvey, "SEU-Hardened Bipolar Flip-Flops," *J. Radiation Effects, Res. & Eng.* **6,** 121 (1988).
13. J. R. Hauser, "SEU Effects in Bipolar RAMs," *J. Radiation Effects, Res. & Eng.* **6,** 44 (1988).
14. G. R. Srinivasan, "Modeling the Cosmic-Ray-Induced Soft-Error Rate in Integrated Circuits: An Overview," *IBM J. Res. Develop.* **40,** 77–89 (1996, this issue).
15. P. C. Murley and G. R. Srinivasan, "Soft-Error Monte Carlo Modeling Program, SEMM," *IBM J. Res. Develop.* **40,** 109–118 (1996, this issue).

16. J. A. Dorler, J. M. Mosley, G. A. Ritter, R. O. Seeger, and J. R. Struk, "A 1024-Byte ECL Random Access Memory Using a Complementary Transistor Switch (CTS) Cell," *IBM J. Res. Develop.* **25,** 126–134 (1981).
17. G. R. Srinivasan, H. K. Tang, and P. C. Murley, "Parameter-Free, Predictive Modeling of Single Event Upsets due to Protons, Neutrons, and Pions in Terrestrial Cosmic Rays," *IEEE Trans. Nucl. Sci.* **41,** 2063–2070 (1994).

Received July 19, 1994; accepted for publication March 2, 1995

Leo B. Freeman *IBM Microelectronics Division, East Fishkill facility, Route 52, Hopewell Junction, New York 12533.* Dr. Freeman, currently retired, was a senior engineer in the Cache Design Department at the East Fishkill facility. He joined the IBM Components Division at East Fishkill in 1969, and worked on array and logic chip design for mainframe computers. Dr. Freeman received a B.S. in electrical engineering and a B.S. in engineering physics from Lehigh University, in 1963 and 1964, respectively. In 1965, he received an M.S. in electronics from Stanford University. He received his Ph.D. in electrical engineering from Lehigh University in 1969. Dr. Freeman retired from IBM in 1993.