The evolution of interconnection technology at IBM

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Advances in interconnection technology have played a key role in allowing continued improvements in integrated circuit density, performance, and cost. IBM contributions to interconnection technology over approximately the last ten generations of semiconductor products are reviewed. The development of a planar, back-end-of-line (BEOL) technology, used in IBM DRAM, bipolar, and CMOS logic products since 1988, has led to a threefold increase in the number of wiring levels, aggressive wiring pitches at all interconnection levels, and high-leverage design options such as stacked contacts and vias. Possible future BEOL technologies are also discussed, with emphasis on the use of higher-conductivity wiring and lower-dielectric-constant insulators. It is expected that their use will result in higher performance and reliability. Applications include future, lower-power devices as well as more cost-effective, higher-performance versions of present-day designs.

Introduction

Evolutionary and revolutionary advances in interconnection technology have played a key role in allowing continued improvements in integrated circuit density, performance, and cost. Over the last 20 years, circuit density has increased by a factor of approximately 10^4, while cost has constantly decreased [e.g., the historical 27% per year decline in price per bit for dynamic random access memories (DRAMs)]. Innovation in BEOL technology has been required in each technology generation, since only part of the density increase could be achieved with improvements in lithography. For example, cell areas for the last five IBM DRAM generations [1–5] are shown in **Figure 1**. Only a 2× decrease in cell area per generation would have been possible through lithography alone, whereas a 3× decrease has been required. The additional 1.5× decrease has come from innovation. Additional innovation will most likely be required in the future to continue this trend.

The key competitive metrics for a multilevel-metal interconnection technology are contacted metal pitch, number of levels of wiring, and maximum number of wired circuits per chip. Contacted pitch is the minimum metal line width and spacing plus additions for via or contact covers or landing pads. Usually DRAM chips use fewer levels of metallization than logic chips of the same lithographic generation, but often exhibit tighter first-wiring-level contacted pitch because of array wiring requirements. For static random access memory (SRAM) and logic chips, multiple levels of metallization at an aggressive contacted pitch are key to achieving high circuit density.

The interconnection technology currently used by IBM reflects a balancing of chip design requirements with manufacturing process options available for metallization,

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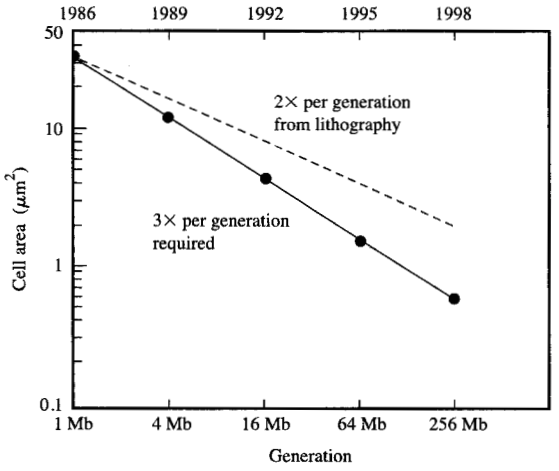

Figure 1

DRAM cell area vs. generation. From [5], reproduced with permission.

insulators, planarization, and patterning. Chip interconnections, or "interconnects," serve as local and global wiring, connecting circuit elements and distributing power [6]. To perform these functions, electrical properties (e.g., resistivity) must be optimized, but interconnects also function as the interface between chip and package, thereby also requiring stringent control of mechanical properties. High electrical and mechanical reliability must also be ensured for a successful interconnection technology. A planar multilevel metallization architecture [7] (introduced into IBM manufacturing in 1988) was the key innovation that improved interconnect structural integrity. Planarity was achieved by extensive use of chemical–mechanical polishing (CMP) [8] and chemical vapor deposition (CVD) of conformal metals (e.g., tungsten) [7]. Improving planarity provided improved electrical and mechanical properties for BEOL films, thereby enhancing reliability. Additionally, improved planarity facilitated continuous improvements in wiring pitch, number of metal levels, and design features such as stacked vias and local interconnects.

In this paper, we review contributions by IBM to interconnection technology over approximately the last ten generations of semiconductor products and discuss future interconnection technology requirements and opportunities. In addition, this paper serves as an introduction to the other papers presented in this issue.

BEOL evolution

Figure 2 shows the evolution of minimum first-wiring-level-contacted pitch for IBM logic and memory semiconductor products as a function of year of introduction into manufacturing. Several notable sections of the curves highlight technology changes. The 1975–1978 reduction in pitch for logic products was a result of the change from wet-etched Al-based wiring to the use of the lift-off patterning method [9]. The prevailing metal patterning technology in the early 1970s was wet subtractive etching, but this technique limited the ability to achieve tighter pitch because etching bias and tolerance were high for Al, and even worse for the Al(Cu) alloys used for electromigration resistance. Furthermore, wet etching undercut structures and formed holes in the metal at any recursive topography on the wafer surface. These factors drove IBM toward the use of a lift-off approach for metal patterning, introduced into manufacturing in 1975, for SAMOS metal-gated DRAMs.

The lift-off approach allowed significant improvements in contacted metal pitch compared to that achievable with wet etching [9], and continues to be used in some bipolar and CMOS logic chip products. However, as metal pitch was tightened with successive lithography generations, topography and reflectivity issues reduced the acceptable lift-off process window. The migration from lift-off to metal reactive ion etching (RIE) occurred in 1986, during 1Mb DRAM production.

In 1988, a planar BEOL technology was used in the fabrication of the 4Mb DRAM product [7]. The

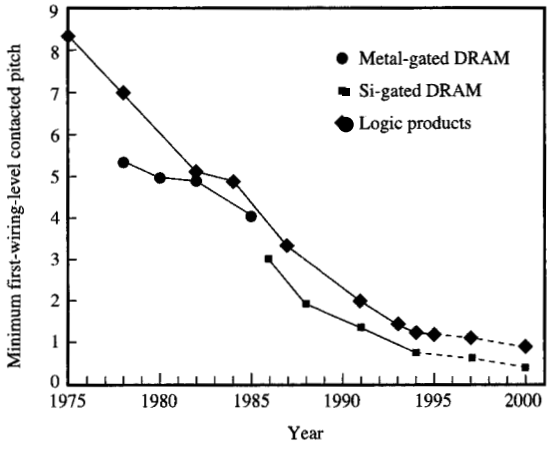

Figure 2

Minimum first-wiring-level contacted pitch as a function of year of introduction into IBM manufacturing.

combination of planarity and the use of W studs allowed further reductions in ground rules by allowing minimum lithographic dimensions to be used in interconnect fabrication. Improved planarity also allowed pitch reductions at upper wiring levels. For example, in 1978 the pitch of the second level of wiring (M2) for IBM logic products was 20 μm, whereas in 1994 upper-level wiring pitches were 1.8 μm [10, 11].

Metal polishing at via levels was the first microelectronics use of the metal patterning technique known as "damascene" (now in wide use in both DRAM and logic chip manufacturing). This technique involves etching trenches or vias in an insulating layer which is then filled with metal. CMP is then used to remove the extraneous material until only the metal in the trenches or vias remains. The damascene technique has been principally used for tight-pitch tungsten wiring and via levels, but is also extendable to other materials [12–14]. Its advantages include easier metal patterning (less sensitive to metal composition), easier lithographic alignment, improved planarity, better tool clustering logistics, and fewer process steps [15].

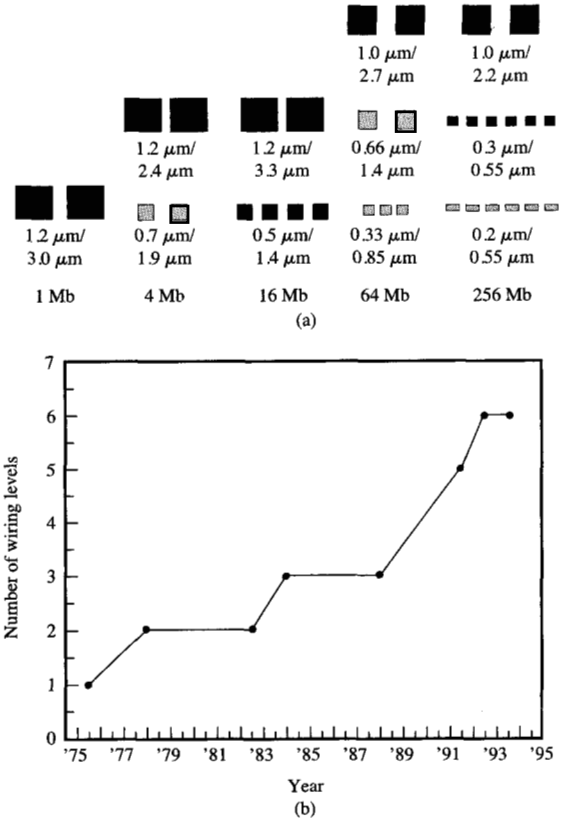

Figure 3

(a) Schematic of wiring levels of 1Mb–256Mb IBM DRAM products. Levels depicted in black represent Al(Cu)-based wiring; those depicted in grey represent W-based wiring. Values of wire thickness/minimum pitch are shown for each level. (b) Number of wiring levels vs. date of manufacturing introduction of IBM n-MOS and CMOS logic circuit products.

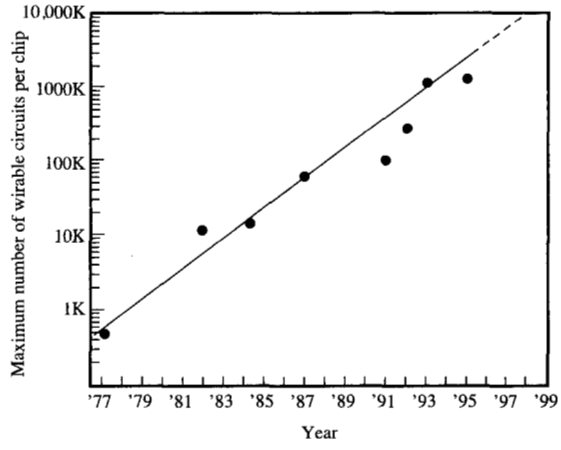

Figure 4

Maximum number of wirable logic circuits per chip vs. year of introduction into IBM manufacturing.

Figure 3(a) is a schematic of wiring levels over the last five generations of IBM DRAM products. The number of wiring levels for IBM n-MOS and CMOS logic circuit products is shown in **Figure 3(b)**. The available number of metal wiring levels has tripled over the last ten years for both logic and memory products. When the approaches used by IBM are compared with industry trends [16], it is apparent that tighter metal pitches have been used ahead of most of the industry. This advantage combined with a planar architecture has made it possible to produce chips having high circuit densities, as depicted in **Figure 4**. The maximum number of wirable logic circuits per chip vs. year of introduction into manufacturing is shown for various IBM chip technology generations, demonstrating that the number has increased by an order of magnitude every 5.5 years since 1977. In addition to considerable improvements in contacted metal pitch and planarity, increased circuit count for both DRAM and logic technologies has been made possible by increasing the number of metal levels, making use of stacked contacts and vias, and increasing chip size. More than one million wired circuits can now be contained on a single logic chip, in contrast to thirteen thousand just ten years ago. This is

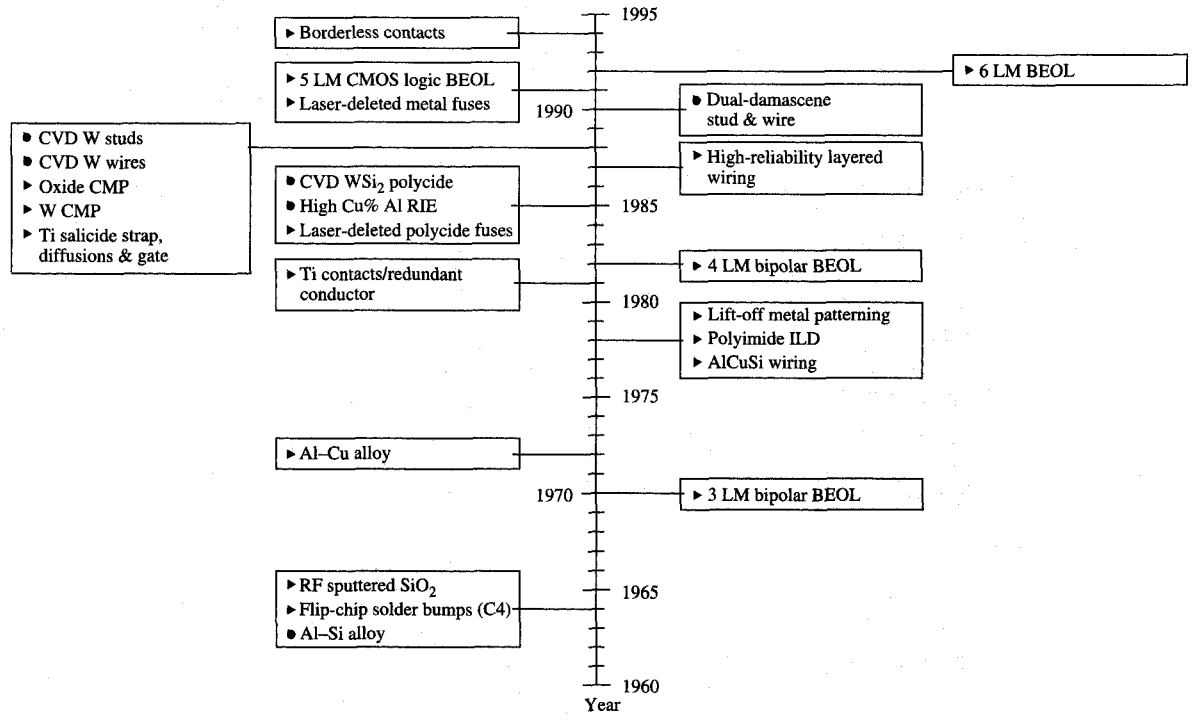

Figure 5

Chronology of key IBM interconnection technology introductions into manufacturing. Years of introduction are indicated. "LM" denotes levels of metallization.

consistent with even the most optimistic predictions of nearly a decade ago [17].

Enabling technologies

Over the years, IBM has pioneered a number of key interconnection technology advances. Many are now part of the mainstream processes of most semiconductor manufacturers. A chronology of the associated technology introductions is shown in **Figure 5**. Technology introductions are usually linked to product programs, as can be understood from the timing shown in the figure. In most cases, several introductions occurred within a year because they were part of the same product program. For example, CVD W wiring, CMP of metals and oxides, and titanium-salicided gates and diffusions were all introduced as part of the IBM 4Mb DRAM technology. It can also be discerned from Figure 5 that the rate of new technology introductions appears to be increasing.

The introductions occur for several reasons, including cost reductions, reliability enhancements, design requirements, or extendability to future products.

In many cases, innovations have more than one driving force. Cost reductions can result from either process step reduction/simplification or final yield enhancement. Al(Si) metallurgy [18], fuse technology advances, Ti contacts [19], and dual damascene structures [15] (see Figure 5) were all instituted to enhance yield, although each had the side benefit of widening process windows as well.

Al(Cu) alloy wiring is an example of an innovation directed at enhancing reliability. Al(Cu) alloys have been used since the late 1960s to alleviate electromigration concerns associated with Al(Si) metallurgy [20]. To further enhance reliability, IBM pioneered the use of thin layers of refractory metals, including the use of Ti, above and below the Al(Cu) alloy layers. The refractory metals reduce contact resistance and provide an immobile redundant layer capable of shunting currents over small voids, thus improving electromigration and stress-migration resistance [21]. It is believed that multilayered, Al(Cu)-based interconnects will persist as the chip wiring material into the late 1990s because of their pervasiveness and acceptance in the semiconductor industry. A multilayered conductor

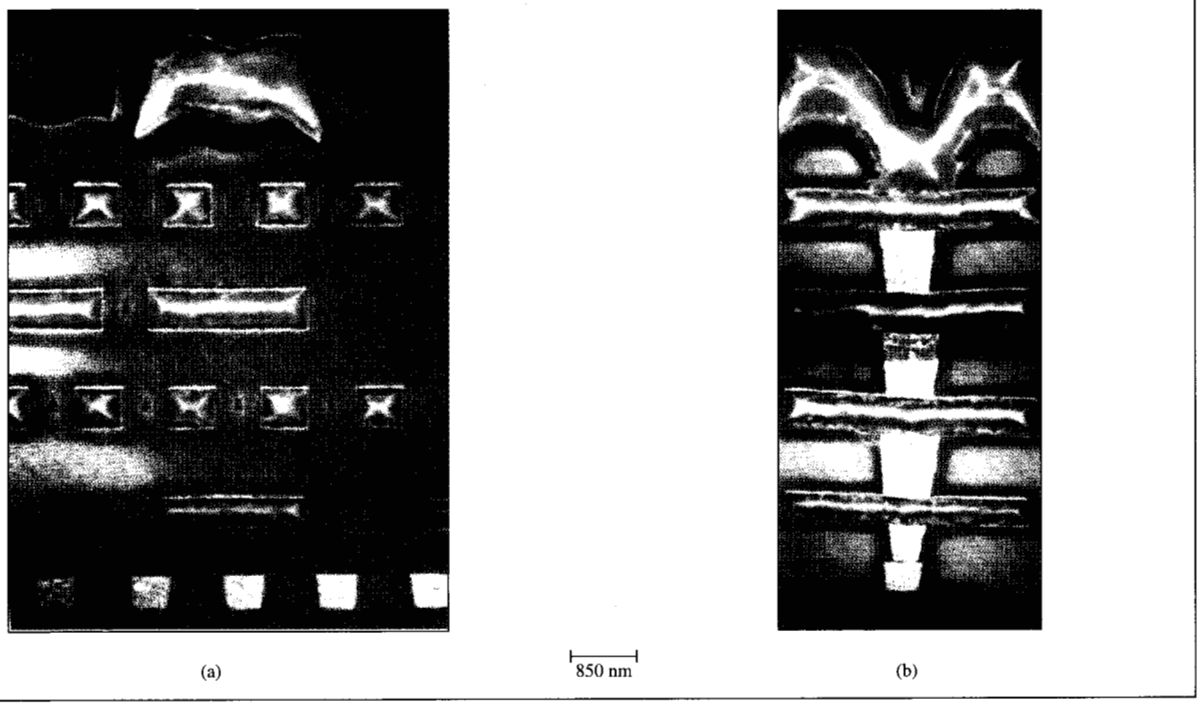

Figure 6

Scanning electron micrograph cross sections of structures fabricated using planar BEOL process: (a) BEOL portion of a 0.5-μm CMOS logic chip currently in production; note that a local interconnect level and five global interconnect levels are used. (b) Stacked contacts and vias. From [11], reproduced with permission.

approach is also used for tungsten-based wiring. Titanium is used in combination with titanium nitride as a liner beneath CVD W studs. The Ti contact material dramatically reduces contact resistance, while the TiN barrier layer improves contact stability, reliability, and W film adhesion [22].

Many innovations are driven by design requirements such as additional wiring levels [10, 11, 23], new materials (e.g., silicides [24]), or new structures (planar wiring [7], borderless contacts [3, 4, 12], solder bump "flip-chip" structures for off-chip connection [25]). Many unit process innovations are needed to successfully produce new design-driven, integrated structures. For example, Ti/TiN/CVD W [22], oxide CMP, and metal CMP were all developed in order to achieve planar BEOL structures. Often, revolutionary approaches are required to meet design needs, even though evolutionary change from the current manufacturing process is more easily accommodated. It is logistically undesirable to maintain multiple processes intended to produce similar structures for different products or generations of products. Therefore the extendability of a process innovation is a key criterion in ascertaining whether it is suitable for introduction into manufacturing. Processes that can be common to several product types or generations are needed for low-cost manufacturing. For example, the IBM lead–tin solder bump flip-chip technology for off-chip connection was developed in the 1960s and provides significant advantages which reduce chip wiring costs. Its key advantage occurs where power is delivered to a large chip and redistributed. Where edge connection (such as wire bonding) is used, long, wide, and thick buses must be used to deliver power to the correct point on the chip. By using the solder bump approach, these large buses can be fabricated in the package, thus allowing power to be delivered with low inductance. This technology is still viable today and is pivotal in reducing the cost of large, high-speed processors.

Current technologies

Planar BEOL technology has been used in IBM DRAM, bipolar, and CMOS logic programs since its introduction into manufacturing in 1988. A cross-sectional scanning electron micrograph of the BEOL portion of a 0.5-μm CMOS logic chip currently in production is shown in **Figure 6(a)**. A local interconnect level and five

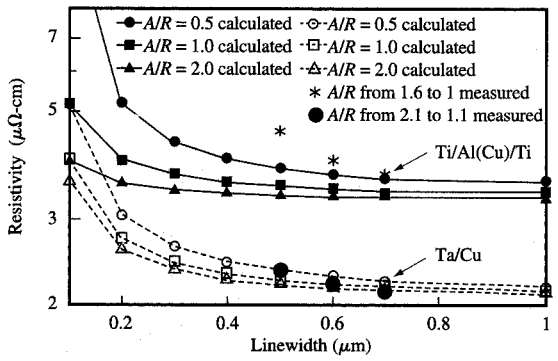

Figure 7

Comparison of effective resistivity vs. linewidth for damascene Cu wires having Ta liners and Ti/Al(Cu)/Ti wires patterned by RIE. From [29], reproduced with permission.

global interconnect levels are used. To improve manufacturability, a repetitive modular process flow is used in which the materials and sequence of steps are identical for each interconnect level. Only horizontal and vertical dimensions distinguish the different metal process modules.

The initial steps in the process flow to form the structure shown in Figure 6 are deposition and CMP planarization of the phosphosilicate glass (PSG) used to passivate the front-end-of-line (FEOL) portion of the structure. After polishing, a contact/local interconnect [11] mask is formed, and openings are etched in the PSG film to the titanium salicided gates and diffusions. After stripping the photoresist used for etching, Ti films are directionally deposited using collimated sputtering [13]. TiN films are then sputtered onto the Ti to act as a barrier and adhesion layer for CVD W, which is deposited next. CMP is used to remove excess metal, making the tops of the W studs and/or local wires thus formed coplanar with the PSG. If a local interconnect level is used (as in the figure), the process sequence is repeated to form W contact studs prior to formation of the first global interconnect level.

The process sequence described above is a significant departure from the reflowed boron–phosphosilicate glass (BPSG) sequence used by most device manufacturers. Utilization of PSG retains the ionic gettering properties required of this layer while simplifying chemical aspects and avoiding various crystalline defects associated with BPSG. The thermal processing requirements for this process sequence are less stringent than the requirements for BPSG reflow and are less likely to cause silicide agglomeration or other harmful device degradation. The CMP process yields better global planarization than the reflow process, as well as a wider lithographic process window for the critical first wiring layer. Finally, CMP oxide planarization is a prerequisite for utilizing W CMP for forming local interconnect or stud structures.

The first global wiring layer [Ti/Al(Cu)/Ti/TiN] is deposited, and photoresist is applied and patterned. This metal layer is then reactive-ion-etched using a chlorine-based plasma. A gap-filling oxide film is then deposited and subsequently planarized using CMP. A second oxide film is then deposited on the polished oxide to provide a dual interlevel dielectric. The application of the first via mask on this oxide surface is the initial step of the next wiring layer process. This set of process steps can be repeated as needed in order to form the total number of wiring levels required. The planar structure facilitates the use of stacked contacts and vias [**Figure 6(b)**]. The modular nature of the process also allows defect and reliability learning to be applied to all metal levels.

At the option of the device designer, the final level of wiring can be specified to be at the same tight pitch as the prior levels, or at a more relaxed pitch, using a thicker, lower-resistance conducting layer. A tapered via rather than a stud may be used with this latter option to reduce manufacturing costs. Planarization is not performed after the last wiring level. The final passivation layers (SiO_2/SiN_x/polyimide) are formed and patterned. The final via level also opens the fuse areas if redundant elements are used in the design. Connections to packages can then be made by means of flip-chip, tape-automated-bonding, or wire-bonding methods, depending on product requirements.

Some additional unique features of this modular process should be noted. The Al(Cu) films utilize an overlying and underlying, redundant $TiAl_3$ refractory layer, which has been shown to be relatively immune to reliability failures from either electromigration or stress-migration mechanisms. The lithographic process window at both metal and contact/via levels is relatively wide because of the superior global planarization obtained by using CMP and the incorporation of a TiN antireflective coating (ARC) as the uppermost layer of the interconnect stack. The interconnect deposition window is relatively wide because of the planarity of the surface between oxide and tungsten stud regions (i.e., step coverage is not an issue).

The key unit process choice for this technology was the extensive use of CMP planarization for both metals and oxide. Although the planarizing capability of CMP is excellent, it was also chosen for its ability to remove prior level defects [8] and to be part of a robust interlevel metal–insulator process. Dual-insulator schemes have proven to be relatively immune to interlevel metal shorting defects [9]. A process flow consisting of gap-filling oxide deposition/oxide polishing/cap oxide deposition is an extremely effective embodiment of this concept.

The tight metal pitches needed on multiple wiring levels require near-vertical, zero-overlap via studs. An alternative to forming W studs by means of CMP is to make use of reactive ion etchback; however, its use results in an extremely tight manufacturing process window and a process that is prone to yield and reliability defects. Any number of processes such as insulator deposition, via etching, photoresist removal, liner deposition, and W deposition can deposit particulates on the insulator surface. Chemically-vapor-deposited W is very conformal and uniformly coats these particles, effectively enlarging them. A significant amount of over-etching must be carried out to remove the W from these particulates during the etchback process. Any residual W or remaining particulates can cause shorting at subsequent interconnect levels. Over-etching also causes the studs to become recessed, building in steep topography that can cause reliability problems for traversing interconnect levels. In contrast, W removal by CMP is more desirable because all particulates from prior-level processes are thereby mechanically abraded from the insulator surface. Polishing times can be extended until all residual tungsten and liner materials are removed without recessing the stud.

Future BEOL technologies

Inevitably, devices will continue to diminish in size, and chip sizes will increase to provide ever greater function and cost benefits. If scaling is accomplished according to "ideal" rules [26], the supply voltage decreases by a factor S at a constant gate field, and the width of the metal lines connecting the devices decreases by the same factor. If the aspect ratio of the lines is maintained and insulator thickness is scaled as S, the capacitance per unit length does not change, but the resistance increases as S^2 and the current density increases as S. The cell area decreases as S^{-2}, as does the power dissipation. Thus, the power dissipation per unit area is independent of scaling.

Most high-performance systems are likely to be designed for general logic applications for which parallelism cannot be invoked to reduce the requirements of processor speed. These include ASICS and microprocessors which may be connected in various arrangements. In such small, higher-power systems, in which neither device voltages nor clock frequencies are reduced, the interconnection issues become even more critical. In such systems, the interconnections must accommodate increased current density, decreased wire width, larger chip size, increased tolerance to noise, and minimization of power variations across the chip, requiring reduced resistance and capacitance interconnections to maintain chip performance.

Scaling requirements are expected to cause wiring technology to evolve from Al-based conductors to Cu-based conductors. **Figure 7** shows a comparison of the effective resistivity, as a function of line width, of damascene copper wires having a 20-nm-thick Ta liner and Ti/Al(Cu)/Ti wires patterned by RIE and having 20-nm-thick Ti layers. The indicated aspect ratios (A/R) denote thickness-to-width ratios. The apparent discrepancy between the measured and calculated effective resistivity values of the Ti/Al(Cu)/Ti wires is due to compound formation during heat treatments, increasing their effective resistivity. Note the better agreement between the observed and calculated effective Cu (including Ta liner) resistivities. For a Ti/Al(1% Cu)/Ti wire having 20-nm-thick Ti layers, the calculated effective resistivity at the indicated A/R levels rises from 3.3 $\mu\Omega$-cm at 1-μm linewidths to about 5 $\mu\Omega$-cm at 0.1-μm linewidths. To avoid this, lower-resistivity metals such as copper must be utilized. Although silver has a lower resistivity than copper, copper-based conductors appear to be optimal, providing low resistivity and low cost with enhanced reliability. Silver is generally considered to be less useful for wiring because of its susceptibility to corrosion in the presence of weak oxidizing agents such as sulphur. The reduction in resistivity is not significant enough to warrant its use. Cu-based structures should not only improve performance, but are also expected to limit the rising costs associated with increasing the number of wiring levels in each generation. **Figure 8** shows that the use of lower-resistance conductors and lower-capacitance insulators should reduce the number of wiring layers required [27].

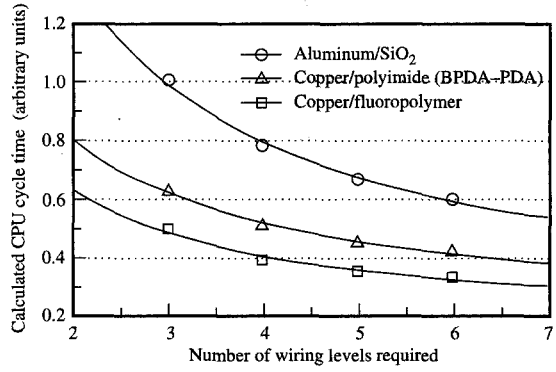

Figure 8

Calculated CPU cycle time as a function of the number of wiring levels for several combinations of conductors and insulators. From [27], reproduced with permission.

Table 1 shows that microprocessor chips have been increasing in size while providing more functionality. Improved cost and performance continue to be required, driving the need for new interconnection structures. For

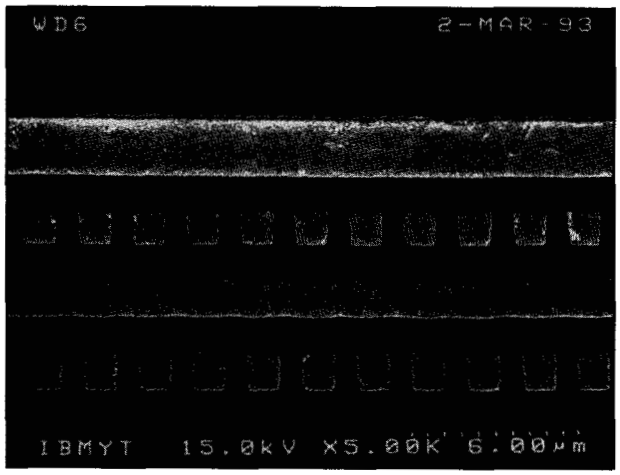

Figure 9

Scanning electron micrograph cross section of a test structure containing four levels of dual-damascene Cu-based wires integrated into a polymeric dielectric. From [14], reproduced with permission.

Table 1 Comparison of microprocessors from several manufacturers.

	Microprocessor	*Chip size* (mm)	*MHz*	L_{eff} (μm)
Intel®	80486	11.9 × 6.9	100	0.8
Intel®	Pentium®	13.3 × 12.3	100	0.8
IBM®	PowerPC 601™	8.6 × 9.5	100	0.5
Digital™	Alpha	12.8 × 12.8	275	0.5

Table 2 Potentially useful polymer insulators.

Material	*Dielectric constant*
-[O-$SiMe_2$-]-	2.3
-[-$SiPh_2CH_2CH_2CH_2$-]-	3.2
Siloxane polyimides	~3.7
-[-SiPhMe-]-	7.7
-[O-$SiMe_2$-Ph-$SiMe_2$-O-SiMe-O]-CH=CH_2	3.5
-[-$SiMe_2CH_2$-]-	2.8
Poly(trimethyl silylnorborane)	2.3
PMDA-ODA/polydimethylsiloxane copolymer	2.8

example, in cases where the density of circuits is to be increased markedly (e.g., in future low-power circuit chips), the reduction in power will probably be accomplished by use of a lower supply voltage and lower operating frequency. If the supply voltage (currently 5 V) were to be reduced to 1.1 V, the resulting power should be reduced by a factor of approximately 250. Note that as the voltage is reduced by a factor of 5, the device area decreases by a factor of 25 according to ideal scaling. The reduction in the operating frequency can be partially compensated for if parallelism can be used to implement the required functions—e.g., linear transformations of multiple data sets, such as are used in discrete cosine functions, which are at the heart of video codecs and other video processing functions. For such applications, although low-resistivity wiring is a key attribute, it is likely that capacitance of the wiring (unchanged with ideal scaling) will become a serious issue, especially for long nets which traverse the chip. Therefore, for such applications, there should be considerable benefit in reducing the dielectric constant of the BEOL insulators, since this reduces the drive current the devices must supply.

Insulator materials and layered structures have changed radically as new equipment and materials have become available. Sputtered quartz was used for several generations, but has been largely replaced by PECVD oxides and nitrides [28]. Combinations of hard insulators and polyimide have also been used [9, 14]. **Figure 9** shows a cross section of a test structure containing dual-damascene Cu-based wires integrated into a polymeric dielectric [14]. Use is made of a layered insulator structure of polyimide and PECVD silicon nitride. The damascene pattern is etched in the polyimide, and Ta and Cu films are then deposited. CMP is used to remove the metal, leaving Ta/Cu in the damascene pattern. PECVD silicon nitride is then deposited. The nitride prevents oxygen contamination of the Cu during subsequent processing and acts as a stop during the next polyimide etching step. The sequence is then repeated as needed to produce the required multilevel structure.

Future insulator structures will need to exhibit low dielectric constants (<3.0), be thermally and mechanically stable, adhere well, and integrate with other BEOL processes. Insulators having lower dielectric constants reduce crosstalk for a given conductor separation. **Table 2** contains a list of potentially useful low-dielectric-constant insulators which span the range of chemical composition from organosilicon to organic materials. As such, they represent a large range of mechanical, physical, and electrical properties. These insulators are unexplored as commercially useful microelectronic intermetal dielectrics, yet demonstrate some of the lowest dielectric constants of thermally stable polymers. Possible methods of incorporating them into wiring structures are described in Reference [29].

Although the phenyl- and silicon-containing polymers shown in Table 2 are more thermally stable than their

aliphatic counterparts, the inclusion of aromatic moieties into polymers (in this case phenyl groups) increases their dielectric constants. Poly(trimethyl silylnorborane) contains no phenyl groups; rather, it is an aliphatic material with ethylenic bonds in the backbone with a pendant trimethyl-silyl group. Although most of these materials exhibit property degradation at elevated temperatures, materials such as poly(methyl-silylphenylenevinylsiloxane) are stable to around 300°C.

To integrate insulators having low dielectric constants into a BEOL structure, they must be mechanically stable and must adhere to the other insulators as well as the metals used, and must withstand the polishing operations and thermal cycling associated with BEOL processing. Also, subsequently deposited films must adhere to them. Possible candidates include layered dielectrics that provide both etching control and a dual dielectric structure for yield and reliability. The ability to obtain etching selectivity during the patterning of organic and organosilicon polymers by using various plasmas, for example, is very attractive for process integration. If an organosilicon polymer with sufficient silicon content is coated with an organic polymer, the etching-rate ratio between the organic material and the organosilicon material in an oxygen plasma can easily approach 20:1 under conditions under which vertical polymer sidewalls are required [29]. Thus, the material used as an etching stop can be relatively thin, permitting stresses to be transferred through it.

Much of the current emphasis on process cost reduction is directed toward reducing the cost of planarization. In that regard, CMP has provided both the most optimal surface for adding further wiring layers and an appreciable challenge with regard to processing cost and yield. Depth of focus issues at small linewidths have driven this process to its present level of maturity, but further reductions in linewidth will increase the challenges of maintaining planarity over the optical field of the chip. Endpoint detection during CMP is difficult. Extensive measurements and inspections are often required to ensure planarity in cases where a material such as SiO_2 is "blind" polished (i.e., polishing controlled by time only; stopping within the SiO_2) [8]. Processes such as damascene patterning have been successful because of "built-in" polishing stops associated with the innate difference in polishing rate between dissimilar materials, allowing endpoints to be determined more easily. Although currently used primarily for tungsten patterning, the dual-damascene process is expected to be the patterning process of choice for future Cu-based interconnection structures.

Concluding remarks

Past, present, and future IBM contributions to interconnection technology have been reviewed and presented as a general introduction to the areas of wiring, insulators, planarization, and reliability described more completely in the other papers in this issue. The development of a planar BEOL technology is perhaps the key advance that has led to interconnection improvements over the last few generations. The availability of new wiring and insulator materials signals the advent of a new BEOL technology generation in the near future.

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