Preface

Rapid advances in silicon chip technology have resulted from progress made in both the "front end" of the chip manufacturing line, where circuit elements are fabricated, and the "back-end-of-line," where the elements are wired into integrated circuits. The relentless drive toward increased circuit count and device speed has necessitated both revolutionary and evolutionary changes in back-end-of-line manufacturing technology. To accommodate decreasing transistor size, wiring pitch must be reduced; to reap the benefit of increasing transistor speed, *RC* wiring delays must be contained; and to deal with increasing design complexity, wiring levels must be added. It is not surprising, then, that the fabrication of on-chip interconnections or "interconnects" has become difficult and costly. Moreover, these trends will certainly continue.

The evolution of processes for patterning chip metallization—from wet etching to lift-off to reactive ion etching—has permitted major reductions in wiring pitch. The development of a planar back-end-of-line approach, which incorporates the use of chemical–mechanical polishing to planarize interlevel dielectrics and metal stud levels, represents a significant advance in interconnect technology. These innovations and their impact on the IBM silicon chip technology are reviewed in the paper by J. G. Ryan et al. Also discussed in that paper are possible new directions involving the use of higher-conductivity wiring and lower-dielectric-constant insulators.

The advantages of using such new materials are elucidated in the paper by D. C. Edelstein et al. By simulations the authors demonstrate how geometry, materials properties, and processing details affect the performance of on-chip interconnects. On the basis of 2D and 3D calculations of interconnect resistances and capacitances and measured dielectric and signal propagation behavior, performance improvements resulting from optimizing a wiring design or from introducing a novel material can be evaluated at the chip and system levels. These calculations permit accurate comparisons among competing future alternatives.

As transistor size continues to decrease, contact resistance begins to play a significant role in circuit delay. Several types of silicides can be used to alleviate this problem. Circuit packing densities can be increased if some of the wires are replaced by "local interconnections." The paper by R. W. Mann et al. examines several state-of-the-art silicide and local interconnection processes, and their incorporation into IBM's manufacturing procedures.

The paper by T. J. Licata et al. describes methods for fabricating interconnects; these include a mixture of two different approaches. In one, a metal film is patterned by reactive ion etching into wires, followed by deposition and planarization of an insulator film. In the other, an insulator film is patterned with recesses, which are then filled with metal and planarized. The paper reviews the development and use of these processes in IBM manufacturing, and suggests that a "dual-damascene" process may become the future process of choice.

As indicated above, the metal reactive ion etching approach for forming interconnects requires the use of insulator films to fill the gaps between conductor wires. The paper by D. R. Cote et al. discusses the development of various chemical vapor deposition techniques aimed at enhancing the gap-filling capability of insulator films. The development of these techniques is presented through a review of the evolution of interlevel and intermetal dielectrics used in IBM DRAM products, ranging from the early 64Kb to the forthcoming 256Mb generation. The potential use of new, high-density plasma techniques is also discussed.

High current densities in the wiring and the thermal-expansion mismatches among the wiring, insulators, and silicon substrate can have pronounced effects on the reliability of on-chip interconnection structures. In evaluating the merits of present and future materials, processes, and structures with regard to reliability, it is critical to use appropriate testing structures and then realistically project accelerated failure data to field conditions. The paper by C.-K. Hu et al. covers relevant electromigration and stress-induced voiding phenomena, and discusses the validity of associated testing methodologies and physical models.

On-chip interconnection technology has been an exciting field, and will continue to be so for years to come. The papers in this issue of the *IBM Journal of Research and Development* cover many innovations that have become part of IBM's manufacturing technology and several that will potentially contribute to this technology in the future.

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