

Low-temperature chemical vapor deposition processes and dielectrics for microelectronic circuit manufacturing at IBM

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Significant progress has been made over the past decade in low-temperature plasma-enhanced and thermal chemical vapor deposition (CVD). The progress has occurred in response to the high demands placed on the insulators of multilevel microelectronic circuits because of the continuing reduction in circuit dimensions. High-aspect-ratio gap filling is foremost among these demands, which also include lower processing temperatures and improved dielectric planarization. This paper reviews the history of interlevel and intermetal dielectrics used in

microelectronic circuit manufacturing at IBM and the current status of processes used in IBM manufacturing and development lines, and describes the challenges for future memory and logic chip applications.

Introduction

There are a number of techniques available to deposit insulators in microelectronic circuit fabrication, but chemical vapor deposition (CVD) is by far the most important. We discuss both thermal and plasma-enhanced CVD [1-9]. Processing temperatures below 800°C are

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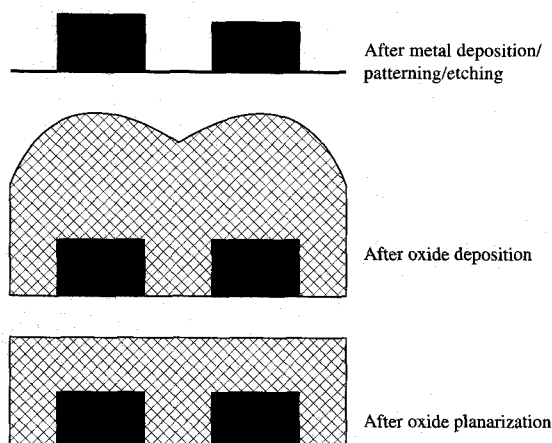


Figure 1

Typical process sequence for a multilevel interconnection structure fabricated by subtractive etching of the metal followed by oxide deposition and planarization. It is critical that the oxide fill the gaps between the metal lines without the formation of voids.

required to maintain shallow junction depths [10] and avoid agglomeration of transition metal silicides used either in silicided junctions or as part of the gate conductor [11–13]. For the Al(Cu)-based interconnect layers, processing temperatures below 450°C are required, since the metal degrades rapidly above this temperature, forming voids and hillocks [14].

Among the insulators used are silicon dioxide and doped silicate glasses. They are easily patterned by reactive ion etching (RIE) and can possess good chemical and mechanical stabilities. Such films can also exhibit moderately low dielectric constants and very high electrical resistivities. It is more difficult to deposit high-quality CVD oxide films at low temperatures [1], because by-products of the chemical reaction, i.e., hydrogen, water, and hydroxyl groups, can be incorporated into the film. These by-products can reduce the device performance and stability. The presence of water increases the dielectric constant and thus decreases circuit speed [6, 15]. Water also aggravates hot-carrier-induced device degradation by diffusing into the gate oxide [16]. Hydrogen and absorbed water also make the insulator less dense or can outgas from the insulator during subsequent thermal steps, causing a change in film stress. This stress change in the insulator can lead to cracking or delamination [17]. Clearly, insulator quality must be very high for reliable device performance, stability, and mechanical integrity.

Originally, the primary source material for low-temperature CVD insulators was silane [18], since it oxidizes easily at temperatures less than 500°C. Silane has been used in low-temperature atmospheric pressure chemical vapor deposition (APCVD) of oxide [19], phosphosilicate glass (PSG) [20, 21] and borophosphosilicate glass (BPSG) [22], and in plasma-enhanced chemical vapor deposition (PECVD) of oxide [23] and nitride [24] layers. CVD of oxide layers by the reaction of tetraethoxysilane (TEOS) and oxygen was reported as early as 1961 [25, 26]. TEOS was subsequently used in semiconductor manufacturing in high-temperature, low-pressure chemical vapor deposition (LPCVD) applications, but the use of TEOS as a source for PECVD was not common until the late 1980s [27]. The PECVD TEOS oxide films have much better step coverage than silane-based oxide films; this improvement in step coverage was fully exploited for gap-fill applications. APCVD [28] and later subatmospheric chemical vapor deposition (SACVD) [29] of oxide layers by the reaction of TEOS and ozone also showed a dramatic improvement in gap filling (or simply “gap fill”) compared to the silane-based APCVD processes, making APCVD and SACVD extendible to sub-half-micron applications.

We discuss two primary applications for low-temperature CVD of insulators: 1) as an interlevel dielectric (ILD) for the passivation of the polysilicon gate conductor in field-effect transistor (FET) devices, and 2) as an intermetal dielectric (IMD) between aluminum/copper or tungsten interconnects. Low-temperature CVD of dielectrics for final passivation is not covered in this paper. Once the coverage and thickness of the insulators (typically PECVD oxide, PECVD nitride, and polyimide) have been optimized, the remaining issues at this level are mainly chip/package interactions [30, 31].

Insulators for multilevel interconnections are commonly deposited by CVD on top of metal layers that have been patterned with reactive ion etching (RIE). Typically, oxide deposition is followed by partial planarization using spun-on-glass [32–34] or resist etch-back techniques [32, 35–37] and more recently by global planarization with chemical-mechanical polishing (CMP). A typical process sequence is shown in **Figure 1**. The oxide must fill the spaces between the metal lines without leaving voids. If the voids are exposed during the subsequent planarization or during the patterning of the next wiring level, metal will easily deposit into the void and form an electrical short. Filling these spaces is difficult when they approach sub-half-micron size.

Another technique used to build a multilevel interconnection structure is known as the “damascene” technique. In this technique, an oxide is deposited on a planar surface and the wiring level is patterned (by lithography and etching) into the oxide, forming trenches.

Metal is then deposited and subsequently removed by CMP, using the oxide as a polishing stop. The metal remains only in the patterned trenches in the oxide [38–40]. The damascene technique is illustrated in **Figure 2**. With this technique, the oxide does not have to fill the gaps between the metal lines; the burden of gap fill lies on the metal, not the oxide. Currently, tungsten is the only metal being used in damascene processing in IBM manufacturing. Since the resistivity of tungsten is approximately three times higher than that of aluminum, the damascene process is used only for applications where line resistance is not critical. Because it is expected that aluminum-based lines formed by RIE will be the mainstay for current and future logic generations, dielectric gap fill will remain a key requirement.

In addition to filling gaps between metal lines, low-temperature insulators must also fill spaces between polysilicon gate conductor lines in a circuit containing MOSFET devices. The spaces between the gate conductor lines are usually smaller than those found in the upper wiring levels, and thus more difficult to fill. The aspect ratios (height of the line divided by the distance between the lines) are typically two to four times larger for the gate conductor level. Doped silicon oxide films such as PSG and BPSG [15] are the preferred insulators for polysilicon gate conductor lines. The general process steps include film deposition followed by thermal densification, reflow, and either sacrificial etch-back or CMP processes. The phosphorus provides protection against mobile ion contamination [41, 42]. In addition, phosphorus- and boron-doped oxides provide high etch selectivity to nitride and undoped oxide, making such oxides desirable materials for etching [43]. Most significantly, boron and phosphorus doping in BPSG allows the use of low-temperature reflow for improved gap fill and planarization. An additional advantage of PSG and BPSG is that they polish 1.5–3 times more rapidly than undoped films, making it cost-effective to use CMP.

A primary concern for ultra-large-scale integrated (ULSI) circuit fabrication is process-induced damage to the gate oxide. Such damage leads to significant device yield loss [44] and reliability problems [45]. Rakkhit et al. [46] have shown that process-induced damage is cumulative as wafers are processed through the BEOL (back end of line). Since advanced integrated circuit fabrication typically involves many plasma-based processes, it is of the utmost importance to isolate and minimize all levels of charge damage throughout the process flow. Charge build-up and damage effects have been reported for plasma etching [47–51] and plasma deposition [44, 45, 51–53].

As an example, we describe the gate oxide degradation in 64Mb DRAM product chips due to PECVD PSG process-induced charge damage, along with our methodology for isolating, fixing, and eliminating the

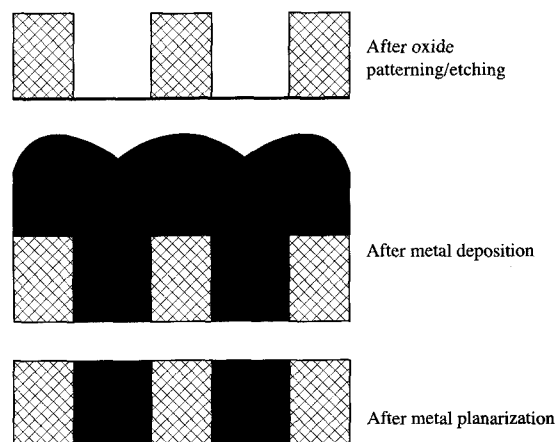


Figure 2

Typical process sequence for multilevel interconnection structure fabricated using the damascene technique. Note that the metal, not the oxide, must now fill the gaps.

charge damage. Reduced device damage in advanced deposition technology such as electron cyclotron resonance (ECR) and helicon plasma deposition is also discussed.

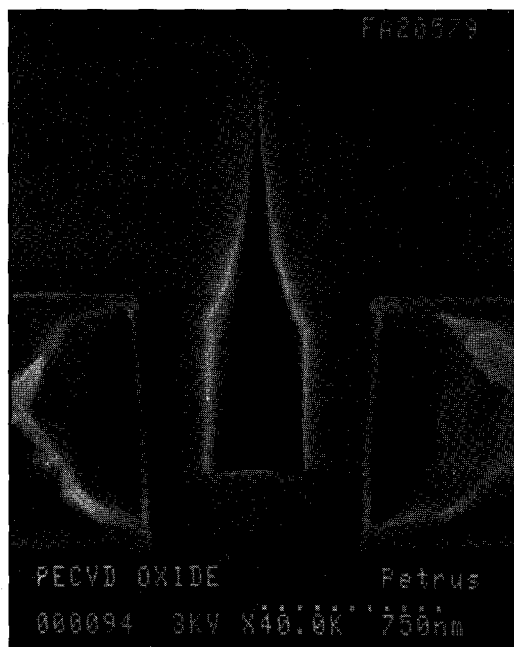
In addition to conventional CVD silicon nitride and oxide films [3–9], there are many other CVD dielectric films (and associated processes) being studied for advanced ULSI applications. We present some recent advanced CVD processes that are being explored for quarter-micron complementary metal oxide semiconductor (CMOS) circuit fabrication. There are other dielectric materials being examined for future applications, such as organic dielectrics for copper interconnects [39]. However, such topics are beyond the scope of this paper.

Historical perspective

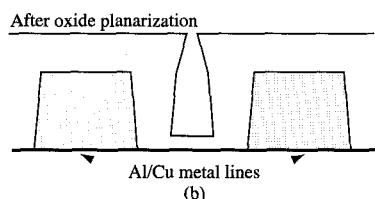
We discuss the evolution of interlevel and intermetal dielectrics using dynamic random access memory (DRAM) chips as the vehicle. For both logic and memory devices and circuits, a significant driving force behind recent technological advances has been the need to fulfill more demanding gap-fill requirements. This discussion is meant to be a survey of the main processes used by IBM, and therefore is not all-inclusive.

• Early-generation DRAM (64Kb, 256Kb, and 1Mb) products

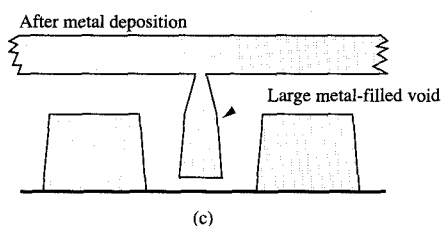
For early-generation DRAM product chips, a variety of techniques were used to deposit passivation dielectrics.



(a)



(b)



(c)

Figure 3

(a) SEM cross section of structure containing PECVD oxide deposited by the reaction of silane and nitrous oxide; an intervening void is the result of the poor step coverage associated with the process. (b) Schematic of the structure after planarization and (c) after metal deposition, indicating likelihood of an intralevel metal short due to the presence of a void.

Beginning with the 64Kb DRAM chip, bias-sputtered quartz and spun-on polyimide were used to insulate the Al(Cu) gate from the next (and final) level of metal wiring. For the 256Kb DRAM product, use was made of a CVD

nitride/spun-on polyimide passivation because of the then-unacceptable particulate levels and low deposition rates associated with bias-sputtered quartz processing. For the 1Mb DRAM product, use was made of polysilicon rather than Al(Cu) gates, allowing more flexibility in the choice of the gate insulator. PSG was deposited onto production wafers at atmospheric pressure using phosphine, silane, and oxygen as the reactants and subsequently reflowed at high temperature, conditions similar to those reported by Kern [54]. Since the 1Mb DRAM product was designed with only a single level of metal at a pitch (line plus space) of $3.0\text{ }\mu\text{m}$, PECVD nitride followed by spun-on polyimide sufficed as the metal passivation.

• 4Mb DRAM product

The reduction in device dimensions from the 1Mb to 4Mb DRAM product chips caused major changes for both interlevel and intermetal dielectric processes. Shallower source/drain junctions reduced the overall thermal budget and limited subsequent heat treatments to below 900°C . The requirements to fill the narrow spaces between the gate conductor lines, and better planarization, drove the migration to a different doped glass for the polysilicon-metal interlevel dielectric. To modify the 1Mb PSG process to reflow at a lower temperature, it would have been necessary to increase the concentration of the phosphorus. Corrosion of metal and device performance was a concern because of the possibility of phosphoric acid formation at high phosphorus concentrations [55]. Therefore, in order to obtain good reflow at a lower temperature (800°C), PSG was replaced with BPSG for the 4Mb DRAM product chips. BPSG was deposited at atmospheric pressure using silane, oxygen, diborane, and phosphine as the reactants. This process was compatible with the salicide gate conductor and filled the submicron spaces easily. Although reflowed BPSG provided sufficient local planarization, there were defect problems associated with the low-temperature BPSG deposition and 800°C reflow. The main problem was hydrolysis of boron oxide in the BPSG, which resulted in the appearance of boric acid crystals on the wafer surface and prompted further changes in the planarization process. Eventually, the BPSG was capped with a thermal silane oxide, then planarized using CMP. The advent of oxide CMP opened the door for important developments in low-temperature dielectric gap fill, since planarization was no longer a deposition issue.

A different approach was required to fill the spaces between the metal lines for the $1.9\text{-}\mu\text{m}$ pitch (line = $0.9\text{ }\mu\text{m}$, space = $1.0\text{ }\mu\text{m}$) with a reliable insulator. CVD nitride and polyimide could not adequately fill the spaces between the metal lines and left voids. Also, nitride has a high dielectric constant, leading to an increase in coupling capacitance. Bias-sputtered quartz was ruled out as a

metal passivation candidate because of the aforementioned limitations of deposition rate and high particulate levels. The step coverage of the available APCVD silane oxide films was poor, causing voids to be formed between the metal lines. PECVD oxide deposited by the reaction of silane and nitrous oxide also had poor step coverage, as shown in **Figure 3(a)**. The PECVD silane oxide is a nonconformal film (i.e., less oxide is deposited on the vertical sidewalls than on the horizontal surfaces), and there is a considerable amount of cusping, giving it a "breadloaf" profile. As the deposition progresses, it pinches off, leaving a large void or "keyhole" between the metal lines. The void might be opened up during the subsequent planarization and/or via etch of the dielectric, as shown in **Figure 3(b)**. CVD metal, e.g., tungsten, can easily fill such an exposed void, creating a likely pathway for shorting, as shown in **Figure 3(c)**.

Therefore, an innovation in intermetal dielectric processing was required in order to fill the smaller spaces of this new DRAM generation. In 1983, planarization of silicon nitride and PSG argon by sputter-etching was reported [56]. Although the sputter-etching was used as a final planarization step in this particular process, it became clear that sputter-etching thinner oxides over smaller features would taper the sidewalls and thus open structures for easier dielectric filling. The idea of dielectric deposition followed by argon sputter-etch and a second dielectric deposition for gap fill was conceived¹ and was later described in the literature [57, 58].

"Dep-etch" process for intermetal dielectric gap filling

The dep-etch process (deposition followed by argon sputter-etching) can be illustrated with a simple three-step sequence. Sputter-etching in argon physically removes oxide from all surfaces by ion bombardment. Faceting occurs, since the sputter-etching rate depends on the angle of argon ion incidence and is faster at the top corner of the oxide. Backscattering results in the deposition of a small amount of the oxide on the sidewalls, as shown in **Figures 4(a) and 4(b)**. For optimum filling, the reduction of oxide thickness should be about 10% of the height of the line. The taper should extend from the top of the oxide to the bottom of the oxide that lies between the lines. Sufficient oxide should be deposited so that the sputter-etching does not extend to the corners of the underlying lines; the oxide thickness should be about five times that removed by sputter-etching. The etching tapers the sidewalls to the bottom of the gap such that the final deposition fills the space easily [**Figure 4(c)**].

The dep-etch process fills the narrow spaces but does not leave a planar surface. In many applications, it is

¹ W. J. Cote, unpublished internal communication, IBM Corporation, Essex Junction, VT, February 1984.

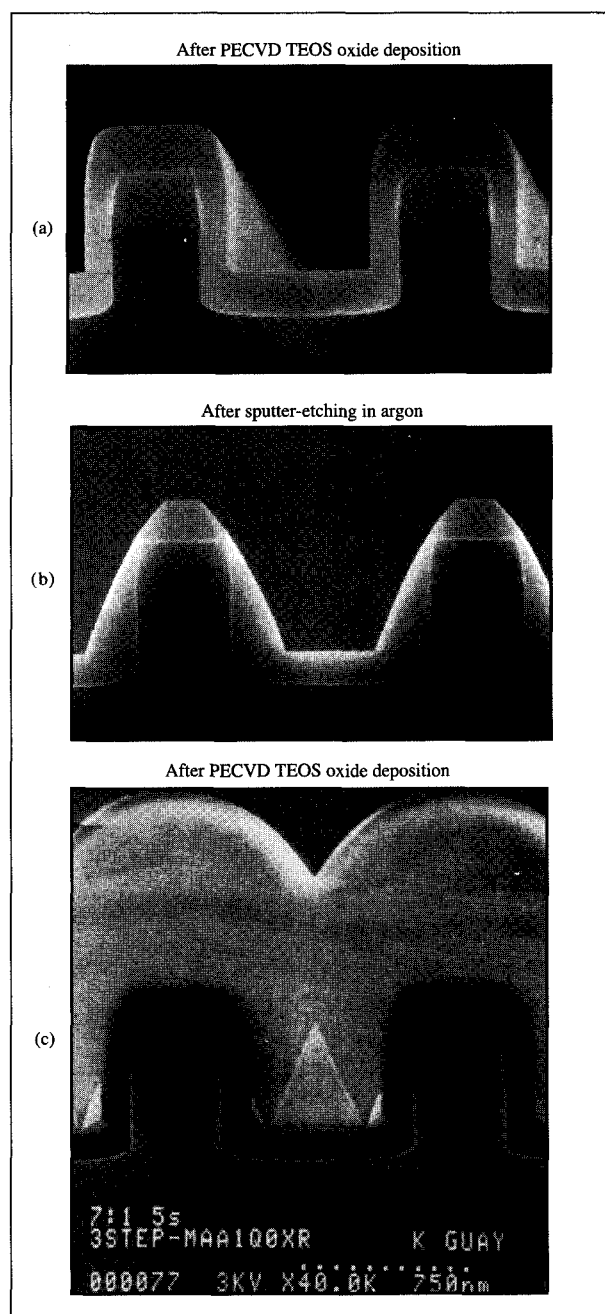


Figure 4

SEM cross section of PECVD formed by a three-step dep-etch-dep process: (a) PECVD oxide after deposition, (b) argon sputter-etching, and (c) a second PECVD oxide deposition. The samples used for (a) and (b) were decorated with KOH; that used for (c) was highlighted with 7:1 buffered HF to delineate the etched layer and redeposited oxide on the sidewalls.

necessary to globally planarize the dielectric prior to fabricating the next metal wiring level. For example, planarity is important when fabricating tungsten studs,

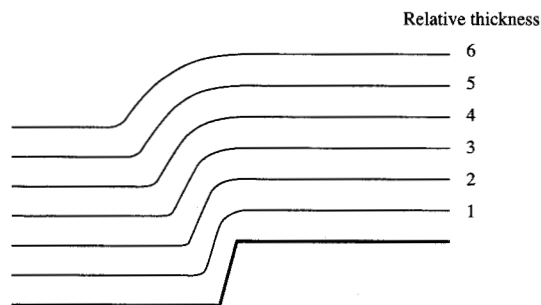


Figure 5

Typical experimental profiles (shown schematically) of as-deposited THCVD TEOS-ozone oxides of different thicknesses in the vicinity of the edge of a metal line. The use of a thicker oxide results in a shallower slope after etch-back. From [60], reproduced with permission.

since nonplanar areas in the oxide are filled with tungsten after metal CMP or etching by RIE. Therefore, the intermetal dielectric for the initial version of the 4Mb DRAM product evolved into a three-step dep-etch process: a dep-etch-dep of PECVD silane oxide followed by oxide CMP for planarization. (See below for comments regarding the later version of the product.)

◆ 16Mb DRAM product

For almost a decade, dep-etch multistep sequences have been the primary means to eliminate voids between minimum-space lines. Initially, the dep-etch process was demonstrated at IBM using PECVD silane oxide deposition on one tool and argon sputter-etching on a separate tool. During the early manufacturing of the 4Mb DRAM product, this multistep process was implemented in a single-chambered batch tool. Since the tool was not automated from a loading and cleaning perspective, multistep processing in the same chamber was difficult. It became evident that the use of a multichamber cluster tool would improve cycle time because of its automated handling features, and would reduce defect density (because of chamber dedication for deposition and argon sputtering processes). Therefore, a clustered tool was sought to meet the dielectric fill requirements for the 4Mb DRAM product and beyond. In 1987, a single-wafer, multichamber cluster tool [59] capable of performing both deposition and etching processes was introduced into the 16Mb DRAM (125-mm-diameter wafers) development line and soon afterward into the 4Mb DRAM (200-mm-diameter wafers) manufacturing line.

This single-wafer cluster tool also made possible the development of a high-quality TEOS-based PECVD oxide.

This came about because a single-wafer chamber permits the use of relatively high power densities, which in turn facilitates complete reaction of the TEOS and oxygen to silicon oxide. Early attempts at TEOS-based silicon oxide deposition in batch tools resulted in the formation of low-quality oxides, mainly because of the use of lower power density levels. TEOS-based PECVD oxide provided a marked improvement in film conformality over silane-based PECVD films (about 15–20%).

Additionally, low-temperature, thermally deposited TEOS films deposited by the reaction of TEOS and ozone at 40–60 torr could be deposited in the same chamber. We refer to this process as the thermal (THCVD) TEOS-ozone process, although it is sometimes referred to in the literature as the low-pressure (LPCVD) TEOS-ozone process. THCVD TEOS-ozone films showed excellent results in step coverage: nearly 100% conformality [1]. Silicon oxide films deposited by organosilicon and ozone precursors have been reported since 1971 [28], but several years were required before the process became more widely accepted, since the quality of the films obtained was not as good as that of those obtained using PECVD TEOS. THCVD TEOS-ozone films have lower deposition rates and higher wet-etching rates, and exhibit tensile stresses compared to PECVD films [1]. In addition, THCVD TEOS-ozone films are more hygroscopic than PECVD films. Nevertheless, their excellent conformality made them desirable for gap filling and therefore warranted further testing for an intermetal dielectric application.

A PECVD TEOS/TEOS-ozone "sidewall spacer" intermetal dielectric process

The tighter pitch for the 16Mb DRAM product (1.4- μm pitch, line width = 0.6 μm , line spacing = 0.8 μm) placed a high demand on the intermetal dielectric process. An improved intermetal dielectric process developed using both the CVD and etching capabilities of the cluster tool was implemented in the 16Mb DRAM process [60]. By using both PECVD and THCVD TEOS-ozone oxide films with argon sputter-etching and anisotropic oxide etching, a high-quality, void-free, partially planarized intermetal dielectric was developed. The first two steps in the intermetal dielectric process include a PECVD TEOS oxide layer that is deposited over the underlying wiring layer and subsequently faceted by argon sputter-etching. The PECVD TEOS oxide is in compressive stress ($\approx 1.0 \times 10^9$ dynes/cm²). Moderately compressive oxide films are desirable for passivating and insulating layers because they resist cracking and minimize stress-induced voiding in the Al(Cu) interconnect layers [61]. Next, a thick layer (at least 5000 Å thick) of THCVD TEOS-ozone oxide is deposited and fills the gaps. Since the electrical and

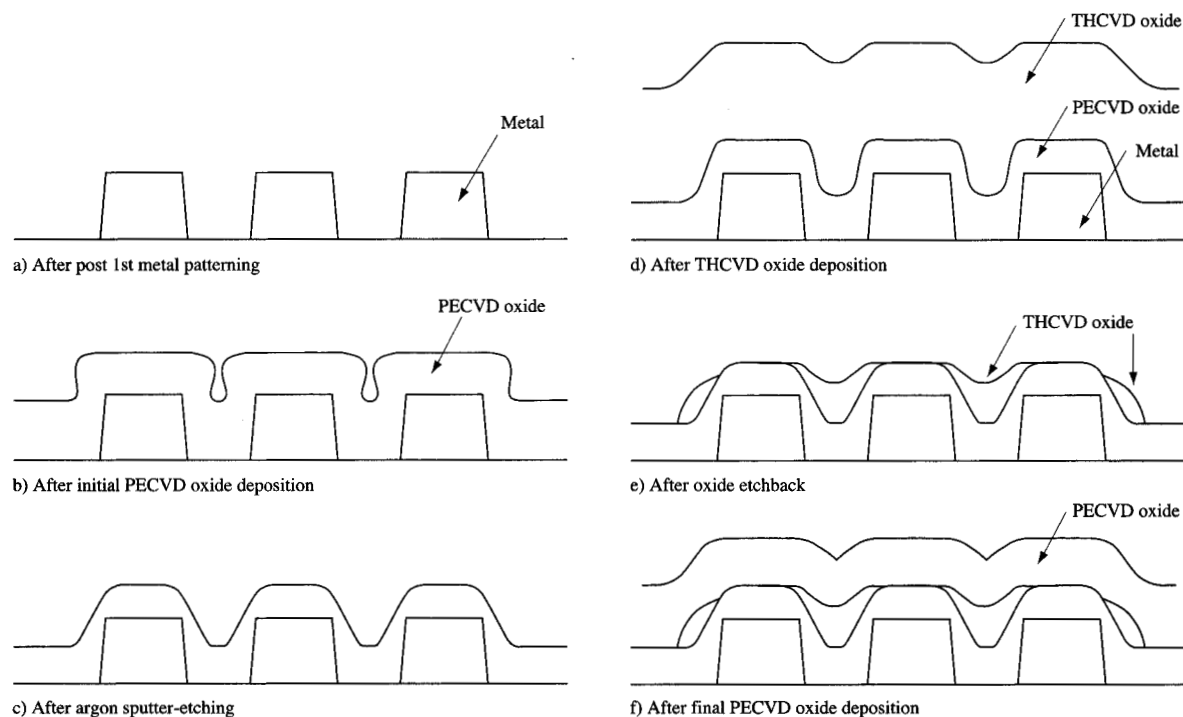


Figure 6

Summary of the PECVD TEOS/THCVD TEOS-ozone "sidewall spacer" intermetal dielectric process. From [60], reproduced with permission.

physical properties of THCVD TEOS-ozone oxide are generally poorer than those of PECVD TEOS oxide, it is desirable to remove most of the film with an anisotropic CF_4/O_2 etch-back. All of the THCVD TEOS-ozone oxide is removed from the horizontal surfaces; it is left in the minimum spaces and as spacers on the sidewalls of the metal lines. These sidewall spacers determine the slope of the dielectric over metal lines: An increase in the initial THCVD TEOS-ozone oxide thickness produces shallower slopes after etch-back, as shown in **Figure 5**. The final layer of PECVD TEOS oxide completes the total desired intermetal dielectric thickness. This intermetal dielectric process provides a smoothed, but not planar, surface between the first- and second-metal layers. Since the dielectric is not planarized, the slope of the dielectric over the metal lines is critical. If the dielectric slope is too steep, metal "stringers" form in the valleys between the metal lines when the next metal wiring level is etched, causing electrical shorts. A summary of the intermetal dielectric process sequence is shown in **Figure 6**.

Dep-etch PSG for polysilicon-metal interlevel dielectric

The use of titanium silicide junctions in the 16Mb DRAM product placed restrictions on the passivation process. Reflow temperatures for PSG and BPSG (greater than 1000°C and 800°C , respectively) are high enough to cause agglomeration of the titanium silicide [11]. Instead, PSG could be deposited by PECVD (with TEOS, oxygen, and trimethylphosphite) in the multichamber tool and incorporated in a dep-etch process, permitting the use of PSG to fill the gaps. The availability of oxide CMP eliminated the need for reflow. The 16Mb DRAM interlevel dielectric process became a low-temperature PECVD PSG dep-etch in the multichamber tool, followed by CMP planarization [62].

The 16Mb DRAM product required the use of a five-step dep-etch-dep-etch-dep to fill the critical gaps between gate conductor lines. The first PSG deposition thickness was determined by the maximum thickness that did not pinch off the smallest gap. This was followed by an argon sputter-etching that tapered the PSG to the corner of the

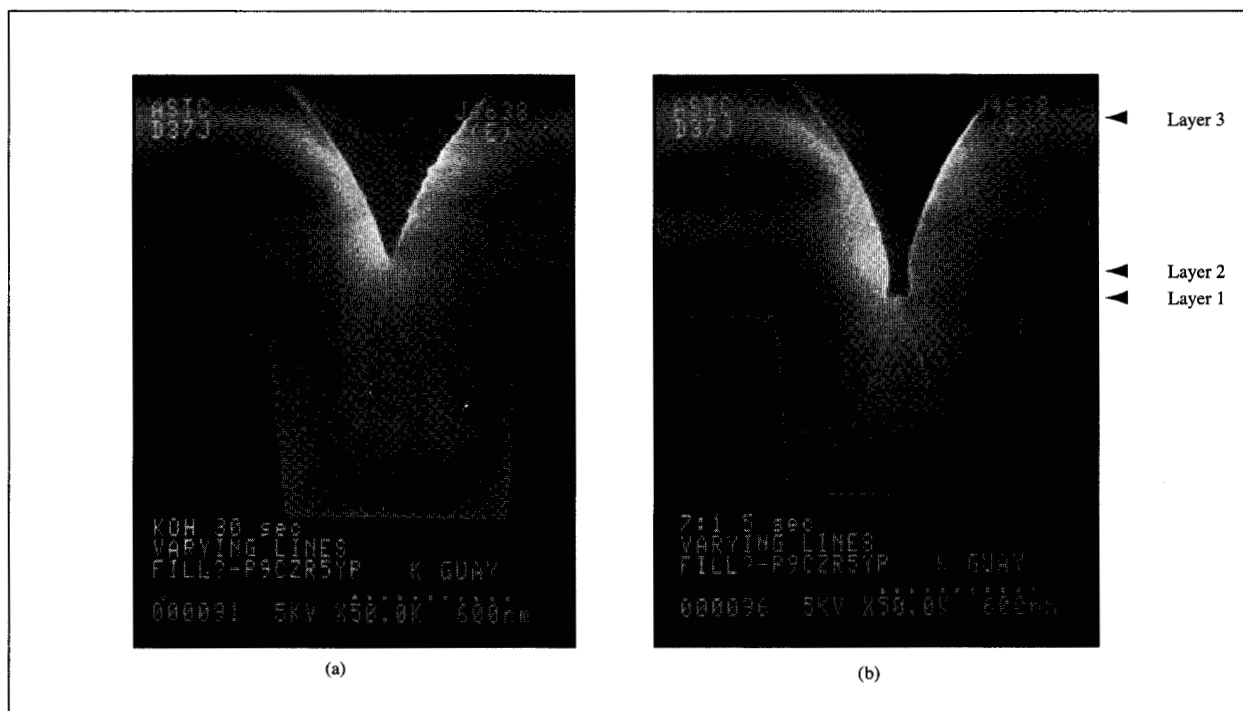


Figure 7

SEM cross sections illustrating a five-step dep-etch of PECVD PSG on a silicon trench monitor: (a) Sample decorated with KOH to decorate the silicon. (b) Sample decorated with 7:1 buffered HF to indicate the dep-etch layers and proximity of each layer to the corner of the structure. The first two layers must be sputter-etched right to the corner of the structure in order to achieve desired gap filling.

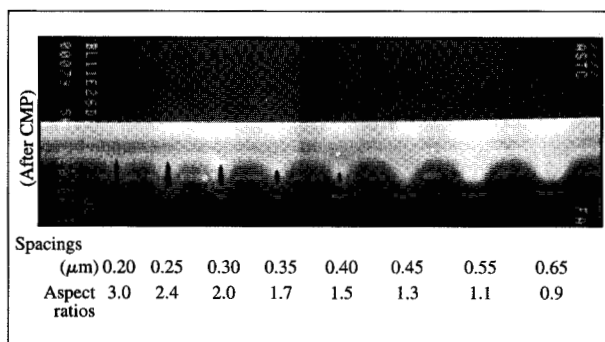


Figure 8

Five-step dep-etch of PECVD PSG over the gate conductor. This SEM was taken of a sample containing different gate conductor spacings in order to ascertain when voids begin to form. Voids are formed in spaces less than $0.45 \mu\text{m}$ wide.

gate conductor. This sequence was repeated: The second PSG deposition was again kept thin enough to avoid closing the smallest gap, and then faceted again to the

corner of the gate conductor. The clustered interlevel dielectric process also includes a thin PECVD silicon nitride film deposited before the PSG by the reaction of silane, nitrogen, and ammonia at 480°C . This nitride acts as a mobile ion and diffusion barrier. An illustration of a five-step dep-etch of PECVD PSG (without a nitride barrier) is shown in **Figure 7**.

◆ 64Mb DRAM product

Even a five- or seven-step PECVD PSG dep-etch process will not fill in the sub-quarter-micron minimum spaces between the gate conductor lines in the 64Mb DRAM product. Though the nominal aspect ratio is 3:1, design rules allow a worst case of 5:1. Large voids form in the PSG for spaces less than $0.45 \mu\text{m}$, as indicated in **Figure 8**. **Figure 9** shows how these voids cause problems in the subsequent damascene metal wiring. The first step in damascene wiring fabrication is to planarize the PSG with CMP. Next, an undoped oxide is deposited on top of the PSG, patterned with resist, and etched. Since the PSG void is close to the top of the PSG surface, the void can be intersected during the etching (there is an over-etch into the PSG). The CVD tungsten used for the metal wiring fills

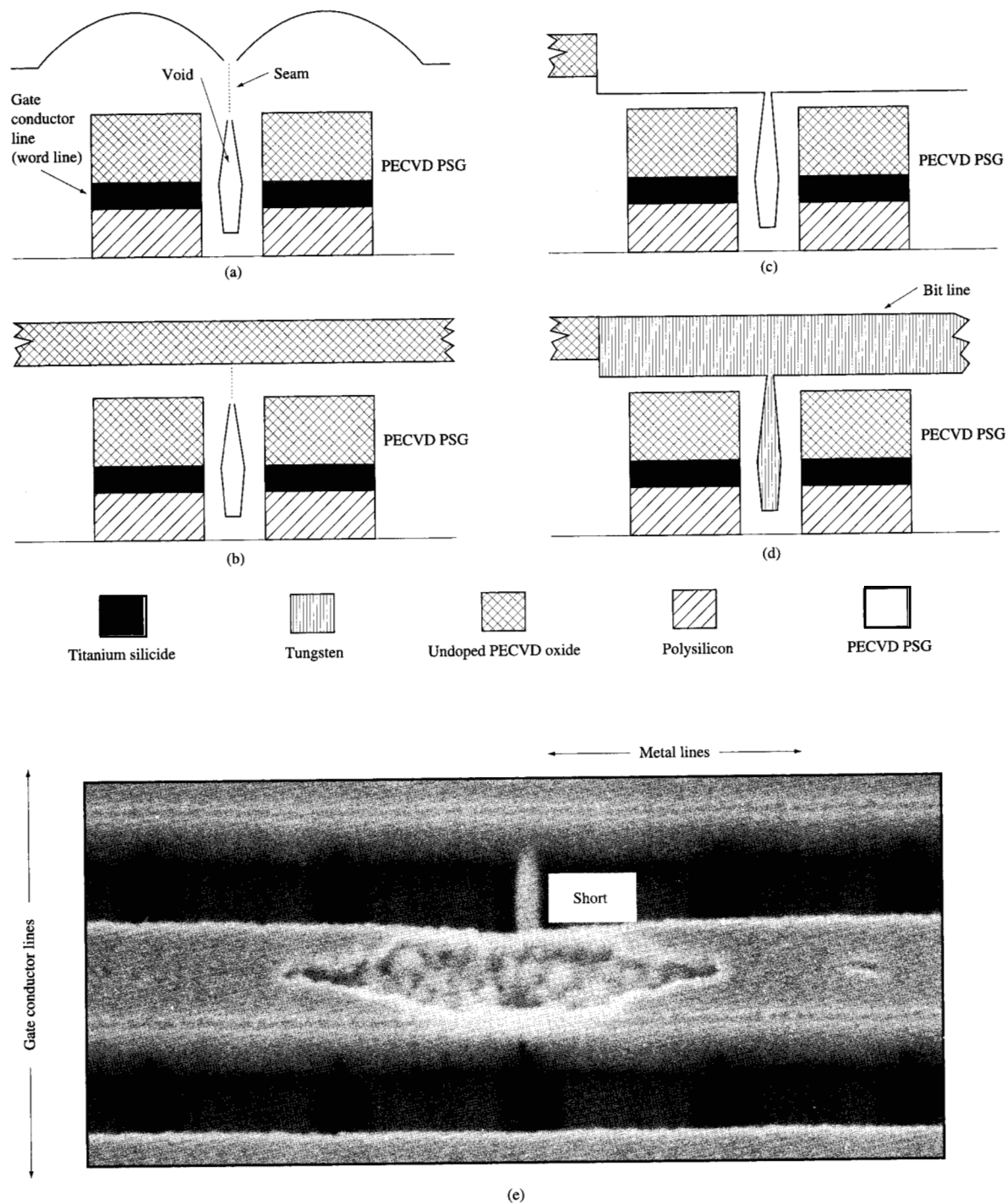


Figure 9

Schematic of how a PSG void between gate conductor lines causes a short to form: (a) after five-step PECVD PSG dep-etch process; (b) after PSG planarization and intermetal dielectric deposition; (c) after patterning (via lithography and RIE); (d) after tungsten CVD and CMP, filling the void as well. The SEM in (e) shows an actual metal short formed in the PSG void. The oxide that normally surrounds and isolates the metal lines has been removed to reveal the short.

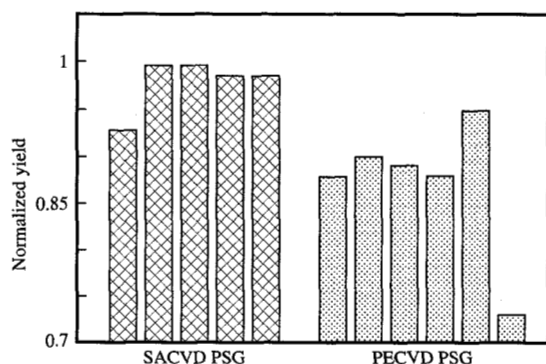


Figure 10

Intralevel shorts yield as measured on a comb/serpentine test structure for an SACVD PSG dielectric vs. a five-step PECVD PSG dep-etch dielectric. Each bar represents one wafer; all wafers were from the same lot.

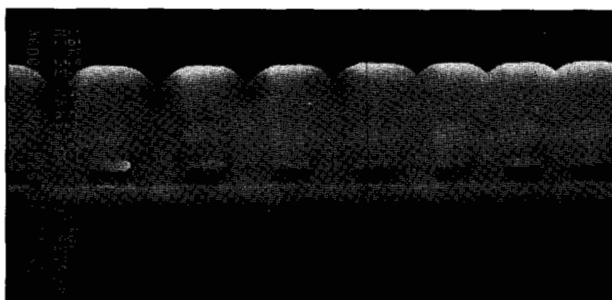


Figure 11

SEM cross section of layer formed by a three-step SAPSG/argon sputter/PECVD PSG fill sequence. Small buried voids have formed in the PSG. The heights of the voids in the very small spaces depend on the sidewall angle of the gate conductor line. The more vertical the line, the taller the void.

the opened void and causes an intralevel short. Figure 9 includes an SEM micrograph of an actual intralevel short formed in a PSG void.

- *A phosphorus-doped TEOS-ozone process for interlevel dielectric fill*

TEOS-ozone CVD processes produce better gap fill than PECVD processes [1]. Also, higher deposition pressures improve gap fill for TEOS-ozone processes [28, 29]. As expected, a thermal TEOS-ozone process for producing PSG results in better gap fill than does a PECVD process. A phosphorus-doped TEOS-ozone film deposited at 600

torr—SACVD PSG—was developed [63] for the 64Mb DRAM interlevel dielectric. The process became one involving a multistep PSG sequence consisting of a thin SACVD PSG deposition to fill the minimum spaces, followed by an argon sputter-etching step to facet the film in the larger spaces. The SACVD PSG was then capped with a thick deposition of PECVD PSG and planarized by CMP. The above sequence was chosen to minimize the use of SACVD PSG, since moisture absorption is a known concern for TEOS-ozone films unless the films are densified or capped with a PECVD film [64]. The intralevel shorts yield for the SACVD PSG fill is significantly higher than for the five-step PECVD PSG process, as indicated in **Figure 10**. Physical failure analysis of the electrical fails confirmed that the shorts for the five-step PECVD PSG process were due to voids in the PSG.

SACVD PSG fills the high-aspect-ratio structures for the 64Mb DRAM sufficiently, but not without the formation of small buried voids between the minimum-space gate conductor lines, as shown in **Figure 11**. The voids form when sidewall angles are greater than 82–84°. It is important to note that these small voids are not a problem if they are buried deeply enough (at least 2000 Å below the top of the gate conductor), because of the fabrication technique for the contacts to gates and diffusions for the 64Mb DRAM product chips. The contacts are borderless with respect to the gates and diffusions, a key design feature that permits formation of a dense array of storage cells [65, 66] (about 40% DRAM cell area is saved). The contacts (tungsten studs) are fabricated using a sacrificial polysilicon mandrel process [67]. Contact holes are etched in the polysilicon mandrel, the holes are filled (deposition + CMP) with tungsten, and the polysilicon is stripped, leaving the studs. Finally, the PSG is deposited. One benefit of the mandrel process is that perfect PSG gap fill is not required, since the studs are formed prior to the PSG deposition. A more detailed discussion of the SACVD PSG process and film properties is included later in this paper.

Intermetal dielectric for tungsten damascene technology

Up to this point, we have concentrated on processes that fill the spaces between metal lines which are patterned using RIE. At some stage in 4Mb manufacturing, the damascene technique was used instead because of the substantial yield improvements that could thereby be achieved [38]. The damascene technique eliminates the need for a cluster tool arrangement for insulator deposition, since the insulator is no longer required to fill gaps between conductor lines. Instead, oxide is deposited on a planar surface, and the metal conductor is formed in this oxide, as was shown in Figure 2. An SEM cross section of tungsten lines from a 64Mb DRAM product chip produced using the damascene technique is shown in **Figure 12**. The oxide is typically deposited by the plasma-

enhanced reaction of silane and nitrous oxide in a multistation, continuous deposition tool described elsewhere [68, 69]. The PECVD oxide displays good film properties such as compressive stress ($\approx -1.0 \times 10^9$ dynes/cm²), minimal water absorption, and compatibility with subsequent etching, photolithography (good resist adhesion), and metal processing (good metal adhesion). Normally, the PECVD silane oxide displays low particulate levels and excellent uniformity ($\leq 3\text{--}5\%$ 3σ) for thin as well as thick films. Damascene technology makes intermetal dielectric processing simpler and more easily extendible. The same process is used for 64Mb and 256Mb DRAM product chips with virtually no changes, even though there is a reduction in metal pitch of more than 50%.

- *256Mb DRAM product and beyond*

Figure 13 summarizes the use of dielectric CVD processes for integrated circuit manufacturing at IBM, including projections into the future. The future interlevel dielectric for the gate conductor in sub-quarter-micron (256Mb DRAM) manufacturing might be the combination of low-temperature reflow BPSG for gap fill followed by CMP of the BPSG for global planarization. High-aspect-ratio void-free fill of sub-quarter-micron spaces has been reported in connection with the use of an LPCVD BPSG process at lower temperatures (700–750°C) [70].

High-density plasma CVD oxide combined with CMP or a low-dielectric-constant fluorinated PECVD oxide film combined with CMP are currently being explored as intermetal dielectrics for the 256Mb DRAM generation. Future prospects and requirements for low-temperature CVD processes for 0.25- μ m CMOS manufacturing are discussed later.

Advances in dielectric processes in 0.35- μ m CMOS manufacturing and development

In this section we examine some recent advances in CVD TEOS processes that have been implemented in IBM manufacturing and development lines. These include improvements in undoped and phosphorus-doped PECVD TEOS oxide processes and TEOS–ozone processes. We also discuss gate oxide degradation due to process-induced charge damage, which is a critical reliability issue for DRAM devices.

- *Gap fill and mixed-frequency PECVD TEOS oxide*

One way to improve gap fill is to add more deposition and sputter-etching steps, but this adds process time and complexity. A better way is to improve film conformality. For a PECVD process, this can be done by decreasing the pressure, thereby increasing the anisotropic component of the deposition. A side effect of lowering the process pressure is a higher occurrence of arcing in the deposition chamber. The power must be decreased to maintain a

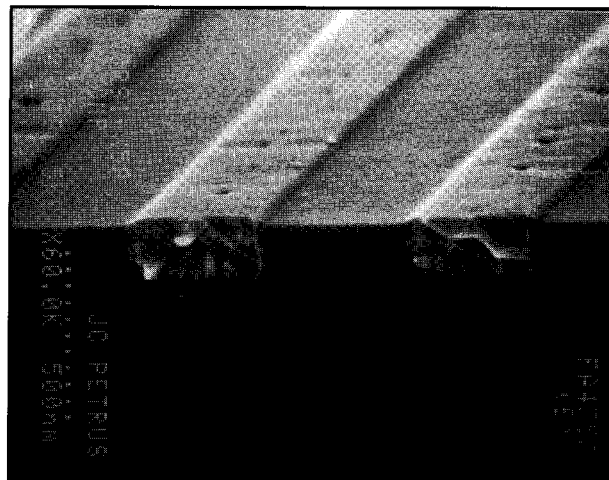


Figure 12

SEM cross section of tungsten/oxide structure from test site of 64Mb DRAM product chip. The structure was produced using damascene technique. The oxide was deposited by the plasma-enhanced reaction of silane and nitrous oxide at 400°C.

stable discharge at the lower pressure, but unfortunately film properties degrade at lower power; e.g., film stress becomes tensile. Therefore, simply reducing the power is not acceptable unless a low-frequency component (356 KHz) is introduced [71]. Ions easily follow the low-frequency component of the plasma, and there is an increase in ion bombardment. The result is a compressive and dense film due to the mixed frequency and improved conformality due to the use of the lower pressure.

Figure 14(a) shows the step coverage achieved if use is made of a mixed-frequency PECVD TEOS oxide deposited at 6.5 torr. **Figures 14(b) and 14(c)** illustrate that the conformality improves as the pressure decreases for this PECVD TEOS oxide process. Another benefit of the use of mixed-frequency PECVD TEOS is a reduction in sputter-etching time, since the deposition is more anisotropic and thus less oxide has to be faceted at the corners of the metal lines. The low-frequency component can be used to modify the stress of the film without greatly changing other film properties such as uniformity. As can be seen in **Figure 15**, the conformality of the mixed-frequency TEOS oxide film results in superior gap fill for a three-step dep-etch process compared to a single-frequency PECVD TEOS three-step process. Phosphorus dopant degrades the conformality of the mixed-frequency film, as indicated in **Figure 14(d)**. This is most likely due to the increase in the sticking coefficient of the PSG [71]. Therefore, the use of mixed-frequency PSG is still not suitable for gap fill. A comparison of process conditions

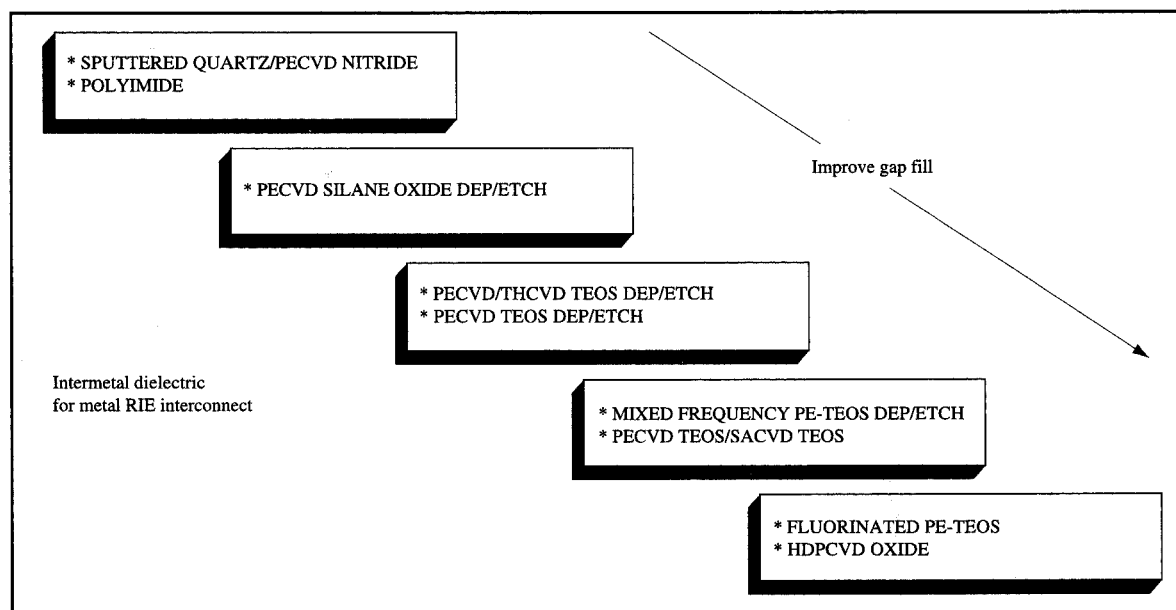
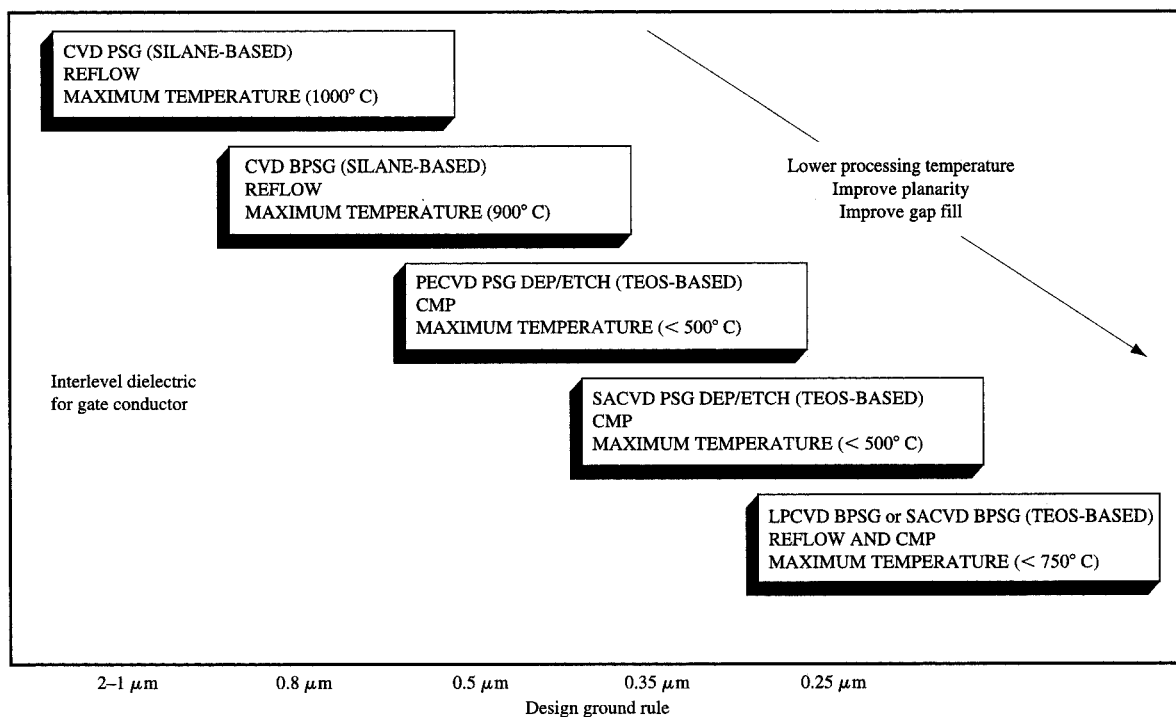


Figure 13

Summary of CVD processes used in manufacturing at IBM relative to design ground rules. Gap filling has been the main driving force for CVD technology advances for both interlevel and intermetal dielectric processes.

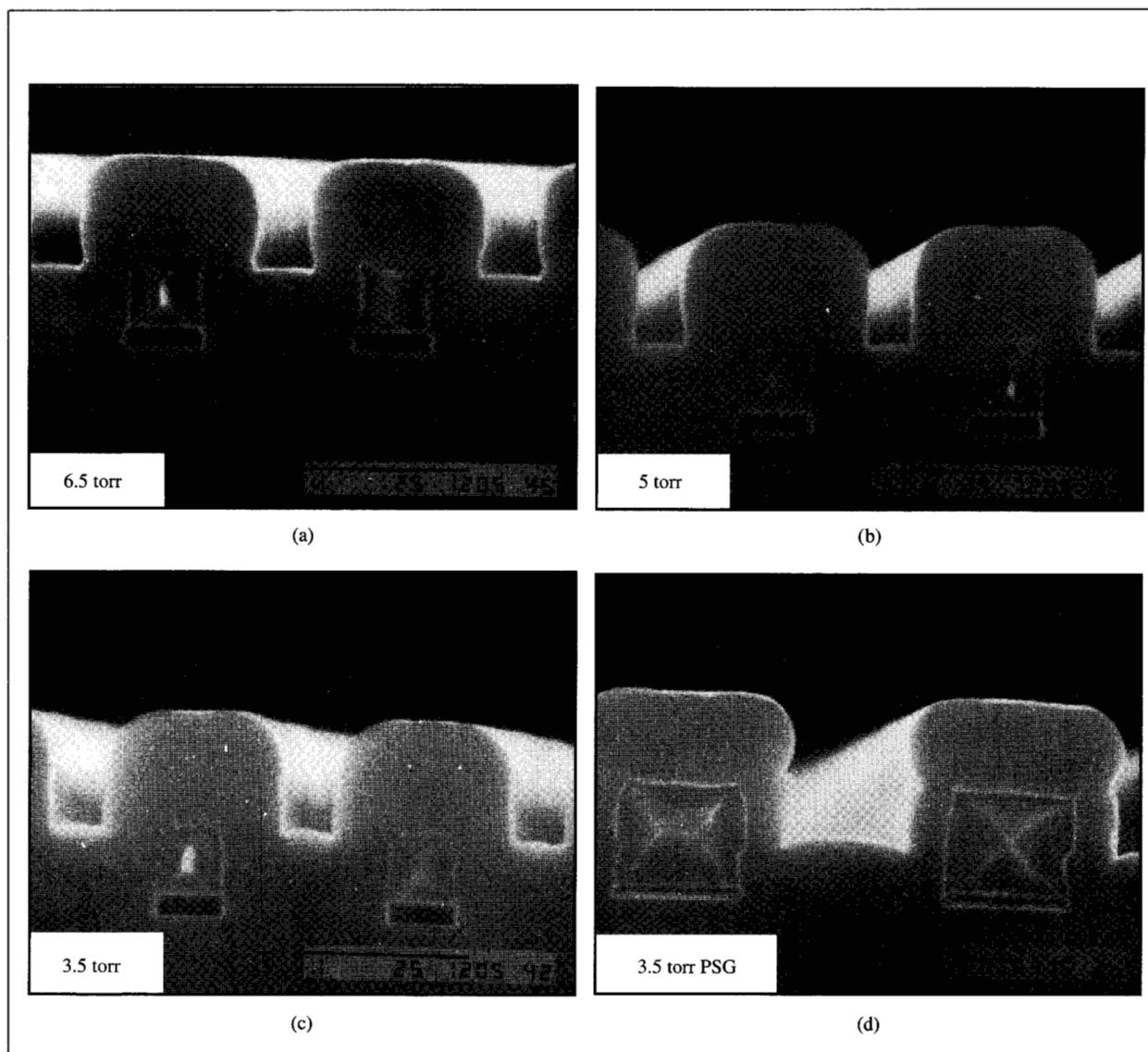


Figure 14

SEM cross sections of a mixed-frequency PECVD TEOS oxide deposited at (a) 6.5 torr, (b) 5 torr, and (c) 3.5 torr. The use of a lower process pressure improves the conformality of the PECVD TEOS process and reduces the cusping at the corners because of the increased anisotropy of the deposition. Adding phosphorus dopant degrades film conformality, as seen in (d), which is a cross section of a mixed-frequency PECVD PSG deposited at 3.5 torr. Note the large increase in cusping at the corners in the latter case. From [71], reproduced with permission.

and conformality for single- and mixed-frequency TEOS oxide films is given in **Table 1**.

- *Plasma deposition and process-induced charging*²

A primary yield detractor and reliability problem for CMOS devices is gate oxide degradation due to process-

induced charging. Process-induced damage from the plasma deposition of trimethylphosphite PSG and the effects on gate oxide reliability [45, 51] and chip yields [44] have been reported for 16Mb DRAM chips. We discuss charge-induced damage from the plasma deposition of triethylphosphate PSG that caused catastrophic low-voltage breakdown of the 100-Å gate oxide for 64Mb DRAM chips [72]. The deposition process pressure was

² The material in this section has recently been presented at a conference and is to be published [72].

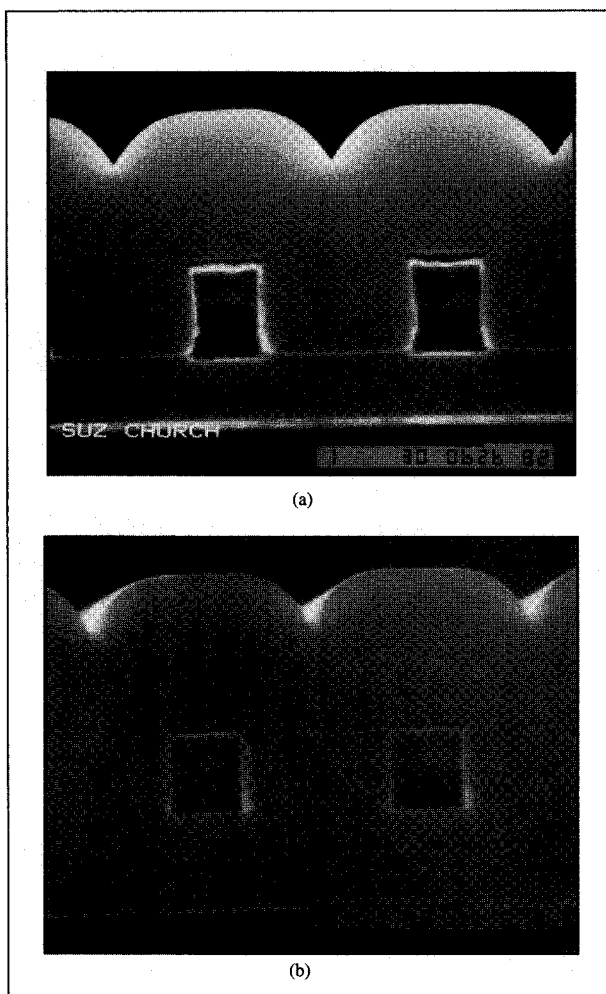


Figure 15

Comparison of a three-step dep-etch of (a) a mixed-frequency PECVD TEOS oxide film and (b) a single-frequency PECVD TEOS oxide film. From [71], reproduced with permission.

Table 1 Conformality of PECVD TEOS films deposited at various process conditions.

Conformality	Standard single frequency 8.5 torr	Mixed frequency			
		3.5 torr	5 torr	6.5 torr	PSG (3.5 torr)
Side/top ($\times 100$)	48	57	48	44	41
Bottom/top ($\times 100$)	75	76	82	79	69

identified as the main factor in causing this charge-induced damage. When undoped PECVD TEOS oxide processes were used at similar pressures, no charge damage was detected. Apparently, the presence of the phosphorus

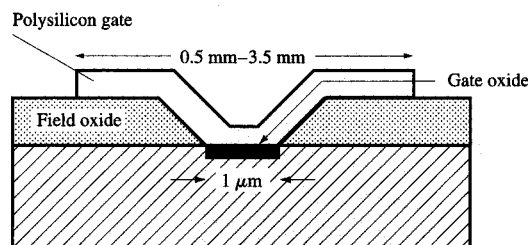


Figure 16

Cross-sectional schematic of the "antenna" structures over thick oxide that were used to detect charge damage to gate oxide. Typical antenna ratios were 2.0×10^5 , 1.0×10^6 , and 1.0×10^7 , with the area of the gate oxide $\approx 1 \mu\text{m}^2$.

dopant causes plasma instability under the same process conditions, thus shifting the low-pressure plasma to a damaging regime.

Simple "antenna" structures were used to isolate the source of the charging damage, as shown in **Figure 16**. The charge-induced damage on product correlated to the antenna monitor damage. Gate oxide defect densities of greater than 1000 electrical defects/cm² were measured on product chip test sites when the triethylphosphate PECVD PSG process was carried out at 8.5 torr; associated antenna monitor yields were zero. Increasing the pressure of the PECVD PSG process to 12 torr decreased the product electrical defect density and improved the antenna monitor yield. However, the process window was narrow at 12 torr, since charge damage resulted from small variations (<100 W) in power. Experiments varying pressure, power, and He-TEOS/O₂ flow ratio were run to develop a larger parameter space for the process. Statistical analysis indicated that the pressure was the main PSG process parameter causing the charge damage, with power being a secondary factor at low pressures; see **Figures 17(a) and 17(b)** [72]. The He-TEOS/O₂ flow ratio was not a significant factor at the process parameter levels used in this experiment. At 16 torr, the PECVD PSG process consistently was found to produce nearly 100% yield on charge monitors, without sensitivity to power fluctuations. Most likely, for this given set of conditions, running the TEPO PECVD PSG process at high pressure eliminated plasma nonuniformity that caused a large enough charging current to break the thin gate oxide. These results are consistent with the mechanism of gate oxide damage from "local ion/electron current imbalance" in nonuniform plasmas described by Fang and McVittie [73]. More detailed analyses of the interaction between pressure and damage for PSG deposition have been

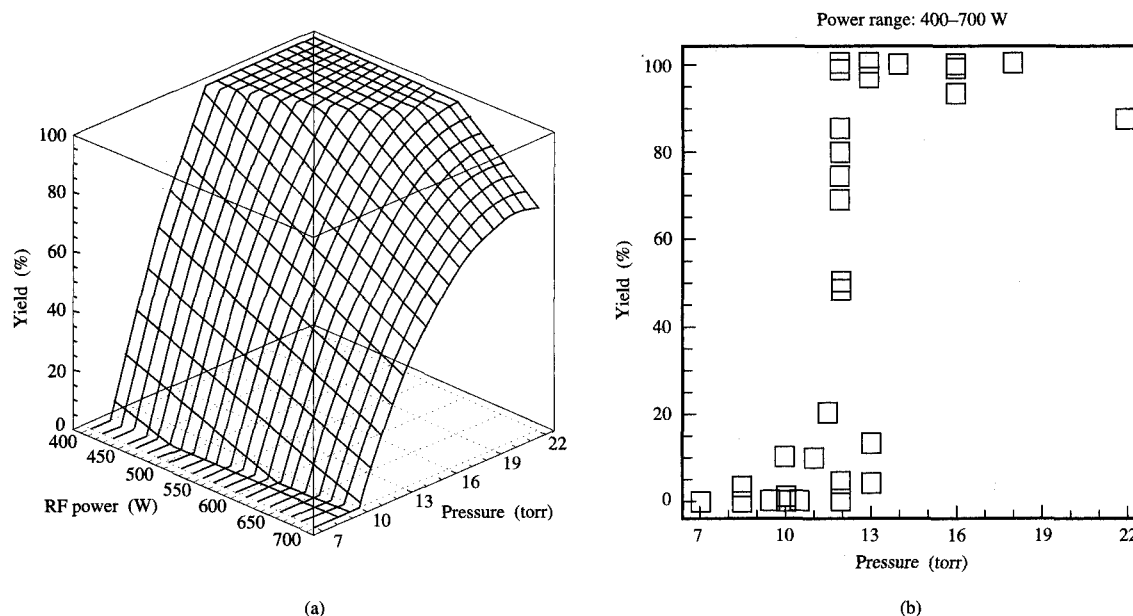


Figure 17

(a) Calculated response surface for a matrix of experiments designed to investigate charging during the triethylphosphate PECVD PSG process [71, 124]. The antenna monitor yield was based on the number of test sites that gave less than 1 nA leakage current at 3.6 V. Pressure was found to be the main process parameter causing the charging. (b) Actual data used to define the response surface; the data showed good correlation with the model.

discussed for the triethylphosphate TEOS-based PECVD process [72] and the trimethylphosphite TEOS-based PECVD process [51].

Additional improvement in gate oxide defect density was gained by eliminating the magnetic field that was present during the argon sputter-etching of the SACVD PSG; however, its elimination resulted in a lower sputter-etching rate. The effect of magnetic field on charge damage has been reported elsewhere [48, 50, 51, 74]. The combined process improvements (16 torr PECVD PSG and elimination of the magnetic field) resulted in a dramatic improvement in product yield. **Figure 18** [72] shows how the gate oxide electrical defect density improved with each PSG process change. Excellent agreement was established between antenna monitors and product chips. The film properties of the PSG deposited at 16 torr are satisfactory compared to those at 8.5 torr. However, at higher pressures the PSG is less compressive because of the decrease in ion bombardment on the wafer surface. Also, at higher pressures the deposition is less directional in nature, and about 7% of sidewall-top conformality is lost. Typical process conditions and film properties for the

8.5-torr and 16-torr triethylphosphate PECVD PSG are given in **Table 2**.

Furthermore, these findings for triethylphosphate PECVD PSG are applicable to the trimethylphosphite PECVD PSG process for the 16Mb DRAM product [51], for which the process was subsequently optimized at 12–14 torr (using antenna monitors), resulting in yield enhancement. This simple methodology provides a cost-effective and manageable means of process optimization, tool monitoring, and control which is essential for the continued development and maintenance of robust, damage-free plasma processes.

• APCVD and SACVD TEOS-ozone processes

The most important advance in TEOS-ozone processes has been the move to higher deposition pressures (200–600 torr) and higher ozone concentrations. Silicon oxide films deposited by TEOS-ozone reactions at high pressures display not only excellent conformality and good gap-fill properties, but also good reflow properties at high ozone concentrations (>6 wt. % ozone) [75]. The superior gap fill for TEOS-ozone oxide films deposited at high pressure is

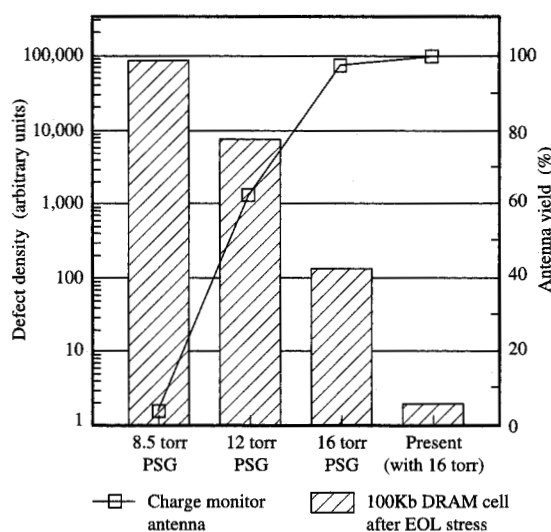


Figure 18

Defect density and yield of 1×10^6 antenna ratio capacitor (as described in Figure 16) is compared with the defect density of a test structure consisting of 100Kb DRAM cells after end-of-life gate oxide stress. The "present" 16-torr defect density includes improvements from other processes.

Table 2 Comparison of typical plasma deposition conditions and film properties of triethylphosphate (TEPO) PSG deposited at 8.5 torr and 16 torr.

Process parameters and film properties	(4 wt. % P) PECVD PSG process	
	8.5 torr	16 torr
Helium/ TEPO flow rate	500 sccm	650 sccm
Ampule temperature	46°C	46°C
Helium/ TEOS flow rate	700 sccm	850 sccm
Ampule temperature	48°C	48°C
Oxygen flow rate	1000 sccm	850 sccm
Electrode spacing	220 mils = 0.53 cm	220 mils = 0.53 cm
RF power	650 W	550 W
Susceptor temperature	440°C	480°C
Deposition rate	480 nm/min	410 nm/min
Uniformity	3-5% (3σ)	3-5% (3σ)
Refractive index	1.462	1.458
Compressive stress (1- μ m films)	-1.2×10^9 dynes/cm ²	-0.4×10^9 dynes/cm ²
Conformality (side/top $\times 100$)	65%	58%
Etch rate (7:1 BHF) X = thermal oxide	3.6 X	4 X

demonstrated using an extremely high-aspect-ratio (10:1) trench structure, as indicated in **Figure 19**. In addition, the use of TEOS-ozone films with excess ozone flow (i.e., high ozone:TEOS ratio) eliminates any potential particle formation due to gas-phase nucleation at high pressures. These high-pressure TEOS-ozone processes are referred to as APCVD TEOS-ozone and SACVD TEOS-ozone processes. A detailed history of the development of the processes has appeared in a recent publication [28].

The foremost problem for TEOS-ozone processes at high pressure and high ozone concentration is the questionable film quality due to the substrate surface sensitivity of the process. When the process is sensitive to the substrate to which it is exposed, the film deposition rate typically decreases, and the film becomes less dense and porous. SACVD oxide films have been known to exhibit substrate surface sensitivity depending on the ozone:TEOS ratio [76]. For undoped SACVD oxide, the higher the ozone:TEOS ratio, the more substrate surface sensitivity is exhibited. The surface sensitivity of the deposition process also depends on the underlying base materials [77]; this has severely limited the window of the process and has required careful consideration of surface pretreatments and process conditions before deposition. If use is made of SACVD oxide films, an underlying PECVD oxide seed layer and overlying PECVD oxide are normally required.

Since substrate surface sensitivity was the main issue with the undoped SACVD TEOS-ozone process, it was one of the first aspects examined in connection with the phosphorus-doped version of the process. One way of quantifying the substrate surface sensitivity of a process is to compare the wet-etching rate of a film deposited on silicon by means of the process to that of the same type of film deposited on the substrate of interest. Typically, if the film exhibits substrate surface sensitivity, it will be of poorer quality and will etch more rapidly than the film deposited on the silicon substrate. **Figure 20** shows that triethylphosphate (phosphorus-doped) TEOS-ozone process or SACVD PSG exhibits no substrate surface sensitivity when deposited on PECVD TEOS and PECVD silane oxide substrates. These results agree with published data for trimethylphosphate (phosphorus-doped) APCVD TEOS-ozone oxide [78], for which there was also no substrate surface sensitivity. For comparison, a high-ozone:TEOS-ratio undoped SACVD oxide deposited on the same oxide surfaces results in very poor film quality, as shown in the figure. Note that in this work the wet-etching rate is normalized with respect to the wet-etching rate of thermally grown oxide.

Next, since undoped TEOS-ozone films absorbed water readily [1], we expected SACVD PSG to absorb water. If the SACVD PSG film is capped with a thin PECVD film, annealed at a temperature above 550°C or argon sputter-

etched, water absorption is prevented. Since hot-electron degradation of devices is indicative of high moisture and/or high hydrogen content in films [16], channel hot-carrier stress was evaluated for p-type and n-type MOSFET devices using PECVD PSG and SACVD PSG processes for the polysilicon-metal interlevel dielectric [63]. No degradation was observed with either process.

SACVD PSG filling is conformal compared to the reflow-like filling achieved using the undoped SACVD TEOS process, as indicated in **Figure 21**. This indicates again that the introduction of phosphorus degrades conformality. The dependence of gap fill on ozone concentration was studied [63] for the SACVD PSG process. All parameters were fixed except for TEPO flow (which was changed to maintain a 4 wt. % level of phosphorus), ozone flow, and ozone concentration. As the ozone concentration increased, the fill degraded. This trend was different from what is typically seen for undoped SACVD oxide films [79]. Further ozone concentration studies for doped SACVD processes are in progress to improve our understanding of the effects on gap fill and film properties. Typical SACVD PSG deposition conditions and film properties are given in **Table 3**.

Advanced CVD processes for the 0.25- μm CMOS generation

Sub-half-micron structures with high aspect ratios cannot be filled using conventional PECVD dep-etch processes. These structures require new CVD processes to meet the gap-fill requirement economically. Multistep integrated processes are costly primarily because of long cycle times. In this section, we review new processes and dielectrics that are currently used in sub-half-micron development lines or have potential for future manufacturing applications as either interlevel or intermetal dielectrics.

• Low-temperature BPSG reflow

For ULSI technology, the critical requirement for BPSG remains the same as for previous generations: Fill high-aspect-ratio structures with a good-quality dielectric at the lowest possible temperature. The fact that BPSG can reflow can be advantageous if it is integrated within the deposition process itself, as illustrated by LPCVD BPSG. Like its phosphorus-doped counterpart, TEOS-ozone BPSG has excellent step coverage [i.e., 100% conformality at a low deposition temperature ($<500^\circ\text{C}$)], making it highly suitable as an interlevel dielectric for sub-half-micron devices.

TEOS-ozone BPSG

BPSG has been deposited using triethylborate, trimethylphosphate, TEOS, and ozone at atmospheric pressure [80] and using triethylborate, triethylphosphate, TEOS, and ozone at 400–600 torr [79]. However,

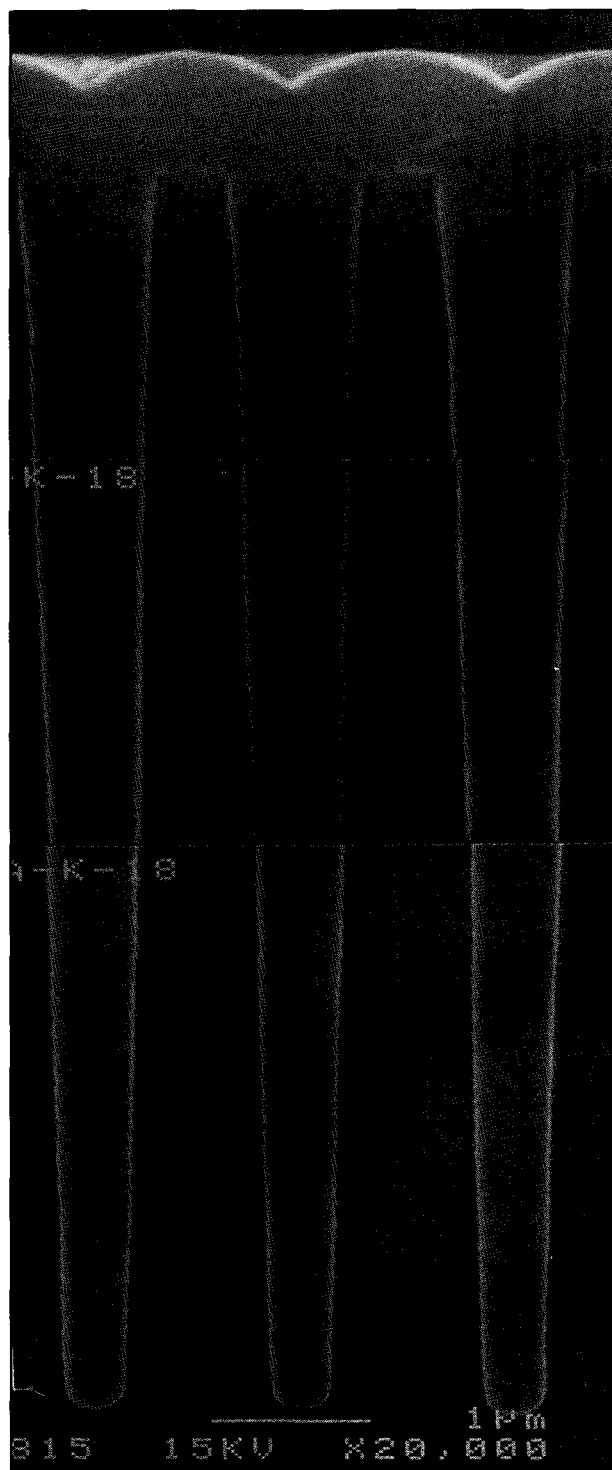


Figure 19

SEM cross section illustrating void-free gap fill with SACVD TEOS-ozone process. Gap width is 0.7 μm , with an aspect ratio of about 10:1. The use of such an extremely high-aspect-ratio structure illustrates the excellent gap-filling capability of high-pressure TEOS-ozone processes.

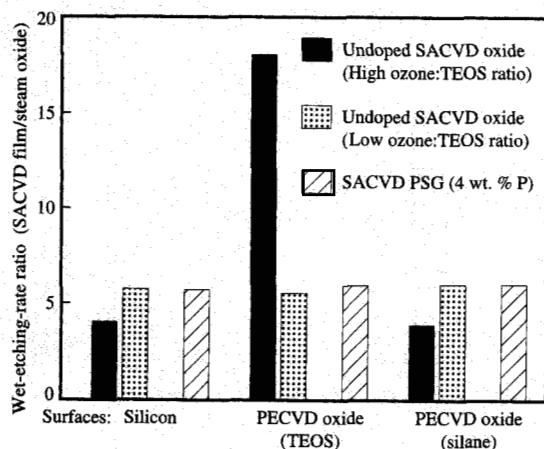


Figure 20

Comparison of wet-etching rate in 6:1-buffered HF for undoped SACVD oxide films and SACVD PSG on three different surfaces and normalized with respect to the wet-etching rate of thermally grown oxide in 6:1 buffered HF [62]. There is no surface sensitivity for SACVD PSG deposited on PECVD TEOS and PECVD silane oxide, since the wet-etching-rate ratio (WERR) is equivalent to SACVD PSG deposited on silicon. The high ozone:TEOS ratio SACVD-undoped-oxide process shows surface sensitivity on PECVD TEOS, since the WERR is high, indicating that the deposited film is less dense and thus of poorer quality.

TEOS-ozone BPSG still requires high-temperature (>750°C) reflow for void-free fill of sub-half-micron spaces. One way to lower the reflow temperature is to increase the boron and phosphorus concentration. BPSG films tend to absorb water upon long exposure in air and may form boric acid surface defects [81]. An increase in boron or phosphorus would elevate the water absorption rate of the as-deposited films and the defect formation, causing subsequent process problems in RIE and CMP. Generally, the boron and phosphorus dopant concentrations in BPSG films are limited to 5 wt. % or less in order to minimize the defect formation.

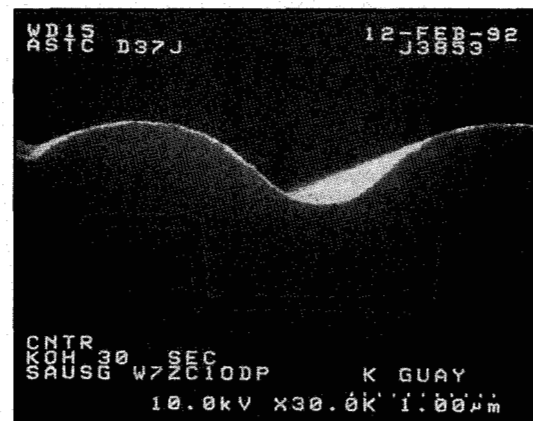
LPCVD BPSG

Simultaneous deposition and fusion-flow planarization of BPSG films has recently been shown to be possible via a single-step LPCVD process at 800–900°C [82]. This temperature range is still too high for titanium silicide films because of their high-resistivity phase formation and agglomeration [11]. Recently, BPSG was anisotropically deposited by the reaction of TEOS, triethylborate, phosphine, and oxygen at a lower temperature (700–750°C) [83]. The film properties were comparable to those of high-temperature BPSG films. The process can fill very high-

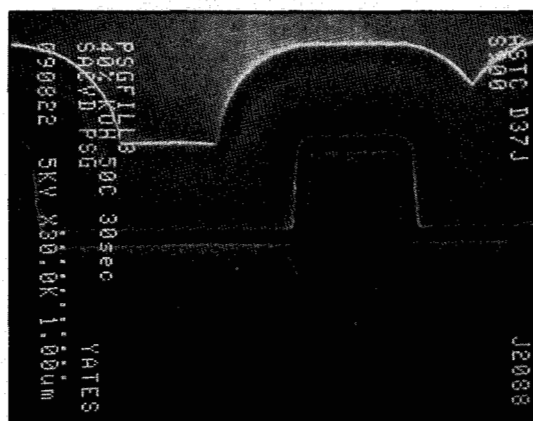
aspect-ratio gate conductor gaps [70] without the need for a subsequent high-temperature reflow process, as shown in **Figure 22**. The gap-fill properties of this type of LPCVD BPSG are strongly affected by boron and phosphorus dopant concentrations, process conditions, and temperature [84]. Although the film reflows slightly at this lower temperature range, this type of LPCVD BPSG film and subsequent CMP processing can be used for metal silicide gate conductor dielectric deposition and planarization, as shown in **Figure 23**.

Germanium-doped BPSG

Germanium-doped PSG has been studied [85] as a low-temperature reflow glass for semiconductor fabrication,



(a)



(b)

Figure 21

SEM cross sections of (a) SACVD undoped oxide and (b) SACVD PSG oxide. Note that the SACVD undoped oxide is reflow-like and the SACVD PSG oxide is conformal.

but the temperatures required for reflow were too high (850–900°C). More recent results have shown that an increase in germanium can lower the BPSG reflow temperature to 750°C in a wet ambient and produce a good reflow profile for local planarization. Using TEOS, ozone, trimethoxygermane, trimethylphosphate, and triethylborate as reactants, up to 20 mole % of germanium can be incorporated into BPSG without significant degradation of film physical properties such as stress, water absorption, and wet-etch rate [86]. BPSG reflow properties are also significantly improved with germanium incorporation, and the process can be implemented with only small modifications to existing CVD equipment. However, more work is still needed in order to understand other aspects of germanium-doped BPSG before its suitability can be assessed (e.g., its electrical breakdown, its compatibility with RIE and CMP, and its effects on microelectronic devices and structures). Furthermore, germanium-doped BPSG films may not be needed immediately, since recent results on single-step LPCVD BPSG [70, 83, 84] have shown the possibility of a significant reduction in processing temperature.

- *New films for sub-quarter-micron intermetal dielectric* Multichamber, multistep dep-etch processes have severe limitations for sub-quarter-micron gap fill. First, increasing the number of deposition and etch steps to fill high-aspect-ratio structures would increase the process time and

Table 3 Typical deposition conditions and film properties of (4 wt. % P) SACVD PSG.

Helium/TEOS flow rate	4800 sccm
Ampule temperature	48°C
Helium/triethylphosphate flow rate	2200 sccm
Ampule temperature	46°C
Ozone flow rate	3000 sccm
Ozone concentration	8.5%
Electrode spacing	220 mils = 0.53 cm
Process pressure	600 torr
Susceptor temperature	480°C
Deposition rate	120 nm/min
Uniformity	<3–5% (3σ)
Refractive index	1.44–1.45
Dielectric constant	3.7–4.2
Tensile stress (1- μ m films)	2.2×10^9 dynes/cm ²
Etch rate (RIE)	1 X PECVD PSG
Etch rate (6:1 BHF)	5.5 X thermal oxide
Oxide polishing rate	1.4 X PECVD PSG
Carbon	$\sim 4 \times 10^{18}$ atoms/cm ³

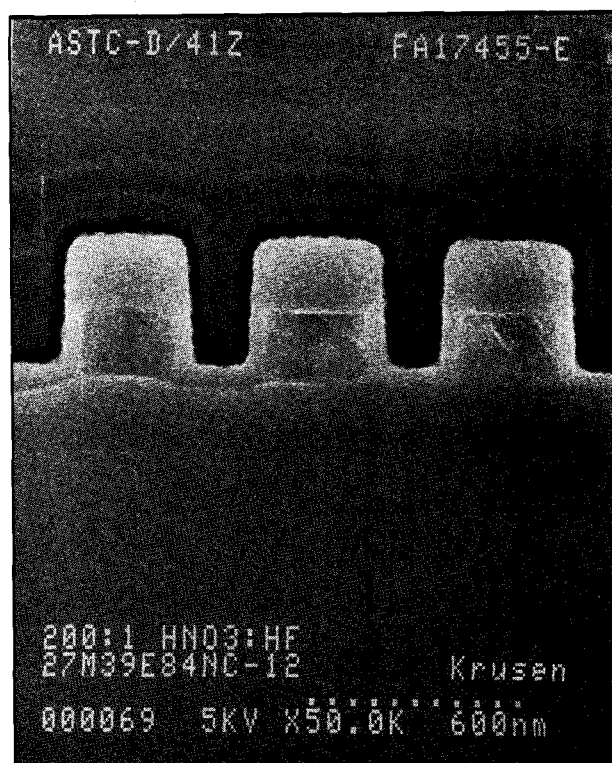


Figure 22

SEM cross section of LPCVD BPSG film deposited by the reaction of TEOS, triethylborate, phosphine, and oxygen at 750°C. The highest aspect ratio for the indicated structure is greater than 3:1.

complexity; it would be extremely inefficient and would most likely result in imperfect gap fill. Although chamber dedication initially provides significant improvement in the efficiency of the cleaning steps for deposition and etch processes, the elimination of wafer movement between chambers should eliminate particles falling on the wafer as a result of these movements. Particles that fall on the wafer after a deposition step can block the following argon sputter-etching step, thus causing void formation and ultimately an intralevel short.

Two potential films for use as sub-quarter-micron technology intermetal dielectric are high-density plasma CVD oxide and plasma-enhanced fluorinated TEOS oxide. The use of fluorine enhances gap fill. Additionally, the use of fluorine in connection with the PECVD TEOS oxide process results in lowering of the dielectric constant [87], leading to improved circuit performance. In effect, the high-density plasma CVD is a simultaneous dep-etch process that fills high-aspect-ratio structures in one step.

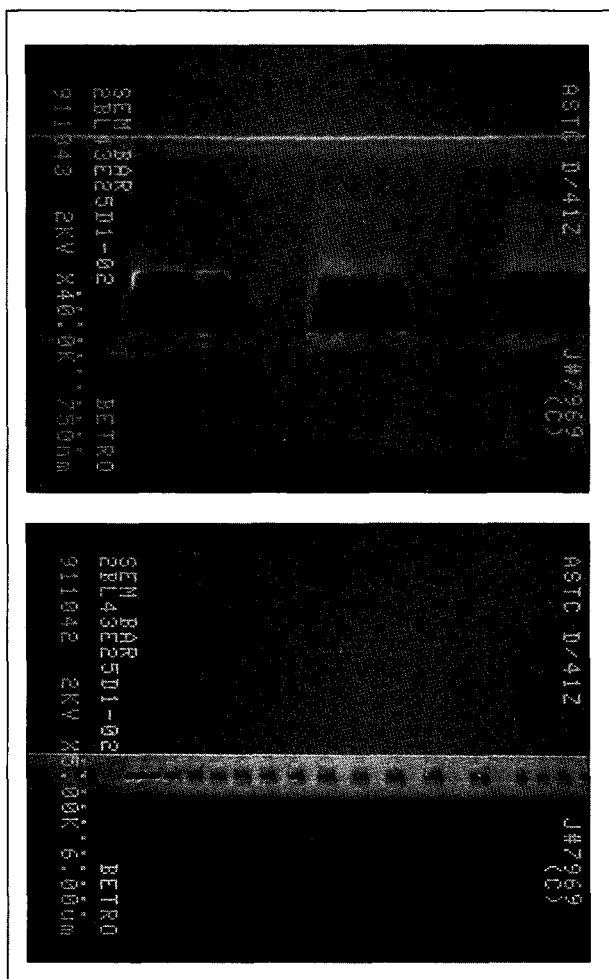


Figure 23

SEM cross sections at two levels of magnification of the same type of LPCVD BPSG film shown in Figure 22 after CMP.

High-density plasma chemical vapor deposition

Many recent publications [88] discuss high-density plasma sources and their application in dry-etching and CVD processing. Among many techniques being developed, electron cyclotron resonance (ECR) [89–91] and other high-density plasma chemical vapor deposition (HDP CVD) processes [92] have shown very encouraging results for high-aspect-ratio gap fill and high-quality silicon oxide film formation.

In HDP CVD processing, loosely deposited films or “deposited species” over planar or topographical surfaces are sputter-etched by reactive ions and radicals simultaneously with deposition. The net deposition rate is the deposition minus a sputter-etching rate. In ECR CVD processing in which silane, oxygen, and argon are the

reactant gases, Ar^+ , O_2^+ ions and H , SiH radicals are the principal reactive etching species [89, 93]. In general, the sputtering at the corner of a feature is much higher than on the horizontal and vertical surfaces, which prevents the gap from being “pinched off.” The high degree of near-vertical ion bombardment limits film deposition on the trench sidewalls. Since this simultaneous profile modification occurs during the deposition process, HDP CVD fills gaps from the “bottom up” [93]. Because of the simultaneous dep-etch nature of the HDP CVD process, the angle and energy of the ions striking the surface and of other reactive species in the plasma determine what gap features can be filled without voids. Therefore, the HDP CVD process may be limited to a specific dimension, feature profile, and aspect ratio depending on process parameters [94].

Pattern and feature dependency common to plasma etching occurs in HDP CVD as well because of its etching component. In addition, the intralevel film quality between filled gaps depends on the magnitude of the ion

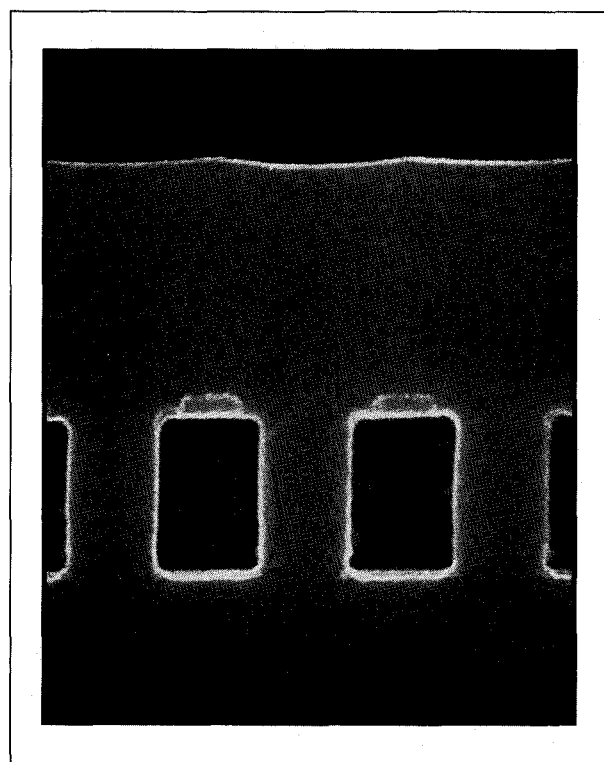


Figure 24

SEM cross section illustrating use of high-density plasma CVD oxide fill for a portion of an aluminum/copper interconnection structure. Line spacing is $0.27 \mu\text{m}$ at an aspect ratio greater than 2.2.

bombardment [94]. The properties of HDP CVD film are quite dependent on process conditions. For example, the silane:oxygen reactant gas ratio is a major factor that determines the physical and dielectric constant properties of ECR CVD [89, 93, 94] and of high-density helicon plasma CVD silicon oxide films [92].

Recent work [95] has shown that the use of ECR CVD oxide for intermetal dielectric deposition does not cause any 0.5- μm n-MOS device degradation. Furthermore, the associated ion bombardment creates a denser and more dangling-bond ECR CVD oxide film with improved water blocking, thus reducing the potential hot-carrier degradation in 0.5- μm MOSFET devices [16, 91]. For sub-half-micron devices with a gate oxide thinner than 100 Å, the effect of HDP CVD on device degradation has not been determined, though it is not a problem at a 100-Å gate oxide thickness, as determined from antenna structures. The impressive gap fill of HDP CVD oxide is demonstrated by the SEM cross section in **Figure 24**, which depicts a portion of a high-aspect-ratio aluminum/copper interconnection structure.

HDP CVD processing can also be used to deposit various dielectric films of boron nitride [96] or fluorinated oxide. For high-performance sub-half-micron CMOS device fabrication, HDP CVD technology will probably meet 0.10- μm device requirements of minimum-feature gap fill, minimal plasma damage, and more controllable film quality.

Fluorinated silicon oxide

Recent publications have shown that fluorinated silicon oxide films can be deposited by either advanced or plasma CVD processing [97–100]. The deposited films have good physical, chemical, thermal-stability, and electrical properties. A fluorinated silicon oxide film formed at room temperature has good step coverage and excellent flow angle over an aluminum wiring structure [97, 98]. Our recent study [101] of PECVD fluorinated silicon oxide films has shown that fluorine incorporation enhanced the gap fill of a 0.25- μm Al/Cu wiring structure. Furthermore, the water absorption and, hence, dielectric constant of the fluorinated silicon oxide films are reduced because the Si–H and/or Si–OH are replaced by Si–F bonds [97, 98]. These films show potential as intermetal dielectrics for sub-half-micron CMOS devices, but the stability and reliability of SiOF in a ULSI interconnection environment have not been investigated and therefore are still open issues.

• *Other low-dielectric films and applications*

For dielectric films, the overall consensus [15] has been that silicon dioxide films will continue to meet design requirements extending to those of the 0.25- μm CMOS

Table 4 Plasma deposition conditions and film properties of fluorinated silicon nitride.

SiH ₄ flow rate	5–90 sccm
SiF ₄ flow rate	10–70 sccm
N ₂ flow rate	5000 sccm
Electrode spacing	500 mils = 1.2 cm
Power density	0.6–2.8 W/cm ²
Process pressure	5 torr = 660 Pa
Susceptor temperature	440°C
Deposition rate	40–300 nm/min
Uniformity	<3–5% (3 σ)
Refractive index	1.63–2.1
Tensile stress (1- μm films)	$1.5\text{--}2 \times 10^9$ dynes/cm

circuit (~256Mb DRAM) generation. Lower-dielectric-constant films with improved CMP and etching characteristics are being studied for use with such circuits and to improve performance. In addition to fluorinated silicon oxide, some inorganic films now being explored for those purposes are boron nitride, silicon boron nitride, and fluorinated silicon nitride. A discussion of organic films such as vapor-deposited parylene-F films [102] is beyond the scope of this paper.

Fluorinated silicon nitride

Plasma-deposited fluorinated silicon nitride films have been studied as potential low-hydrogen, low-temperature passivation films for CMOS devices. Various processes and associated film properties have been analyzed in detail [103–107]. Most of the deposited fluorinated nitride films tend to be unstable either when exposed to air for long periods or after high-temperature annealing in nitrogen or oxygen ambient. However, suitable substitution of stronger Si–F and N–F bonds for weaker Si–H and N–H in the plasma silicon nitride bonding network should result in a more stable silicon nitride with a lower hydrogen content [106, 107]. N-type MOSFETs passivated with fluorinated silicon nitride have a longer life and lower interface-state density because of the reduced hydrogen concentration [108].

Stable and highly conformal fluorinated silicon nitride films can be deposited at low temperatures (300–400°C) in a single-wafer (13.6-MHz), plasma-enhanced chemical vapor deposition system using silane, silicon tetrafluoride, and nitrogen as reactant gases under the conditions listed in **Table 4** [108]. The fluorinated silicon nitride films formed with a silicon tetrafluoride:silane flow ratio greater than 1 display good thickness uniformity and are stable in ambient air and after annealing at 900°C in nitrogen. X-ray

Table 5 Fluorinated silicon nitride film compositions as analyzed by X-ray photoelectron spectroscopy (5 torr, 400°C, 260 W, 20 sccm SiF₄, 5000 sccm N₂, SiH₄ = 5–60 sccm).

Flow rate ratio (SiF ₄ /SiH ₄)	Composition (at. %)				
	Silicon	Nitrogen	Fluorine	Oxygen	Carbon
4	57	25	17	<1	0
2	56	27	16	1	0
1	55	27	15	3	0
2/3	51	22	14	13	0
1/2	50	22	13	15	0
1/3	55	28	10	7	0

Table 6 Conditions for plasma deposition of boron nitride films.

Process parameters	Precursor	
	B ₂ H ₆ /NH ₃	Borazine: B ₃ N ₃ H ₆ /N ₂
B ₂ H ₆ flow rate (1% in N ₂)	1800 sccm	—
Borazine flow rate	—	100 sccm
NH ₃ flow rate	120 sccm	—
N ₂ flow rate	4200 sccm	200 sccm
Electrode spacing	250 mils = 0.6 cm	380 mils = 0.95 cm
RF power	500 W	200 W
Process pressure	5 torr = 660 Pa	3 torr = 400 Pa
Susceptor temperature	400°C	300°C

photoelectron spectroscopic analysis (Table 5) shows that up to 17 at. % of fluorine is incorporated in the film, and the fluorinated silicon nitride does not degrade upon long-term exposure to air, indicating a stable Si–F bonding network. Results from nuclear reaction analysis show that the hydrogen content (4–6 at. %) in these films is significantly lower than that of typical plasma silicon nitride films (15–24 at. %) deposited under similar conditions. This is primarily because of the Si–F substitution for the Si–H bonds in the conventional silicon nitride films. The fluorinated nitride films show excellent conformality over silicon trench surfaces, but poor conformality over Al(Cu) lines. Stable fluorinated nitride films have a dielectric constant of 6–6.5, just slightly lower than that of conventional plasma nitride films. These stable fluorinated silicon nitride films are expected to be preferable for passivation at the ULSI level of integration.

Plasma CVD boron nitride and silicon boron nitride

Such films have been deposited [109–117] and studied as low-dielectric-constant materials for bipolar devices [109–115], and also as hard-coating materials [116]. Various chemical precursors such as

Table 7 Properties of plasma-deposited boron nitride films.

Properties	Precursor	
	B ₂ H ₆ /NH ₃	Borazine: B ₃ N ₃ H ₆ /N ₂
Deposition rate	300 nm/min	370 nm/min
Uniformity	<5–10% (6σ)	3% (3σ)
Refractive index	1.746	1.732
Stress	-4×10^8 Pa = -4×10^9 dynes/cm ²	-1.5×10^8 Pa = -1.5×10^9 dynes/cm ²
Etch rate (RIE)	62 nm/min	28 nm/min
Etch rate (H ₃ PO ₄ —167°C)	1–11 nm/min	—
Etch rate (BHF)	0.5 nm/min	<1 nm/min
B/N ratio	1.02	1.02
Hydrogen content	<8 at. %	<8 at. %
Density	1.89 g/cm ³	1.904 g/cm ³
Optical bandgap	4.7 eV	4.9 eV
Step coverage	60% (1 × 1 μm)	80% (0.5 × 0.5 μm)
Structure	amorphous	amorphous
Dielectric constant	3.8–5.7	3.8–5.7
Breakdown potential	6–7 MV/cm	6–8 MV/cm

borane–amine–hydrocarbon complexes [110], diborane–BCl₃–ammonia [110–115, 117], and borazine [116] have been used for film deposition. Recent publications [115, 118] show that the dielectric constant of boron nitride can vary from 2.7 to 7.7 depending on deposition conditions and measurement methods.

The mechanical resistance of boron nitride films to abrasives makes them useful as chemical–mechanical polishing stops for global planarization [119, 120]. The high plasma reactive ion etching rate of such films compared to silicon oxide and silicon nitride films (>10:1) makes them desirable insulators in the fabrication of borderless contacts and multilevel interconnections [121]. In more recent work [121, 122], stable boron nitride films have been deposited in single-wafer plasma chemical vapor deposition systems. Two different reactant gas systems are used in the deposition: 1) dilute diborane (1% diborane in nitrogen), nitrogen, and ammonia; and 2) borazine (B₃N₃H₆) and nitrogen. Tables 6 and 7 show deposition conditions and associated film properties indicating that stable boron nitride films can be deposited by either system. Additionally, the films do not react in boiling water and display good breakdown characteristics (6–8 MV/cm). Although the films deposited using the two systems showed many differences in bonding and physical

properties, their dielectric constants were similar, all lying between 3.8 and 5.7, depending on deposition conditions.

Although boron nitride films doped (i.e., oxidized, contaminated) with oxygen have a lower dielectric constant, they are generally unstable because of the formation of hygroscopic boron oxide phases in the films. Overall, the dielectric constants of plasma CVD boron nitride films correlate well to composition, bonding structures, degree of crystallinity, and deposition conditions. For boron-rich boron nitride, the dielectric constant values are 3.7 or lower, because the boron-rich layers react in air to form both boron nitride/boron oxide phases (as for oxygen-doped boron nitride or oxygen-doped silicon boron nitride) [121]. It should be noted that MIS measurement versus capacitance data on such films can be misleading if n-type Si substrates are used. This is because the initial diffusion/implantation of excess boron during plasma deposition of a boron nitride film can form a p-n junction at the interfaces, leading to inaccurate capacitance results and, hence, misleading dielectric constant values [123, 124].

Summary

Significant changes in the development of low-temperature CVD dielectrics have occurred over the past twenty years. Narrow spaces between conductor lines, reduced thermal budgets during fabrication, and the need for improved dielectric planarization have provided the impetus for the major advances that have been achieved: the development of dep-etch processes in conjunction with TEOS-based oxide processes for improved gap filling, and the development of oxide CMP processes for planarization. More recently, high-pressure ozone-activated TEOS processes have helped meet high-aspect-ratio filling requirements for more aggressive sub-half-micron devices. Device damage due to process-induced gate oxide degradation has become a major reliability issue for plasma processes as device geometries shrink. With continuing development efforts, process control, and process monitoring, these sources of charge damage are becoming better understood and are being eliminated.

Advanced CVD approaches involving the use of CVD TEOS-ozone, plasma CVD fluorinated oxide and nitride, single-step LPCVD BPSG, plasma CVD boron nitride, and high-density plasma CVD oxide layers show encouraging results for sub-half-micron ULSI development and manufacturing. With better control of ion density and energy and improved high-aspect-ratio sub-half-micron gap filling, high-density plasma CVD shows promise as a low-dielectric-constant deposition approach for sub-quarter-micron circuit fabrication.

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