CMOS scaling in the 0.1-μm, 1.X-volt regime for high-performance applications

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Deep-submicron CMOS is the primary technology for ULSI systems. Currently, the state-of-the-art CMOS device has a 0.25-μm effective channel length and operates at 2.5 V. As the CMOS technology is extended into the deep submicron range, it is estimated that the next generation will have a nominal channel length of 0.15 μm with a supply voltage of $\leq$2 V. In this paper, two potential technologies with application to 1.X-V CMOS are presented. First, a bulk CMOS technology with the nominal channel length of 0.15 μm is described. It is next argued that because of issues related to power dissipation, such a device may face problems when operated at its maximum speed–density potential in high-performance logic chips. CMOS on a silicon-on-insulator (SOI) substrate offers circuits with lower power at the same performance. Such a CMOS technology, with channel lengths down to less than 0.1 μm, is described next. This technology is particularly useful for applications near a 1.0-V supply. We describe, for example, a 512Kb SRAM with an access time of less than 3.5 ns at 1.X V. The clear power–performance advantage of CMOS on SOI over that of CMOS on bulk silicon in the 1.X-V regime makes it the technology of choice for sub-0.25-μm CMOS generations.

1. Introduction

Scaling of CMOS on bulk Si has been the principal focus of the microelectronics industry over the last two decades: As one reduces the channel length, the circuit becomes faster. The supply voltage used in most CMOS circuits has been 5 V for many years. In the last two to three years, however, as channel lengths have been pushed into the deep-submicron region below 0.5 μm, the supply voltage has dropped for reliability reasons. This trend is summarized in **Figure 1**. Currently the supply voltage for the state-of-the-art 0.35-μm CMOS is 3.3 V, and this will drop to 2.5 V for 0.25-μm CMOS within the next two years. As the nominal CMOS channel length is further reduced, to $\leq$0.15 μm, supply voltage will have to drop still more to preserve an acceptable device lifetime. Despite the drop in the supply voltage, device performance is preserved as channel length is reduced. CMOS threshold voltage is not easily scalable in all applications, however,

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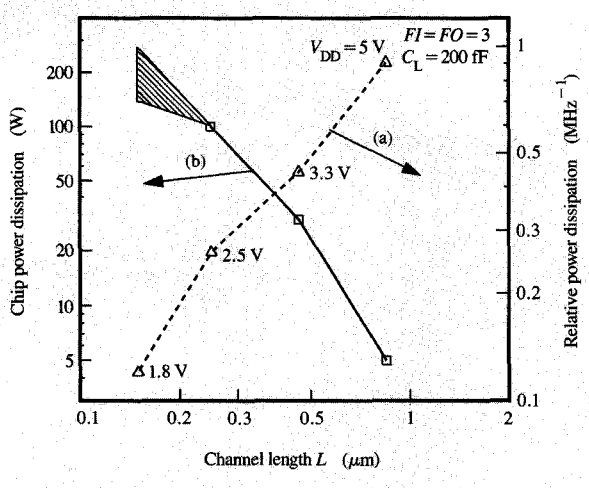


Figure 1

Trends observed in CMOS technology: (a) relative switching energy (power dissipation); (b) chip power dissipation.

and places a limit on how much the supply voltage can be reduced without loss in performance. Figure 1 shows the relative switching energy for four generations of CMOS devices. At every generation, there is a marked improvement in relative switching power. However, as the speed and density improve, the power consumption increases drastically in a chip that fully utilizes the speed and density of a technology and the most advanced CMOS circuit and logic design practices. The maximum reported chip power for every generation is also shown in Figure 1. For a 0.35-μm CMOS chip, this power is in the tens of watts; it is predicted to be about 100 W for a 0.25-μm CMOS chip. A straight scaling of CMOS below 0.25 μm leads not only to improved performance, but also to very high power in chips that fully utilize the technology. Thus, it is clear that in addition to hot-electron degradation (the primary reason for reducing the supply voltage), power consumption must be considered in choosing the elements of a sub-0.25-μm CMOS technology for high-performance logic. Means must be devised to reduce the power effectively. One effective way of reducing the chip power is to drop the supply voltage even faster than necessitated by lifetime limitations. At lower voltages, the performance of CMOS devices on bulk silicon substrates is severely affected by junction capacitance (which is becoming more important in custom-designed circuits) and by the body effect (which raises the threshold and causes severe degradation in the performance of circuits with stacked and pass gate devices). Using SOI (silicon-on-insulator) substrates, however, eliminates many of the obstacles faced by bulk-substrate CMOS at low voltages. There is no junction capacitance on SOI. Furthermore, since the subthreshold slope of an SOI device can be lower than 60 mV/decade, the device-apparent threshold and supply voltage can be further reduced below those shown in Figure 1, while incurring no more leakage than its bulk counterpart.

In this paper, a 0.15-μm bulk CMOS technology is first described. Compared to previous generations, this technology has a number of novel device design elements which allow scaling of the device to below 0.1 μm. The technology also uses a polycide-stack gate to reduce gate resistance. Very high performance has been obtained, but power considerations present serious limitations.

Next, elements of a high-performance CMOS-on-SOI device are described. Silicon-on-insulator, as an alternative substrate for silicon integrated circuits, has existed for some time, but has failed to break into the mainstream of CMOS applications. The biggest barrier associated with SOI has been the so-called floating-body effect that leads to lower device breakdown voltages (below conventional supply voltages) in CMOS generations at effective channel lengths of 0.35 μm or less. Recently, however, concerns about high power dissipation and the need for reduced supply voltages have opened a window of opportunity for SOI as the substrate for the most advanced CMOS designs. In Section 3 of this paper, a high-performance, low-power CMOS-on-SOI technology is described. To demonstrate such a technology, it was necessary to depart from the present-day SOI technology practice of using fully depleted films by using undepleted designs, which are shown to be superior in every way. Next, in Section 4, the unique benefits of SOI for a near-1.0-V technology are discussed. To show the potential of this technology, it was applied to a 512Kb SRAM with access time better than 3.5 ns at 1.X V.

2. A 0.15-μm bulk CMOS technology

Currently, the state-of-the-art CMOS device has a 0.25-μm effective channel length and operates at 2.5 V [1]. As the technology is extended into the deep-submicron range, it is estimated that the next generation will have a nominal channel length of 0.15 μm at something less than 2.0 V. To develop this technology, a number of problems related to device design and manufacturing must be overcome, including control of short-channel effects, reduction of gate resistance, and improvement of density (isolation, metal pitches, and the number of metal levels). A cross section of a CMOS device is shown in **Figure 2.** It uses a number of changes from previous CMOS technologies, including highly nonuniform channel doping, an ultra-shallow source–drain extension and halo, a polycided gate stack, and in general tighter ground rules than previous

generations. In this section some of the key elements used in device design are reviewed, and circuit results using this technology are presented.

- *Device design*

Control of short-channel effects

Control of short-channel effects (SCE) is one of the most critical issues faced in scaling into the submicron range [2, 3]. In developing a 0.15-μm CMOS technology, because of variations in gate length caused by lithography and processing, it is estimated that threshold voltage and roll-off current must remain acceptable at effective channel lengths, L_{eff}, of less than 0.1 μm. In other words, SCE must be acceptable in devices with $L_{eff} \leq 0.1$ μm. To achieve such SCE, two departures from previous CMOS technologies were introduced: highly nonuniform channel doping and an ultra-shallow source–drain extension and halo. With these techniques, devices with excellent SCE below 0.1 μm for use in a 0.15-μm CMOS technology were obtained.

Nonuniform channel profile The design of the CMOS channel profile involves a careful choice of well background doping to control punch-through, and a shallow threshold implant to bring the device threshold to the desired value [4, 5]. This method of design can lead to minimum body effect and junction capacitance. As the channel length is scaled to 0.25 μm and below, the background and channel doping must be raised to values of 3×10^{17} cm^{-3} and higher in order to control short-channel effects. This leads to reduced mobility and difficulty in obtaining a low threshold. To circumvent these problems, the use of a nonuniform channel implant has been suggested and implemented, mostly in deep-submicron devices. Nonuniform channel doping can also produce better short-channel effects, although this result has been shown by simulation only, with no substantiating experimental data. According to the simulations, for best SCE results it is desirable to place the peak as close to the surface as possible. A variety of methods have been used to obtain nonuniform doping: boron implantation [6], indium channel implantation [7], silicon epitaxial growth on a heavily doped substrate [8], and BF_2 implantation [9]. To maximize the nonuniform channel doping, indium was used in our work, since an indium channel implant [10] produces one of the sharpest profiles. Devices with uniform channel doping and those with highly nonuniform indium doping were systematically compared using a 0.25-μm CMOS technology [11]. **Figure 3** shows the channel doping profile of the two cases [SIMS (secondary ion mass spectroscopy) measurement], **Figure 4** the high drain (V_{DS} = 2.5 V) threshold roll-off for the two cases. Although the nonuniform (indium) case has a lower V_t than the uniform doping case (boron), it has significantly better threshold roll-off. This shows that a nonuniform channel doping, in particular one obtained by indium channel implantation, is superior to uniform channel doping in terms of SCE. There is some penalty, however, in using the indium channel implant: There is about 4% degradation

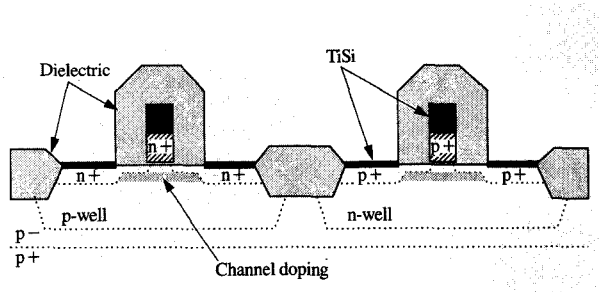


Figure 2

Cross section of a finished 0.15-μm technology.

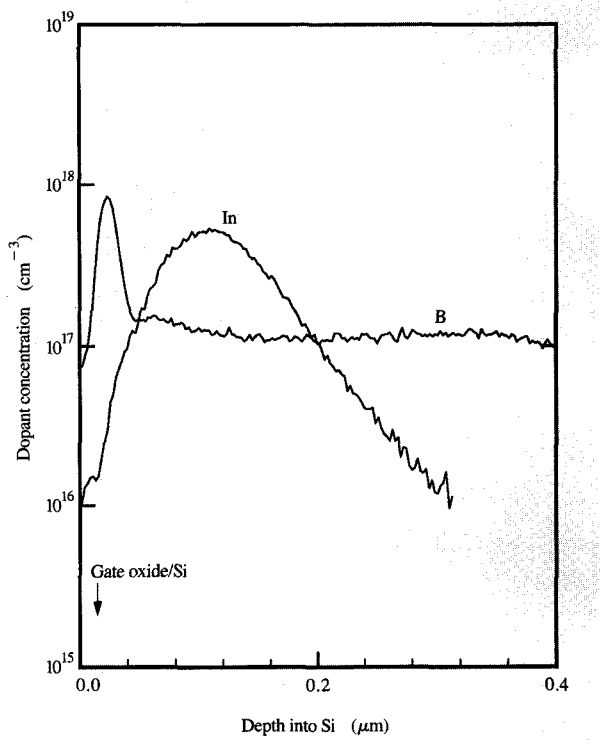


Figure 3

SIMS measurement of nonuniform (indium) and uniform (boron) channel doping used in SCE study.

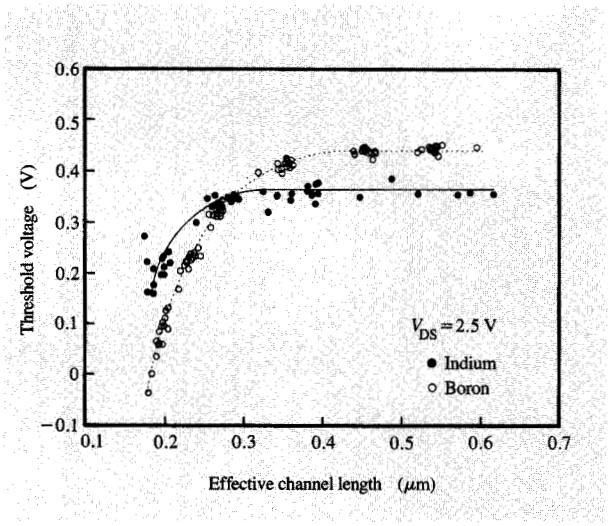


Figure 4

Threshold roll-off for high drain voltage (V_{DS} = 2.5 V) in (a) a device with nonuniform indium implantation (long-channel linear low-V_{DS} threshold, 0.40 V) and (b) an n-MOS device with uniform boron implantation. Despite a lower threshold, the nonuniformly implanted device has a better roll-off.

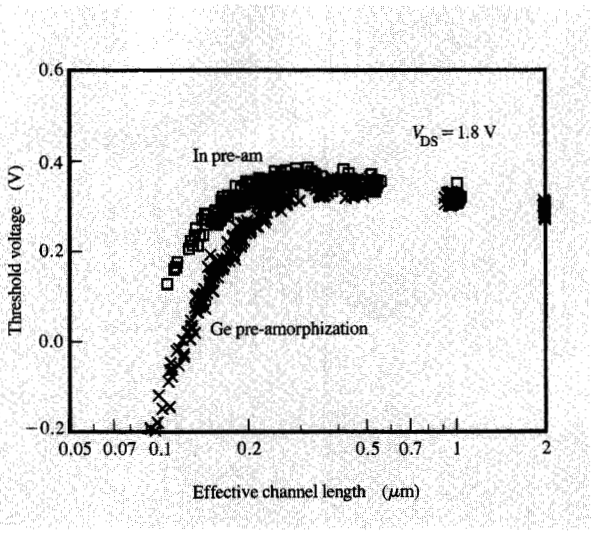


Figure 6

Threshold roll-off for high drain voltage (V_{DS} = 2.5 V) in an n-MOS device with (preamorphized with In) and without (preamorphized with Ge) halo. Arsenic energy was 10 keV. (Indium channel implant was at 150 keV.)

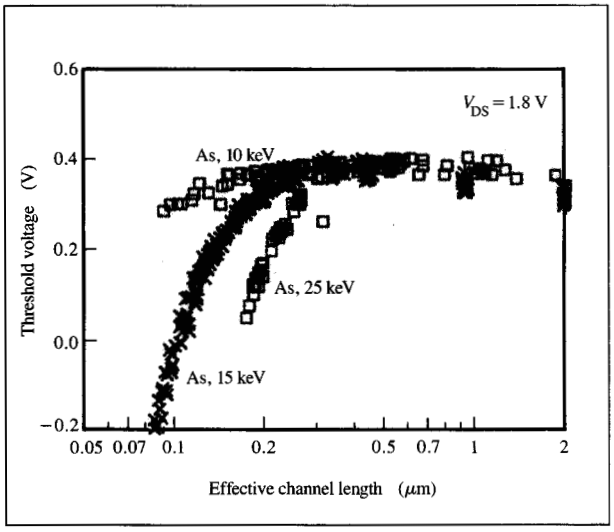


Figure 5

Threshold roll-off for high drain voltage (V_{DS} = 1.8 V) at three different n-MOS extension energies, showing the sensitivity of roll-off to energy. (Indium channel implant was at 190 keV.)

in the transconductance, a slightly higher body effect (the threshold shift, ΔV_t, at a body potential of $V_{BS} = -2$ V is 25% higher for the indium-implanted case, compared with the uniform boron case having the same threshold), and a higher junction capacitance (up to 25% higher for the best SCE) [11].

Ultra-shallow source–drain junction and halo The use of nonuniform channel doping in itself is not enough to reduce the SCE in 0.15-μm devices to an acceptable range. To further improve the SCE, the junction depth must be reduced, as shown by a first-order calculation [12]. In quarter-micron CMOS technology, the junction depth has been reduced to 0.11–0.15 μm (down from the $\geq$0.2 μm used in 0.35-μm CMOS) [13]. The junctions in 0.25-μm CMOS have been salicided, and thus cannot be reduced further because of a large increase in junction leakage and source–drain resistance. In a 0.15-μm CMOS device, source–drain extension has been used: a very shallow junction at the edge of the source and drain where no silicidation takes place, and a deeper junction away from the source–drain edge where silicidation occurs (Figure 2). The use of source–drain extension, because of the shallower junction, reduces the gate and source–drain overlap capacitance. In addition to reducing SCE, a more abrupt extension junction, because of the low-energy implants used, reduces source–drain parasitic resistance and leads to higher transconductance. To show the effect of junction depth on SCE, n-MOS devices were fabricated with different extension energies. **Figure 5** shows the effect of extension depth on threshold roll-off. As expected, lower energy results in better SCE. To further reduce the

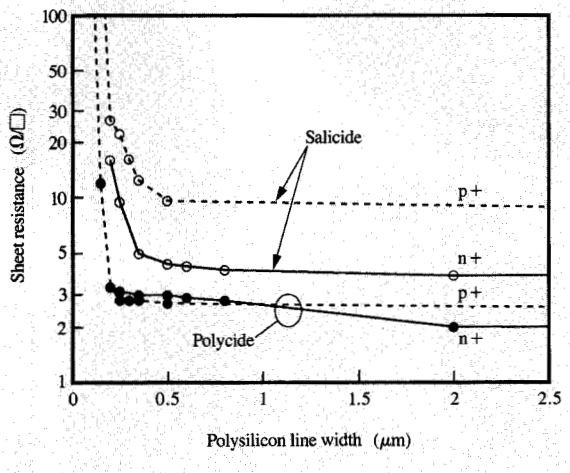


Figure 7

Polysilicon sheet resistance vs. line width for salicided and polycided cases.

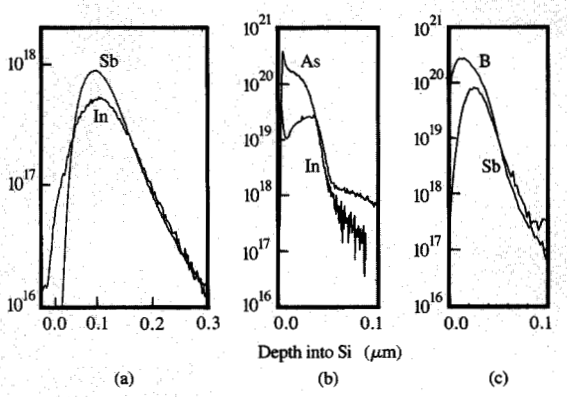


Figure 8

SIMS measurement of the channel implant for (a) n-MOS and p-MOS; and the source–drain extension and halo profiles for (b) n-MOS and (c) p-MOS.

SCE, a halo (counter-doping around the junction) was used around the extensions. **Figure 6** shows the effect with and without the halo. In the latter case, preamorphization was done with Ge; in the halo case, preamorphization was done with indium, which also serves as the halo. A combination of extensions, the halo, and nonuniform channel doping can make the SCE acceptable for channel lengths below 0.1 μm.

Polycide gate stack One of the important issues faced when scaling CMOS into the deep-submicron regime is that the gate *RC* time required to charge and discharge the polysilicon gate becomes a significant part of the device delay. There are two concerns: the absolute value of the gate resistance and the variation in that value (which affects the circuit design). Salicide structures have been used in CMOS technologies down to 0.25-μm channel length, but barring some breakthrough, at present they seem unscalable to technologies below 0.2 μm. For 0.15-μm CMOS, a $TiSi_2$ polycide gate stack was used. Polycide significantly complicates the process: The polysilicon must be pre-doped before the deposition of $TiSi_2$, and a spacer must be deposited to protect the polycide gate stack during high-temperature heat cycles. Nevertheless, some form of polycide might be indispensable for the highest-performance circuits. **Figure 7** shows polysilicon sheet resistivity vs. polysilicon width for salicided and polycided cases: With polycide, it is possible to obtain low sheet resistivity down to gate widths of about 0.15 μm.

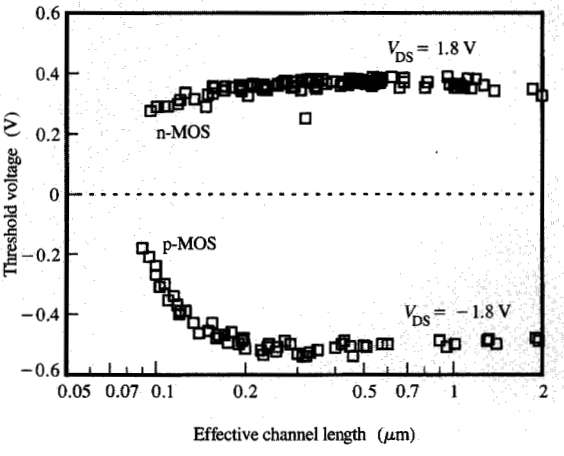
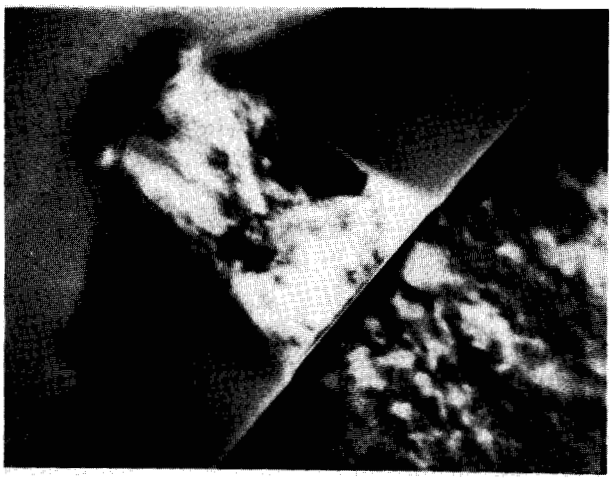


Figure 9

Threshold roll-off for 0.15-μm CMOS at $V_{DS} = 1.8$ V.

Furthermore, the polycide has a much tighter distribution in regions of small polysilicon width.

• *Process technology and electrical results*
Using the technology elements just described, a 0.15-μm CMOS technology has been demonstrated. Indium and antimony were used in the wells to obtain a highly



(a)

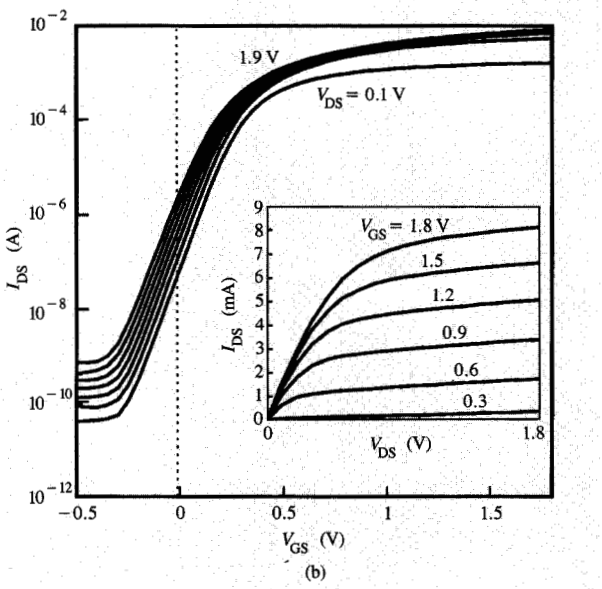


Figure 10

(a) TEM photograph of a 0.06-μm L_{eff} n-MOS (showing L_{drawn} = 0.12 μm) and (b) corresponding device characteristics. Gate oxide = 4.0 nm, and W = 10 μm.

nonuniform channel dopant profile in order to minimize SCE. **Figure 8(a)** is a SIMS (secondary-ion mass spectroscopy) measurement of the channel implant used for n-MOS and p-MOS channel regions. **Figures 8(b)** and **8(c)** are SIMS measurements of source–drain extension and halo of the n-FET and the p-FET. Ultra-shallow source–drain extensions and halos were obtained with an indium preamorphization and halo and a low-energy As implant for the n-MOS devices [14], and Sb preamorphization and a BF_2 implant for the p-MOS devices [15]. The n-FET extension is about 50 nm deep and the p-FET extension is 60 nm deep. These deep source–drain junctions were designed to overwhelm the highly doped region of the well, intersecting the well dopant profile at close to the background level in order to minimize the junction capacitance. The heat cycle was minimized to avoid boron penetration through the gate oxide. **Figure 9** shows the threshold voltage roll-off for these CMOS devices at high V_{DS} (V_{GS} at which $I_{DS}L/W$ = 50 μA at V_{DS} = 1.8 V). Devices exhibit a small short-channel effect for channel lengths down to less than 0.1 μm. **Figure 10(a)** is a TEM (transmission electron microscope) cross section of a 0.06-μm L_{eff} n-MOS device (0.12-μm L_{drawn}); **Figure 10(b)** shows the electrical characteristics (t_{OX} of this device is 4 nm) of the same device. No punchthrough is observed. The drain-induced barrier lowering is 150 mV. The maximum V_t roll-off (from long-channel V_t at low V_{DS} to the high-V_{DS} threshold of this device) is 250 mV, showing the excellent SCE obtainable with this device design. The saturated transconductance of the 0.1-μm n-MOS and p-MOS were, respectively, 450 and 225 mS/mm at $|V_{DS}| = |V_{GS}| = 1.8$ V. Device lifetime was measured as a function of peak substrate current. For a device lifetime of ten years, the peak substrate current must be below 0.1 μA/μm for the minimum-channel-length device. This limits the operating supply to 1.8 V for these devices [14]. Using these devices, a number of ring oscillator structures were fabricated. **Figure 11** shows the unloaded inverter and loaded three-way NAND circuit delay per stage vs. channel length at a supply voltage of 1.8 V. For the loaded three-way NAND ($FI = FO = 3$, C_L = 0.24 pF), a nominal delay of 200 ps and a minimum delay of 150 ps were obtained. The minimum inverter delay was 25 ps at V_{DD} = 1.8 V.

- *Outlook for 0.15-μm bulk CMOS*

These technology elements, and the example using them, demonstrate the feasibility of a 0.15-μm CMOS technology with a minimum channel length below 0.1 μm, with a clear performance gain over the 0.25-μm generation. Such a technology will have many applications in the future. However, because of concerns over extrapolated power,

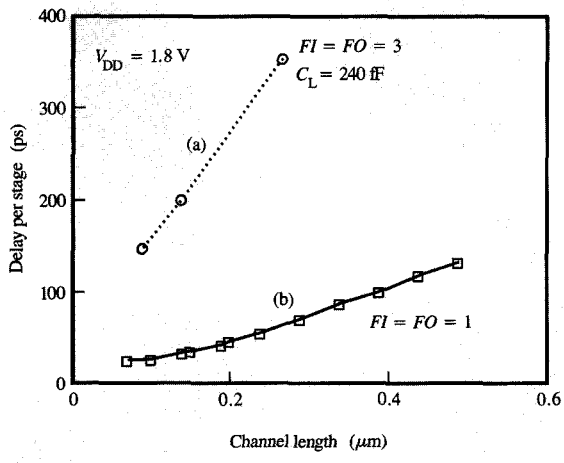


Figure 11

Delay per stage for (a) loaded three-way NAND ($W_n = W_p =$ 15 μm) and (b) unloaded inverter ($W_n = 15$ μm, $W_p = 30$ μm) vs. channel length at a supply voltage of 1.8 V.

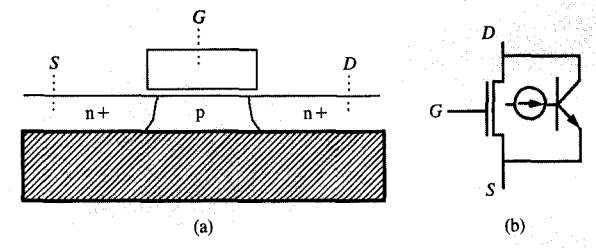


Figure 12

Schematic cross section of (a) n-MOS on SOI and (b) corresponding circuit model.

it remains unclear whether such a technology will be used for the most advanced logic to the full extent of its potential in terms of density–performance. The biggest barrier to its use is the existence of a CMOS technology with lower power at the same performance. This CMOS is described in the next section.

3. A 0.1-μm CMOS technology on SOI

The use of SOI, III–IV compounds, and low-temperature CMOS have been proposed as alternatives or supplements to scaling as means of improving CMOS performance. Over the last two decades, SOI has been used in a number of specialty applications, but one of the primary barriers to its application in mainstream CMOS technology has been a steady improvement in the performance of bulk CMOS. Scaling of bulk CMOS will become more difficult in the future, however, because of issues related to power and manufacturability. Another barrier to the introduction of SOI has been the "floating-body effects" caused by the floating MOS device channel: The floating MOS channel acts as the base of a bipolar device (**Figure 12**), and the base current is supplied by impact ionization. These manifest themselves in the kink effect, anomalous subthreshold currents, and early device breakdown [16]. Kink effect is an increase in output conductance that leads to lower device gain, which is extremely undesirable in high-gain analog circuits. Floating-body effects also manifest themselves in the form of reduced subthreshold slope at high V_{DS}, high device off current I_{off}, inability to turn the device off completely, and, in the extreme case, single-device latching [16]. MOS devices fabricated on SOI, in particular n-MOS devices, have about 2–3 V lower breakdown voltage than comparable bulk devices. Floating-body effects in general have complicated device design on SOI, and have severely restricted the use of CMOS on SOI in high-voltage applications, especially when burn-in conditions (operation at higher than nominal voltage to screen out early failures) are taken into account.

A number of methods have been proposed to either eliminate or minimize floating-body effects. The main strategy has been to use ultra-thin, fully depleted devices (where the film thickness is less than the depletion width of the device). It has been argued that full depletion not only eliminates many of the floating-body effects, but also leads to improved SCE [16]. Another strategy for eliminating floating-body effects has been to use body contact, but that approach results in an area penalty [17]. As a third alternative, it is argued in the next section that the use of undepleted SOI is superior to the fully depleted case. Device design and manufacture are significantly simplified as a result.

- *SOI device design*

The use of fully depleted, ultrathin SOI has been widely advocated to eliminate the body-charging effect and improve the short-channel behavior of devices [16]. Various device structures and designs on SOI have been systematically studied [18] using a two-dimensional device simulator [19]. One of the strongest incentives for using ultrathin, fully depleted SOI has been that the thin SOI film reduces the SCE [16]. It has been reported that as the film thickness is reduced, the threshold voltage roll-off improves and the device threshold drops. This reduction in SCE is only caused, however, by the reduction in source–drain junction depth that is implicit in ultrathin

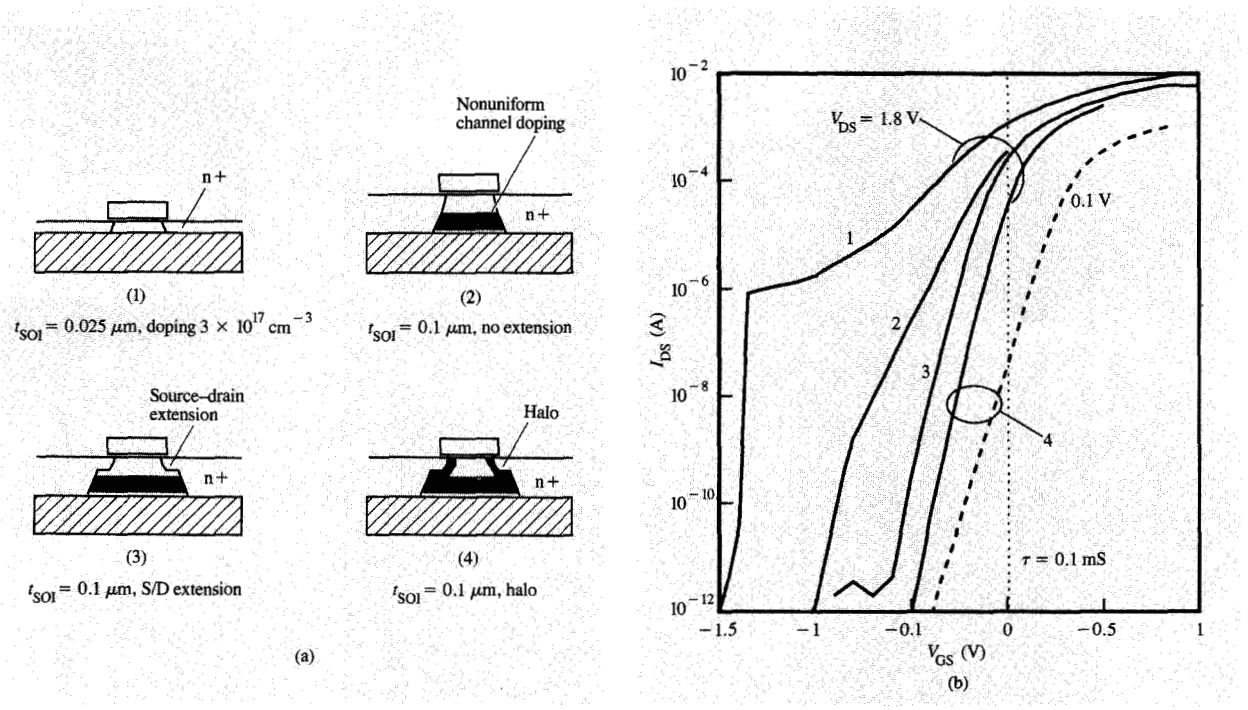


Figure 13

Two-dimensional simulation of a 0.1-μm-channel-length device on ultrathin and thick SOI (with and without extension and halo): (a) corresponding structures, (b) high-V_{DS} currents.

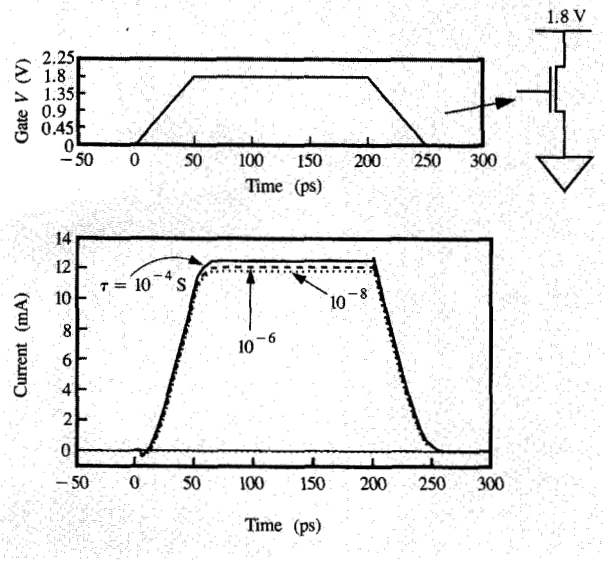
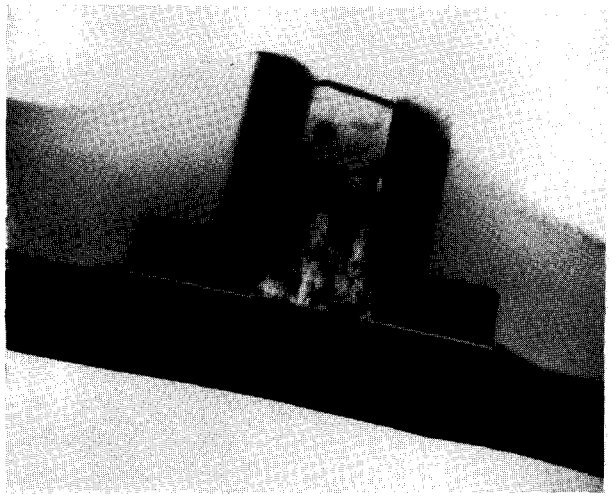


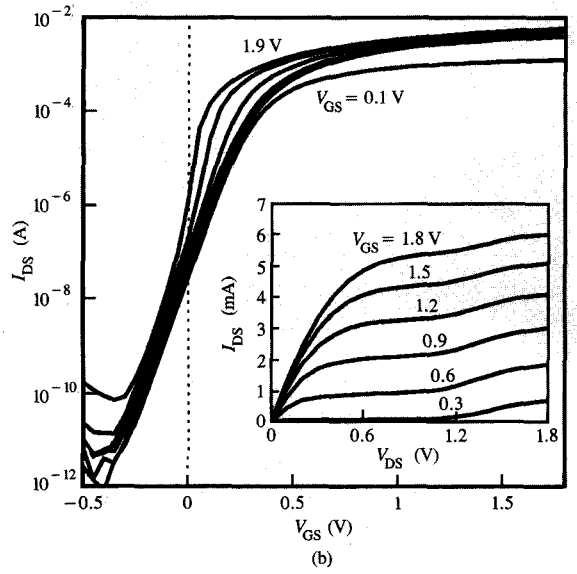
Figure 14

Switching characteristics of a 0.1-μm n-MOS on SOI as the bipolar gain is varied by changing the carrier lifetime. The device current is under the control of the gate, and no large-time-constant current component is observed.

SOI. For the same junction depth, bulk silicon has the same threshold roll-off. In fact, considering the high drain-source voltage subthreshold slope, SOI has *worse* SCE than bulk. To study floating-body effects on SOI, a device simulator with hydrodynamic device modeling and temperature-dependent impact ionization [20] was applied to a 0.1-μm n-MOS with 5 nm gate oxide (with the same doping profiles as those used in our regular fabrication process when applicable). A carrier lifetime of 10^{-6}–10^{-4} best approximated the actual device behavior. It was found that ultrathin SOI ($t_{SOI} \ll t_{depletion}$) results in significant reduction of floating-body effects (in particular the kink effect). The reduction in floating-body effects is very sensitive to SOI film thickness, and even a 5–10-nm increase in film thickness brings back the floating-body effects in the form of device leakage that cannot be turned off. Thus, in order to eliminate bipolar effects, the SOI film thickness must always be well below the depletion width with tight control. This results in a low device threshold V_t which cannot be increased by raising the substrate doping (otherwise, the device will not be fully depleted). Furthermore, using fully depleted films, even in the absence of bipolar effects, results in changes in the low-V_{DS} device threshold because of thickness variations [21]. This requirement of thickness control, even in the absence



(a)



(b)

Figure 15

(a) TEM cross section of a 0.13-μm L_{drawn} n-MOS on SOI; (b) corresponding device characteristics (0.07-μm L_{eff}).

of bipolar effects, is a severe limitation on the use of ultrathin SOI in deep-submicron CMOS.

To eliminate the V_t sensitivity for deep-submicron CMOS, designs with thin but undepleted SOI were studied [18]. Undepleted SOI has a number of benefits: V_t sensitivity to SOI thickness is eliminated; the use of highly nonuniform retrograde channel doping becomes feasible, and, more significantly, any threshold can be achieved simply by changing the film doping. The major drawback of undepleted SOI is the existence of floating-body effects. To solve this problem, source–drain extensions were used to significantly reduce the emitter and collector areas of the parasitic lateral bipolar device, and thus reduce its current. The use of nonuniform doping increases the back interface doping, thus increasing the bipolar Gummel number and further reducing the gain. The use of extension and nonuniform doping also significantly improves the SCE.

Figure 13(a) summarizes the structures studied: Ultrathin SOI (1), thick SOI (2), thick SOI with extension (3), and halo (4). **Figure 13(b)** shows the high drain characteristics of a 0.1-μm-channel-length MOS. Ultrathin SOI can eliminate the body effect, but suffers from low threshold and excess SCE. Thick SOI has a high leakage (a consequence of bipolar action). MOS with extension and halo results in low leakage but a sub-60-mV/dec subthreshold slope (a consequence of floating-body effects). The low threshold in this case can be remedied by using higher film doping.

The main drawback of undepleted SOI is that the kink effect is still present, leading to a reduction of device gain. This manifests itself in lower amplifier gain. The operational amplifier on SOI has about 10× lower gain and slightly higher offset voltages [18]. In digital circuits, the important device characteristics are the on and off currents. Thus, the kink effect does not affect the performance of the digital circuit. In fact, it leads to more current, and is beneficial. To show that this excess current, which is due to the bipolar device, can be turned on and off quickly and with no long-lasting residual currents, a simulation of a switching 0.1-μm device was carried out. The gate was turned on and off in 50 ps, and the bipolar gain was varied by changing the lifetime. The result is shown in **Figure 14**. As the lifetime is increased, one obtains more current, as expected, and in all cases the device current is under gate control and can be turned on and off quickly. In cases of analog circuits where high gain in a device is desired, body contact is necessary [17].

In summary, it has been shown through simulation that although the use of fully depleted films eliminates floating-body effects, it does not result in better SCE (when compared to a bulk MOS device of similar junction depth). In fact, ultrathin SOI results in worse SCE and threshold sensitivity to thickness. Its perceived benefit of eliminating floating-body effects is very sensitive to SOI thickness. All of these characteristics severely restrict the use of fully depleted SOI in the deep-submicron range and bring into

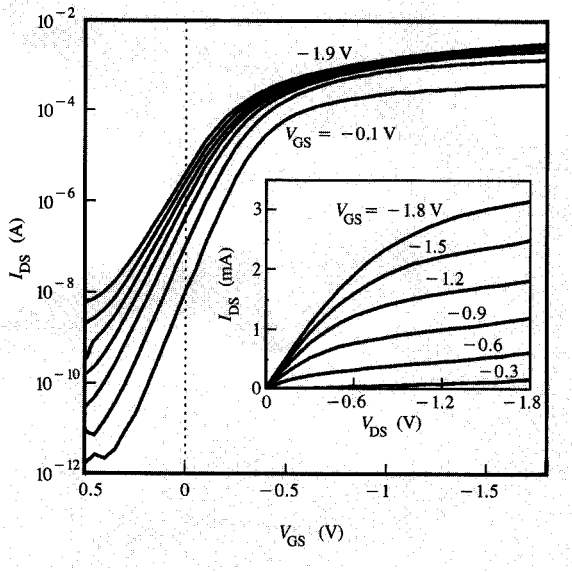


Figure 16

Device characteristics of an 0.08-μm L_{eff} p-MOS.

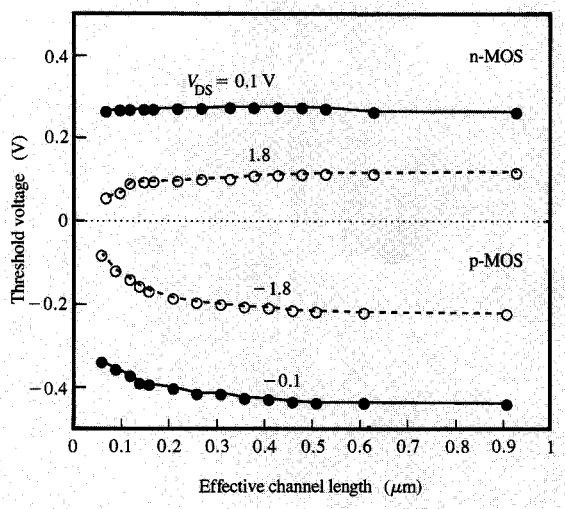


Figure 17

Threshold roll-off for 0.1-μm CMOS at V_{DS} = 0.1 V and V_{DS} = 1.8 V.

question the feasibility of a fully depleted, high-threshold, manufacturable design point. It has been shown that by using undepleted films and proper device design, it is possible to reduce floating-body effects in MOS devices to an acceptable range. This design is now being used in a high-performance 0.1-μm CMOS technology.

• *Process technology and electrical characteristics*

SOI devices with extension, halo, and nonuniform channel doping, similar to the bulk structure of Figure 2, were fabricated on relatively thick, undepleted SOI (100–150 nm) [18]. The gate oxide thickness was 4.2 nm. **Figure 15(a)** is a cross section of a finished n-MOS device with a drawn channel length of 0.13 μm. **Figure 15(b)** shows the characteristics of the same device with an effective channel length of 0.07 μm and width of 10 μm. In fact, using TEM to determine the physical length, it was found that there was very little SCE down to 0.055-μm effective channel length, and even the 0.045-μm device is not in punchthrough [although the drain-induced barrier lowering (DIBL) is considerable] [18]. **Figure 16** shows the characteristics of an 0.08-μm p-MOS device. The p-MOS device has slightly worse SCE because the p-MOS extension is deeper than that of the n-MOS device. **Figure 17** shows the threshold roll-off at low (0.1-V) and high (1.8-V) drain bias. No low-V_{DS} roll-off was observed. At high V_{DS}, V_t is reduced due to floating-body effects. The threshold can be increased if desired by just increasing the film doping. Saturated transconductance on SOI was also measured. Devices on SOI had consistently 10 to 20% lower saturated transconductance than their bulk counterparts, perhaps because of heating effects [22]. One of the concerns about CMOS on SOI is the low breakdown voltage of the n-FETs, which affects high-voltage operation and the burn-in strategy. **Figure 18** is a plot of n-MOS breakdown vs. channel length. **Figure 19** shows the unloaded inverter and loaded three-way NAND circuit delay per stage vs. channel length at a supply voltage of 1.8 V. Inverter delays as low as 20 ps at a channel length of 0.1 μm were obtained. For the loaded three-way NAND ($FI = FO = 3$, C_L = 0.3 pF), a minimum delay of 130 ps was obtained (a loaded three-way NAND $FI = FO = 3$ with C_L equivalent to 1 mm of Al wire has a 140-ps delay). At channel lengths below 0.2 μm, circuit performance is affected by the large gate resistance. **Figure 20** shows the switching power per stage for (a) unloaded and (b) loaded three-way NAND circuits with 0.15-μm devices on bulk and on SOI. At a given delay per stage, SOI requires the lower operating power. This figure illustrates the real reason for using SOI in the deep-submicron region.

4. SOI for low power and application to 512Kb SRAM

• *SOI for low (1.0-V) voltage*

As is apparent from Figure 1, although CMOS has been the technology of choice for low-power electronics, today

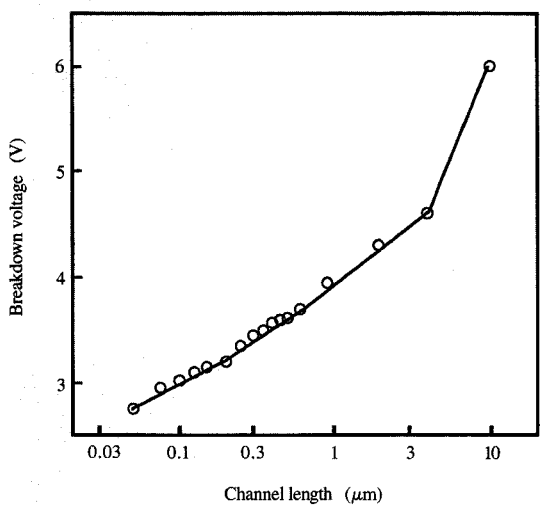


Figure 18

Breakdown voltage for n-MOS devices (V_{DS} at $V_{GS} = V_t$, where I_{DS} is half the value of the I_{DS} at $V_{DS} = V_{GS} = 1.8$ V).

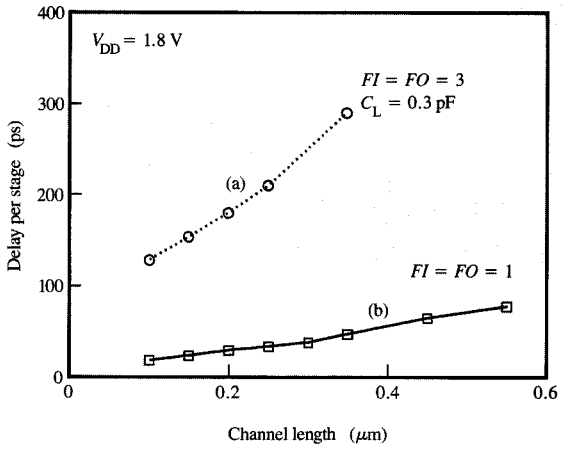


Figure 19

Delay per stage for (a) loaded three-way NAND and (b) unloaded inverter vs. channel length.

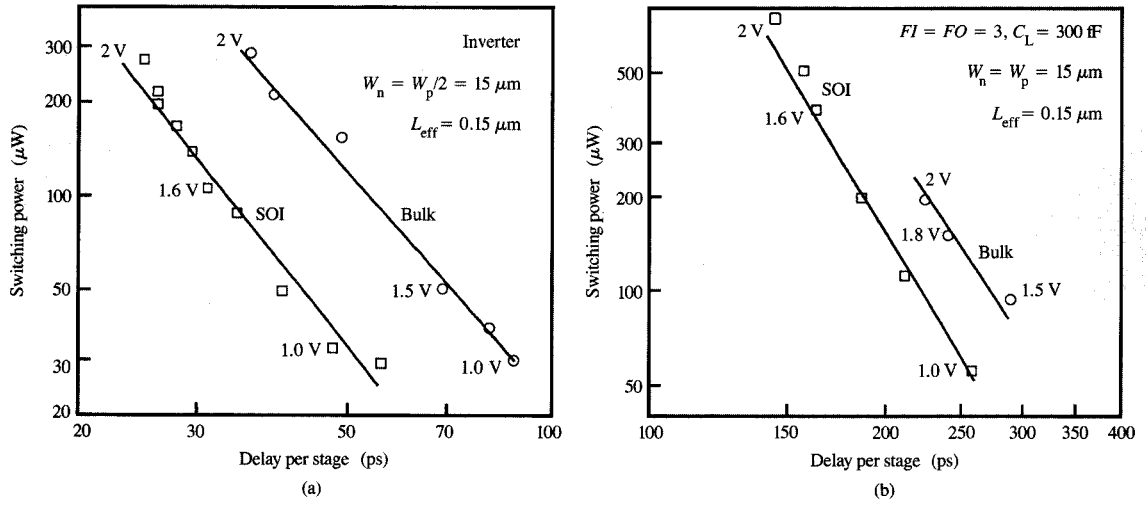


Figure 20

Measured switching power of (a) single-stage inverter ($W_n = 15$ μm, $W_p = 30$ μm) and (b) three-way NAND ($FI = FO = 3$, $C_L = 0.3$ pF, $W_n = W_p = 30$ μm) at $L_{eff} = 0.15$ μm.

some high-end chips consume power in the range of tens of watts, and this is projected to rise rapidly in the near future to a point at which serious compromise must be made in performance and/or the density of the chip in

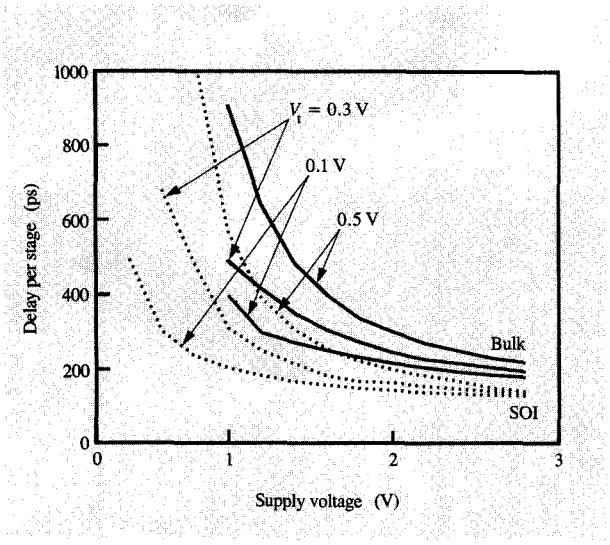


Figure 21

Simulation of fully loaded NAND vs. supply voltage for different thresholds on bulk and on SOI ($FI = FO = 3$, $C_L = 0.2$ pF, $W_n = W_p = 30$ μm at $L_{eff} = 0.25$ μm, using 0.25-μm CMOS models).

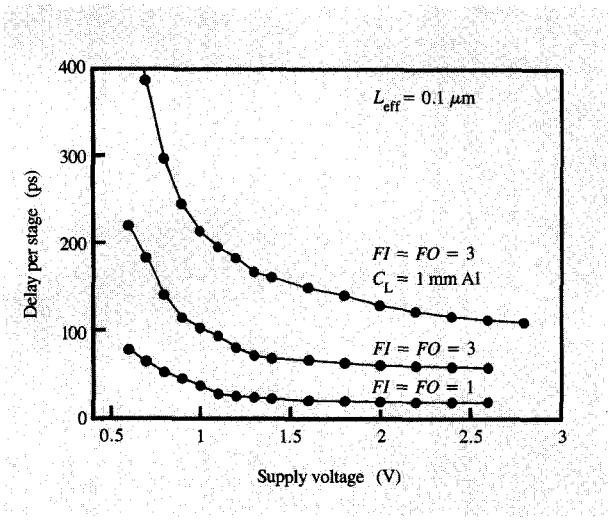


Figure 22

Measured ring oscillator performance for loaded and unloaded cases vs. supply (at $L_{eff} = 0.1$ μm).

order to keep power consumption in check. Scaling of the power supply voltage can help significantly to reduce the power, but this has usually been accompanied by a large drop in performance. This is a consequence of increased junction capacitance (which is already rather large in custom-designed microprocessors) and reduced drive current due to body effects. Both of these effects become more significant at lower voltages. SOI is the ideal substrate for low-voltage CMOS technology, because both body effects and junction capacitance are nearly absent on SOI. SOI operating at 1 V shows a significant power–delay improvement, as is apparent in Figure 20.

When operating at low voltage, it is desirable to drop the threshold as much as possible; the lower threshold leads to significantly better performance, especially at low voltages. This is shown in **Figure 21**, where circuit simulations of a loaded three-way NAND were carried out at different thresholds (using 0.25-μm-technology device models, with $L_{eff} = 0.25$ μm). It is clear that at low supply voltages the performance is critically dependent on threshold voltages, and that lower thresholds lead to improved performance. At low voltages, performance is also very sensitive to threshold voltage variations that are usually present in a given technology. Reduced V_t also is beneficial in reducing the V_t sensitivity of performance at low voltages. Lower thresholds do have the side effect of increasing the standby power of the chip (due to leakage), but the increase in standby power is usually negligible when compared to the gain in performance and reduction in active power that is the result of reduced supply and V_t. Undepleted SOI is particularly useful when used for low-voltage CMOS, because it has a sharper high-V_{DS} subthreshold slope and thus a lower V_t at the same leakage. In our SOI CMOS, high-V_{DS} subthreshold slopes are in the high 50's mV/dec range compared to high 80's mV/dec for bulk CMOS (this is caused by floating-body effects and the subsequent bipolar action, which also leads to a kink effect). This reduction in apparent V_t at high drain voltage and increase in overdrive (without increase in leakage) is particularly useful in a low-voltage CMOS. Furthermore, SOI has almost no junction capacitance. MOS body effects on bulk Si (increase in V_t associated with finite source-body bias) are also nonexistent in SOI. In Figure 21, delay per stage of the same loaded NAND inverter is also shown; a large increase in speed due to elimination of junction capacitance and lower threshold is obtained.

Figure 22 shows the performance of ring oscillators measured (using a picoprobe to verify full swing) at voltages all the way down to 0.6 V. Unloaded ring delays are 40 and 72 ps at channel lengths of 0.1 and 0.2 μm, respectively, at 1 V. Unloaded three-way NAND delays are 96 and 170 ps, and fully loaded delays ($FI = FO = 3$, $C_L = 1$ mm Al) are 195 and 310 ps at channel lengths of 0.1 and 0.2 μm, respectively. Rings working all the way to 0.6 V with speeds much less dependent on supply voltage (when compared to bulk CMOS monitor devices) were obtained.

• *Application to 512Kb SRAM*

To show the potential of this device design and the capability of SOI when operated at low voltage, this technology was applied to a three-level-metal, fully pipelined 512Kb SRAM [23]. This SRAM had previously been fabricated in a 0.5-μm 3.6-V CMOS technology, and an access time of 3.8 ns at 3.6 V had been obtained. For SRAM on SOI, SIMOX (separation by implantation of oxygen) wafers were used. Bulk monitors were also included. The same mask set as before was used [24], except that the gate level was reduced to 0.25 μm L_{drawn} (measured after gate RIE). **Figure 23** shows the SRAM access waveform at a supply voltage of 1.0 V. **Figure 24** shows access time vs. supply voltage for the SOI SRAM. The bulk monitor had access times of 5.5 and 11 ns at 1.6- and 1.0-V supplies (the bulk devices had a threshold of 0.5 V for both p-FET and n-FET). Neither the bulk nor the SOI version worked at supply voltages above 1.6 V. This is most probably because they are self-resetting circuits, designed using a 3.6-V bulk technology. Nevertheless, this successful demonstration of SRAM shows the real potential of the present SOI device design, and underlies the fact that undepleted SOI is capable of delivering high-performance circuits at low supply voltages with a significant performance advantage.

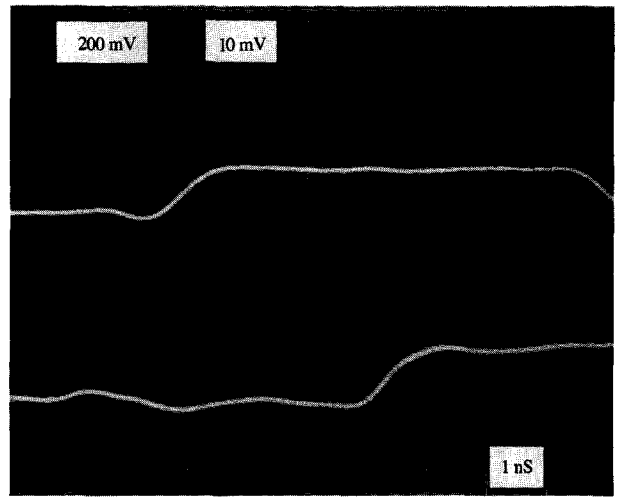


Figure 23

SRAM access time at supply of 1 V.

Summary

In this paper, two potential CMOS technologies for use in the 1.X-V region have been described. First, an advanced 0.15-μm CMOS technology on bulk silicon was presented. Its key elements were highly nonuniform channel doping (obtained by indium and antimony channel implants), shallow source–drain extensions and halo (by In and Sb preamorphization and low-energy As and BF_2 implantation), and a polycide gate stack. Maximum high-V_{DS} threshold roll-off was 250 mV at an effective channel length of 0.06 μm. A loaded NAND ($FI = FO = 3$, C_L = 240 fF) delay of 200 ps and an unloaded delay of 33 ps at a supply voltage of 1.8 V were demonstrated at the nominal channel lengths.

It is expected that there will be serious concern about the power consumption of the most advanced logic done using such technology, but CMOS on SOI offers a way out: the same or better performance at lower power. A new design point for SOI, which is manufacturable and extendible to the sub-0.1-μm range, has been defined. This design point uses relatively thick undepleted (0.15-μm) SOI film, highly nonuniform channel doping, source–drain extension, and halo. Excellent short-channel effects (SCE) down to channel lengths below 0.1 μm were obtained. These devices were applied to a variety of circuits, and very high speeds were obtained. Unloaded delay was 20 ps, unloaded NAND ($FI = FO = 3$) delay was 64 ps, and loaded NAND ($FI = FO = 3$, C_L = 0.3 pF) delay was 130 ps at a supply voltage of 1.8 V.

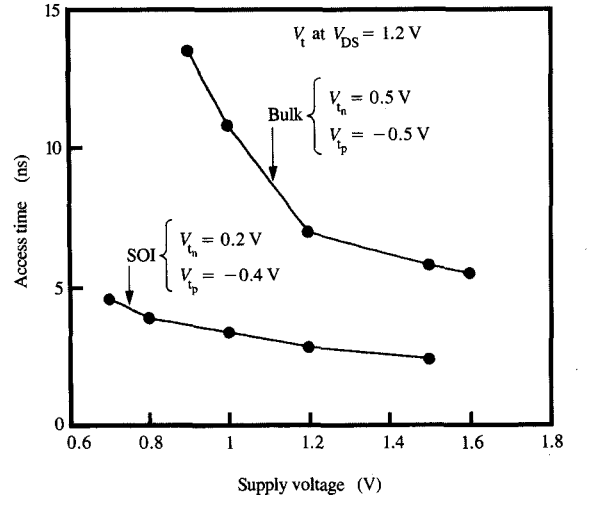


Figure 24

SRAM access time vs. supply.

It has been shown that such SOI technology is particularly useful for a 1.0-V CMOS. This technology was applied to a self-resetting 512Kb SRAM, and access times of 2.5 ns at 1.5 V and 3.5 ns at 1.0 V were obtained.

Concerns about CMOS power and lower operating voltages now allow SOI to mount a serious challenge to bulk silicon. It is expected that in the sub-0.2-μm family of CMOS technologies, SOI will be the substrate of choice.

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