A half-micron CMOS logic generation

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During the early 1990s, half-micron lithography was demonstrated in 16Mb DRAM fabrication. Utilization of this capability for CMOS logic devices within IBM followed with a trio of programs, each with different performance, density, feature list, and schedule. The first version melded 3.3/3.6-V 16Mb DRAM MOSFET devices with an improved version of an existing dense, planar, reliable multilevel back-end-of-line (BEOL) metallization and wiring technology. Since it was built directly from existing technologies, it was released quite quickly. A 3.3-V follow-on technology was added several months later. This logic offering added a local interconnect and a faster device. A second follow-on achieved greater speed improvement, calling upon a 2.5-V power supply and very tight channel-length control to obtain performances 50% above previous-generation standards, at lower power.

Introduction

Until the early 1980s, IBM MOS logic consisted entirely of n-MOS technologies. During the decade of the eighties, however, the advantages of significantly lowered power consumption, simplified design practices, and improved noise immunity ensured that CMOS would overtake n-MOS as the technology of choice. CMOS front-end processing was combined with conventional interconnection technologies to spawn two successful introductory CMOS families [1]. These logic families

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Table 1 Summary of technology elements qualified in IBM CMOS semiconductor technologies prior to introduction of half-micron logic.

Generation (approximate year)	*Technology element*
CMOS 1 (1984)	2.0-μm lithography CMOS devices
CMOS 2 (1986)	1.25-μm lithography LDD elements (sidewall spacers) $TiSi_2$ salicides
1Mb (n-MOS) DRAM (1987)	1.0-μm lithography WSi_2 polycide gates
CMOS 4 (1989)	0.7-μm (MUV) lithography Planarized multilevel BEOL technology Borderless local interconnects Retrograde n-well
16Mb DRAM; CMOS 5 (1992)	0.5-μm (DUV) lithography Shallow-trench isolation Rapid thermal processing

employed linewidths as narrow as 1.25 μm, introduced titanium salicide for low-resistance diffusion regions, and served as vehicles with which early CMOS device problems, such as latch-up, could be characterized and controlled. Synergistic growth with the IBM 1Mb (n-MOS) DRAM sped defect learning.

In 1988, introduction of the IBM 4Mb DRAM marked a coming of age for CMOS; lower power capabilities were utilized to great advantage, and unique possibilities afforded by CMOS processing enabled the implementation of novel low-leakage, high-capacitance memory cells [2]. In addition, small cell size resulting from the use of trench storage nodes pushed interconnection technology to keep pace; planarized passivation layers and damascene plug contacts and vias resulted [3]. Extrapolation of dense one or two levels of planar metallization formed the basis for dense multilevel interconnections [4]. Logic derivatives from the 4Mb DRAM employed these technology macros to produce very dense logic families offering up to four levels of tight-pitch metallization. By the early nineties, the DRAM-derived technology macros were melded with higher-performance devices to build industry-leading logic families in the 0.7–0.8-μm regime. A borderless damascene local interconnection was qualified to significantly improve SRAM density [5] and further improve wireability.

The IBM 16Mb CMOS DRAM, introduced in 1992 [6], signaled continued evolutionary progress in memory density. Deep-UV (DUV) lithography was introduced to manufacturably achieve 0.5-μm feature sizes. Shallow-trench isolation reduced the space required for isolation, improved surface planarity, and integrated well with the advanced application of deep trenches for both signal storage and device isolation. **Table 1** summarizes the progression of CMOS technologies in IBM.

The basic ingredients for the next family of CMOS logic were now coming together. Previous memory and logic generations had demonstrated dense and extendable interconnection processes, continued the development of salicides for low-resistance electrodes, and pursued reliable high-performance devices using optimized drain engineering. Memory development provided denser device isolation and next-generation photolithography. Development of competitive logic devices for the mid-nineties required optimization of these available elements to fit with new device and structural features uniquely required by next-generation logic technologies. What evolved for the IBM logic set in this era was a trio of logic versions.

CMOS 5L was the name given to the initial 3.6-V offering, a low-cost process which could be rapidly introduced by taking maximum advantage of the qualified DRAM base process. A 3.6-V design point was selected for compatibility with existing internal IBM designs. CMOS 5S was a higher-performance follow-on which added several additional features and used a 3.3-V design point compatible with the OEM semiconductor industry. CMOS 5X was a 2.5-V technology designed for even higher performance at lower power consumption. For all three technologies, fabrication begins and ends with nearly identical process steps. Ground rules are very similar. Differences appear mainly in the details of device engineering and the choice of available features.

Device isolation

Chip size for many logic designs is only moderately affected by device isolation efficiency; wiring density is more often the limiting factor. Shallow-trench isolation (STI) was, nevertheless, chosen for all half-micron logic versions despite its somewhat higher wafer processing cost compared to LOCOS (localized oxidation of silicon).

Commonality with concurrent-volume DRAM production was a factor in the decision.

The cost disadvantage also is offset by several other major advantages. For STI, as opposed to LOCOS, pitch is generally limited by photolithographic capability and the minimum active region width required for salicidation. Multidimensional oxidation effects, such as bird's-beak, do not play significant roles. Circuit density can thus be improved significantly for several key circuit types. Static RAM cells, for example, can be made up to 25% smaller by using STI, depending upon layout details. Surface planarity, particularly at the critical point of device gate exposure, is significantly improved. The step height that gate polysilicon encounters at the edges of the STI typically runs 25 nm to 70 nm, versus approximately 90 nm for LOCOS structures. Decreased step height reduces interference-related notching, eases lithographic depth-of-focus concerns, simplifies PSG planarization, and lowers over-etch requirements during contact formation. Note that the direction of the step between isolation and active regions is reversed. With LOCOS, the isolation is "higher" than the active regions. With STI, the isolation is "lower."

The processing of STI for these logic technologies remained essentially the same as for DRAM. Extending the original DRAM-based isolation to dimensions below approximately 0.8 μm, however, required some process modifications. The vertical sidewalls required for the 16Mb DRAM cell make complete trench fill difficult. Since even "good" TEOS (tetraethyl orthosilicate)-based oxide deposition is not perfectly conformal, mid-trench seams became likely as trench aspect ratio increased. **Figure 1** shows one result of incomplete fill; stripping with HF after planarization opens the central seam, and gate polysilicon is subsequently deposited into this seam. The usual over-etching is not sufficient to guarantee removal of the polysilicon in the seam, and line-to-line shorts can result. Modifying the shallow-trench etch provides trench wall tapering without degrading ground rules. Also, using a higher-pressure process for the low-pressure chemical vapor deposition (LPCVD) of the TEOS-based oxide fill improves conformality. These two modifications result in successful processing of trenches to a design width of less than 0.4 μm without resorting to decreasing the trench depth to achieve a smaller aspect ratio. **Figure 2** compares 0.6-μm and 0.4-μm (design) trenches.

One constraint on circuit performance in MOS technologies is diffusion-perimeter capacitance. Boron field doping, typically used with LOCOS for n-MOSFETs, can encroach into device regions and increase perimeter capacitance. Sidewall doping of shallow isolation trenches is unnecessary, however, because the sidewall and corner parasitic devices are well-behaved and do not unacceptably degrade off-current. This difference results in extremely low perimeter capacitance for STI-bordered diffusions. P-channel devices with LOCOS show similar effects due to "snowplowing" of n-well dopants during the long oxidation cycles required to grow thick oxides. Because of its reduced thermal oxidation thickness, p-MOSFET perimeter capacitance also is improved with STI.

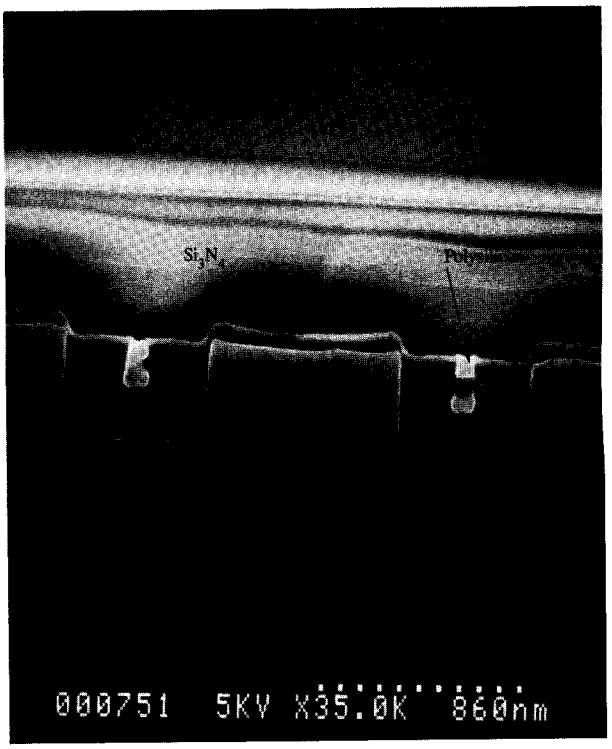


Figure 1

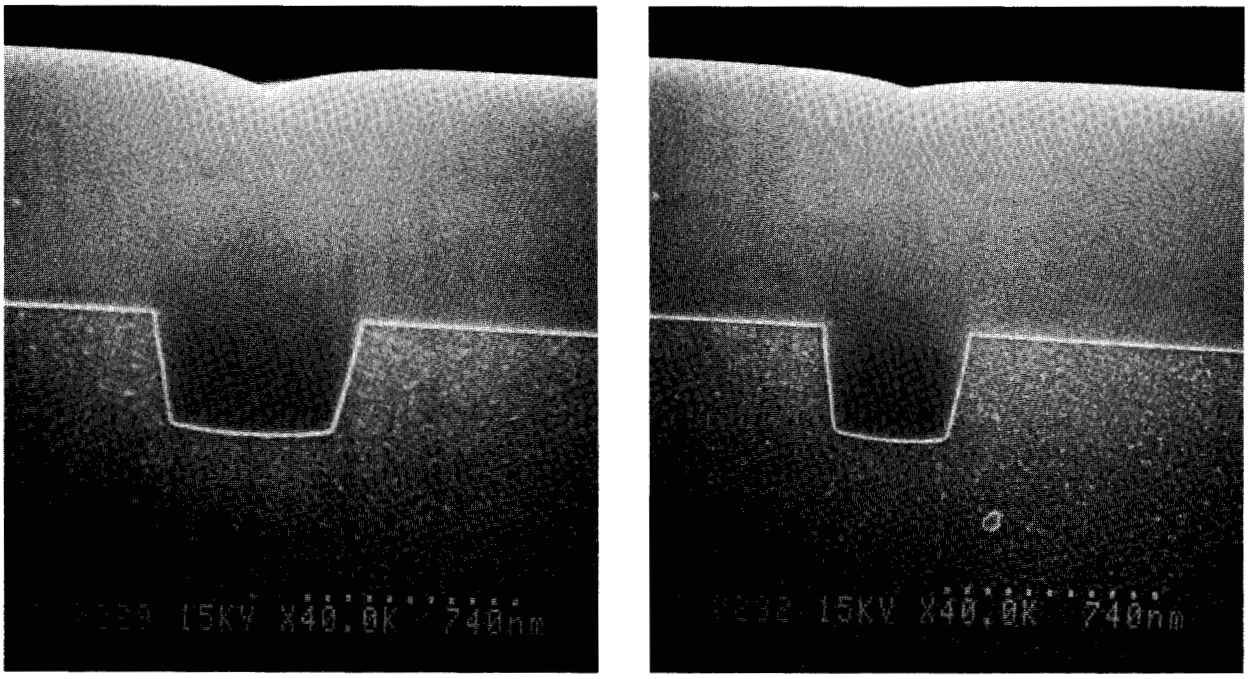
Sub-half-micron isolation features after PSG passivation. No sidewall taper was used. Gate polysilicon filled mid-trench seam and is not completely removed with over-etch. Note that HF highlight dip has enlarged void.

Inherent in any CMOS technology is a parasitic pnpn structure. With sufficient energy, SCR action can be triggered in this pnpn device, resulting in a low-impedance state called latch-up, which then must be suppressed with careful technology design techniques such as low-resistance substrates and retrograde wells. However, since latch-up requires gain from the lateral parasitic bipolar device, STI technologies have a significant advantage over those using LOCOS. Latch-up voltages in CMOS 5 technologies are equivalent to the junction-to-well breakdown voltages and are not a concern.

Device design

- *Base substrate/well processes*

A 2.3-μm 5 $\times$ 10^{15} cm^{-3} boron-doped epitaxial layer on an 0.008-Ω-cm p-type substrate is used for the entire CMOS 5



(a) (b)

Figure 2

STI using ≃75° sidewall taper and higher-pressure TEOS-based fill: (a) 0.60-μm design. (b) 0.40-μm design. Narrow feature has discolored mid-trench region from highlight etch (sample preparation) but no mid-trench void.

family of logic technologies. This choice provides a highly conductive substrate to further improve latch-up immunity and provide low noise.

P-well implants for both isolation and n-MOSFET short-channel control are accomplished with a single p-well mask. Insignificant device-performance compromise is required because of the depth and planarity of the shallow-trench isolation.

A single n-well mask similarly serves for implants to control short-channel p-MOSFET behavior, p-isolation, and latch-up. A deep, retrograde phosphorus implant sets n-well sheet resistance to minimize contact restrictions for latch-up, thereby affording optimal density. The n-well also provides low-impedance decoupling capacitance between V_{DD} and ground because of the high conductivity of the substrate, providing significant built-in noise suppression.

It is primarily in other aspects of MOSFET device engineering that CMOS 5L, CMOS 5S, and CMOS 5X differ.

• *CMOS 5L: 3.6-V DRAM derivative logic*

The objective of the CMOS 5L program was to develop a logic process quickly and with minimal added resource to the 16Mb DRAM activity. Maximizing the number of process steps shared with memory allowed CMOS 5L hardware to benefit directly from memory process learning and to be processed with good turnaround time in the development phase of the program.

The CMOS 5L device design point was dictated by DRAM considerations, namely retention time and high-voltage burn-in. These resulted in a trade-off of performance in order to prevent p-MOSFET hot-carrier damage during product burn-in and poor memory retention time due to gate-induced drain leakage (GIDL) [7].

The technology uses n+ polysilicon gates with a deposited layer of tungsten silicide to provide low sheet resistance. Since the p-MOSFET is a buried-channel device, its channel length is set 50 nm longer than that of the n-MOSFET in deference to the fact that short-channel effects are more severe. Since the gate polysilicon is doped before patterning, junction and gate polysilicon doping are independent, and gate polysilicon depletion is not a concern. However, fluorine present in the tungsten silicide deposition is incorporated into the gate oxide, causing the electrical oxide thickness to be 13.5 nm compared to 12.5 nm as-grown.

Both n-MOSFET and p-MOSFET employ an LDD (lightly doped diffusion) structure to reduce drain field and the resulting hot-carrier degradation. The n-MOSFET LDD is formed by a dual implant consisting of phosphorus to provide junction grading, and arsenic to lower the parasitic series resistance. Boron is used for the p-MOSFET LDD.

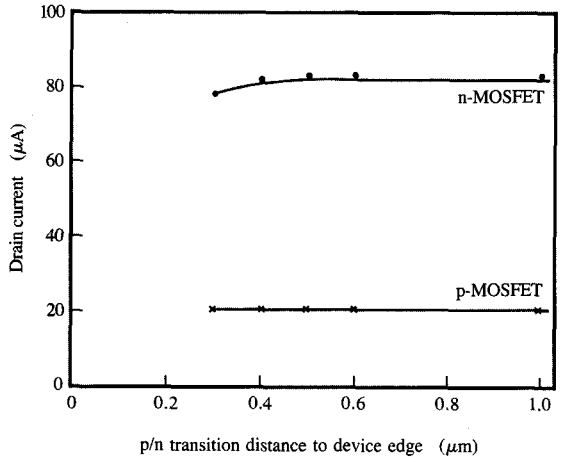


Figure 3

Device current for long-wide device as function of spacing to opposite-polarity polysilicon reservoir. Note that no degradation is observed with spacings of 0.4 μm.

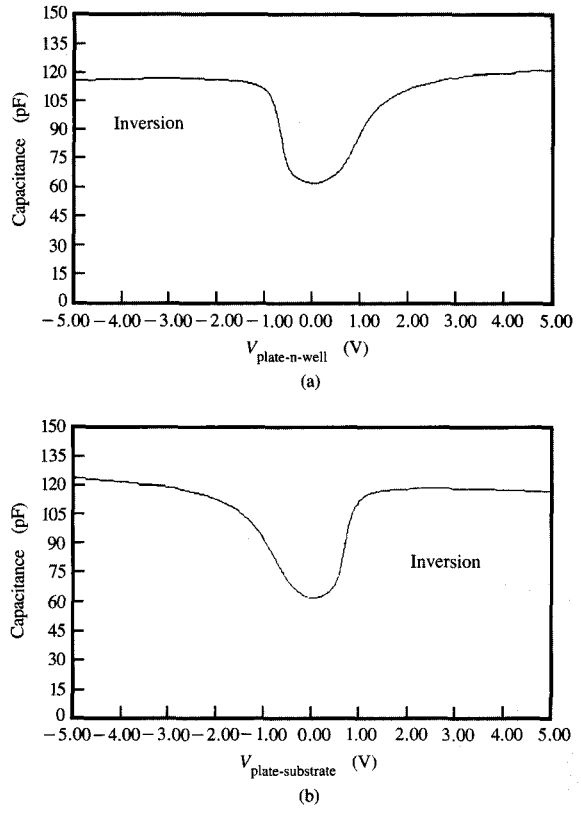


Figure 4

Typical CV plot for (a) p-channel capacitor and (b) n-channel capacitor illustrating polysilicon gate depletion in inversion regions.

Drain junctions are created using arsenic and boron for n-MOSFET and p-MOSFET respectively after formation of a 120-nm oxide spacer. Activation is provided by high-temperature rapid thermal annealing (RTA), which also serves to lower the resistance of the tungsten silicide layer and to reduce the stress accumulated from prior thermal oxidations.

Source/drain diffusion depths are approximately 0.25 μm and 0.30 μm for n-channel and p-channel devices, respectively. Parasitic diffusion resistance is lowered, as in the memory process, by using sputtered titanium reacted with silicon to form self-aligned $TiSi_2$. Rapid thermal processing (RTP) is employed for self-aligned titanium silicide (salicide) formation and transformation processes.

• *CMOS 5S: 3.3-V high-performance logic*

To match the IBM technology to the OEM semiconductor market, an enhanced-performance version of 0.5-μm CMOS targeted at the industry-standard supply voltage of 3.3 V was developed. This version, called CMOS 5S, differs from CMOS 5L in several ways, all motivated by the need to increase MOSFET performance. Dual-workfunction gate electrodes are employed to alleviate short-channel device effects [8]. A lower field results at the drain edge of the p-MOSFET with a p-doped polysilicon gate electrode, which allows operation at channel lengths below 0.25 μm at 3.3 V. The n-MOSFET retains an n-type gate electrode. This complementary gate doping is accomplished through use of the same masks and implants in the source/drain formation with no additional complexity. The polysilicon/tungsten-silicide/nitride gate stack used in CMOS 5L, however, would block the source/drain implants. For this reason, for CMOS 5S a self-aligned titanium silicide (salicide) is formed on the gate electrodes after source/drain ion implantation, to achieve a gate-electrode sheet resistance of 4.5 Ω/□.

Dual-workfunction gate electrodes, now becoming an industry standard, present considerable challenges to process integration. Sufficient thermal processing must follow the source/drain implants to activate the dopant in the gate, yet activation cycles must not disrupt the required shallow junction depth. Furthermore, diffusion of n-type dopants laterally into a p-MOSFET gate (and vice versa) can degrade the drain current if the n/p transition is too close to the active MOSFET. With a 1000°C RTA for source/drain drive-in, no device degradation is observed to below 0.4 μm spacing (**Figure 3.**) The gate-electrode depletion is less than 10% from 5-V accumulation to 3.3-V inversion (**Figure 4.**) An 8.7-nm equivalent

Table 2 Comparison of CMOS 5 technologies.

Technology	*Power supply* (V)	$T_{effective}$ (nm)	X_{J_n} (μm)	X_{J_p} (μm)	*n-FET* L_{eff} (μm)	*p-FET* L_{eff} (μm)	V_{T_n} (V)	V_{T_p} (V)	ID_{SAT_n} (A/M)	ID_{SAT_p} (A/M)	$\tau_{inverter}$ (ps)
CMOS 5L	3.6	13.5	0.25	0.30	0.46	0.51	0.64	−0.84	350	190	90
CMOS 5S	3.3	8.7	0.22	0.22	0.36	0.36	0.60	−0.55	495	230	75
CMOS 5X	2.5	7.7	0.18	0.18	0.25	0.25	0.50	−0.55	484	192	60

gate oxide thickness is achieved with a 7.8-nm as-grown process.

LDD implants are used in both MOSFET polarities. The n-LDD is set to control drain avalanche current and concomitant channel-hot-electron degradation during use. The p-LDD provides superior n-MOSFET-to-p-MOSFET channel-length matching, with gate overlaps of source/drain controlled by one sidewall oxidation post-gate-electrode etch. Phosphorus and boron are implanted, after a 120-nm silicon nitride spacer, to form n+ and p+ junctions, respectively. Nominal performance is improved 20 to 40% over that of the 3.6-V (CMOS 5L) technology.

The same titanium salicide used to lower polysilicon wiring resistance lowers the parasitic source/drain resistances. Since junction depths are shallower for CMOS 5S than for the DRAM-based CMOS 5L process, the thickness of silicon consumed in the salicidation reaction had to be lowered to prevent unacceptable junction leakage. This requirement necessitated the use of thinner sputtered titanium layers. Thinner titanium silicide layers, however, are subject to resistance anomalies due to agglomeration and incomplete C49-to-C54 phase transformation [9]. These anomalous sheet resistances were reduced for CMOS 5S through optimization of the RTP and chemical stripping steps.

• *CMOS 5X: 2.5-V high-performance, low-power logic*

To provide IBM with an enhanced-performance, low-power version of 0.5-μm logic, a new 2.5-V offering was developed. This technology offers the first 2.5-V device design point in the industry. This version, called CMOS 5X, differs from CMOS 5S primarily in the junction structure, again driven by the need for increased MOSFET performance. Nominal improvements in performance of 50–60% over that of CMOS 5L are achieved with 0.25-μm effective channel lengths.

Dual-workfunction silicided polysilicon gate electrodes are used as in CMOS 5S; however, the n-MOSFET gate and diffusions are doped with arsenic to maintain the shallow source/drain junction profiles necessary for enhanced performance and low leakage current. This creates the added constraint of obtaining sufficient dopant to minimize polysilicon gate depletion, yet still provide for silicide formation over the heavily doped arsenic source/drain regions. With the appropriate choice of annealing time and temperature, the depletion is limited to 10%. This has resulted in an equivalent gate oxide thickness of 7.7 nm from a 7.0-nm as-grown process.

Device channel lengths of 0.25 μm are obtained by printing images at approximately 0.4 μm. The DUV lithography, proven at half-micron image sizes in prior technologies, was extended to these sizes with excellent channel-length control. A 0.5-NA (numerical aperture) deep-UV (245-nm) step-and-scan tool, employing an IBM negative-tone resist system, was optimized for tight channel-length control.

With operating voltages reduced to 2.5 V, considerable simplification in the junction structure is possible. Single-species, single-implant junctions (non-LDD) are incorporated to reduce mask count and process complexity. The n-MOSFET junctions are formed with arsenic; the p-MOSFET uses boron. Both are implanted after a 56-nm nitride/oxide composite spacer to control gate overlap of the junction region. Dopant activation occurs with 1050°C/60-s and 1000°C/5-s RTAs for the n-MOSFET and p-MOSFET, respectively. This sequence affords compromise between gate depletion and junction depth while protecting against boron penetration of the p-MOSFET gate oxide. The lower-voltage operating point provides relief from hot-electron degradation, allowing reliable effective MOSFET channel lengths down to 0.17 μm.

Table 2 compares the significant parameters from the three half-micron logic technologies.

Local Interconnects

Reduced SRAM cell size and high-performance logic circuits necessitate the use of borderless local interconnects [10]. The IBM approach for this feature is the use of damascene tungsten wiring [5]. To build local wiring using this technique, trenches are first etched into the passivating phosphorus silicate glass (PSG) layer, penetrating to contact desired polysilicon gate and diffusion regions. If this etch penetrates past the active diffusion regions, down the isolation sidewalls, the wiring metal will contact low-doped well regions beneath the diffusion and high leakage will result.

The technique employed by CMOS 5S and CMOS 5X to minimize over-etch in these selective regions is to employ a PSG etch which is highly sensitive to an underlying silicon nitride etch-stop layer. Following the PSG etch, the nitride is removed from the bottoms of the contact holes by using a selective nitride etch. This approach uses commonly available films and tooling. After formation of the trenches where the wiring is to go, tungsten is deposited on the wafer and removed via planarization from atop the PSG. A fully processed CMOS 5X damascene local interconnect is depicted in the SRAM cell of **Figure 5**. Chemical-mechanical polishing is utilized for both dielectric and metal planarization. Contact studs from the local tungsten interconnect to the first level of aluminum wiring are fabricated by a similar process [3]. The global planarity of the local interconnect with five levels of metal is shown in **Figure 6**.

Integrating a damascene-tungsten local interconnect into a shallow-junction/trench-isolation technology requires the optimization of the PSG-to-nitride etch selectivity, the nitride etch-stop thickness, and the junction depth in order to prevent a mixed Schottky/p–n junction behavior. **Figure 7** illustrates the inverse relationship between selectivity and etch-stop thickness. Also shown is the dramatic reduction in selectivity requirements due to planarization. The nitride thickness is fundamentally determined by the selectivities generated by both the oxide and the nitride RIE (reactive-ion etch) chemistries. Reduction of the isolation oxide loss is accomplished by thinning the nitride etch-stop thickness and increasing the PSG etch selectivity and/or increasing the nitride etch selectivity. The mixed Schottky/p–n junction behavior arises from recessing the isolation oxide and exposing the low junction-doping concentration ($<5 \times 10^{19}$ cm^{-3}) to the linear metallurgy. A low liner-metallurgy barrier height to n+ junctions increases the mixed Schottky/p–n junction leakage behavior, necessitating a deeper n+ junction (**Figure 8**). The n-channel device characteristics were essentially unchanged by increasing the junction depth.

Contacts and global wiring

The dense multilayer interconnects required for 0.5-μm logic designs are provided with a scaled version of the technology developed for an earlier 0.7-μm logic generation [4]. This extendable technology includes up to four levels of low-resistance wires with vertical via connections between levels. Sputter-deposited aluminum–copper clad with titanium is patterned and etched to form wires. Silicon dioxide insulators are deposited between levels using plasma-enhanced chemical vapor deposition (PECVD). The insulators are planarized with chemical-mechanical planarization (CMP). A damascene process is employed to fill vertical vias with tungsten, providing a nearly flat surface for each metal level.

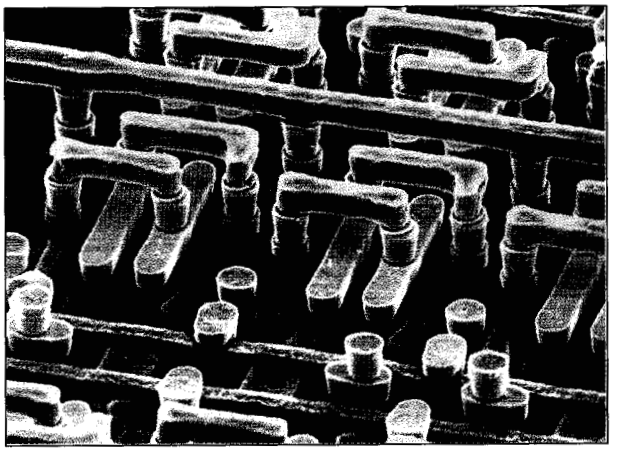


Figure 5

SEM of local interconnect and first aluminum wires in an SRAM cell.

Scaling the interconnects involved shrinking wiring pitches by about 30%. The pitch of the first wiring layer was reduced from 2.0 μm to 1.4 μm, and the width of the global wires was reduced from 2.4 μm to 1.8 μm. An additional level of global wires was added primarily to deal with the wiring demands of larger chips. The metal thicknesses were reduced by 30% (to 0.6 μm for M1 and 0.9 μm for M2–4) so that the aspect ratio of spaces between wires was not increased. The existing insulator deposition process, which is limited as to the kinds of spaces it can fill, could thus be used.

A low-resistance, relaxed-pitch last level of metal is offered in both the 0.7- and the 0.5-μm generations for power distribution and pad transfer. The insulator and via processing between the last true wiring level and this power distribution level was simplified in the 0.5-μm generation. The CMP-planarized insulator and tungsten-filled vias were replaced with a nonplanar deposited insulator and tapered vias. This much simpler process has a 40% lower manufacturing cost. SEM cross sections of five-level-metal test structures fabricated with a complete interconnect process are shown in Figure 6.

Precision resistor

An ion-implanted and diffused precision resistor is a part of the CMOS 5S and CMOS 5X processes. This feature adds only mask and ion implantation steps to the process. Dose and energy were chosen to give a sheet resistance of 60 $\Omega/\square \pm 10\%$. Phosphorus is used as the implanted species. If the ion implantation is done early in the process (after sacrificial oxidation, but before the well implants), the thermal cycles inherent in the process are sufficient to drive in the dopant and provide the proper sheet

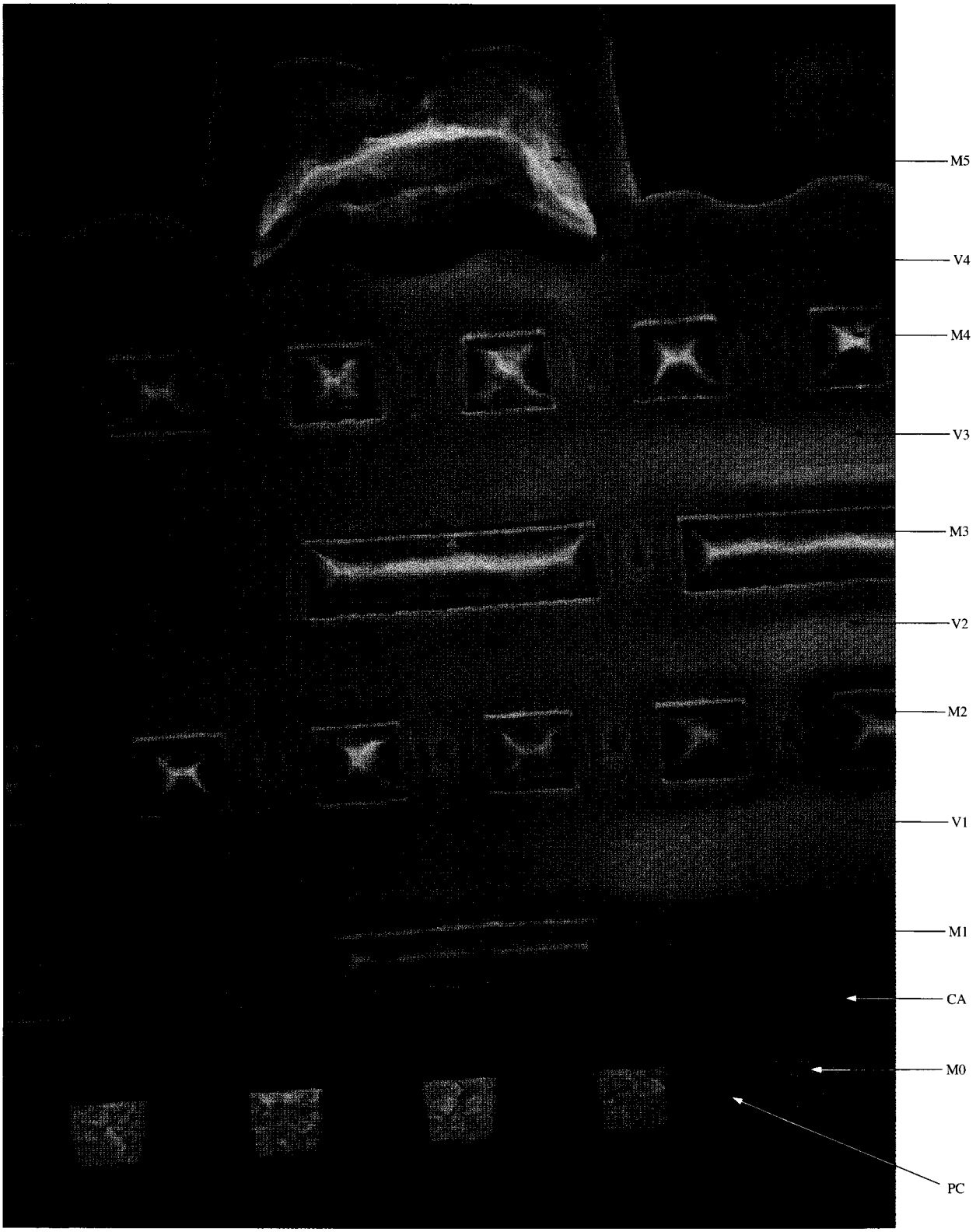


Figure 6

SEM of global planarity of five levels of metal with a local interconnect.

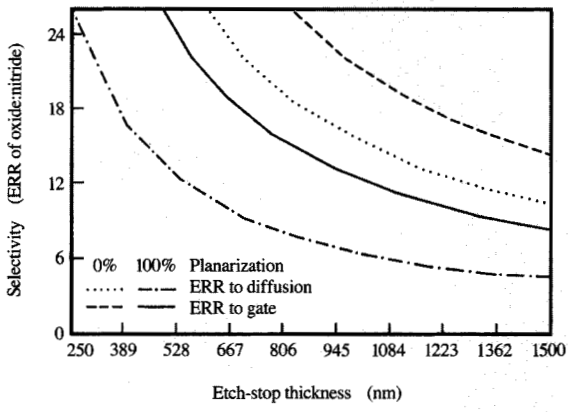


Figure 7

Inverse relationship of selectivity as a function of etch-stop thickness.

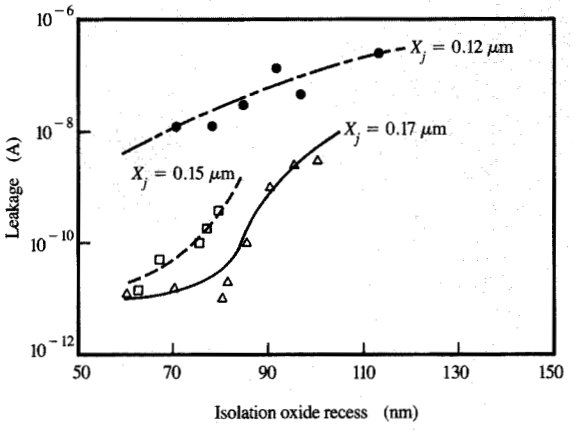


Figure 8

Sensitivity of n+ junction leakage to oxide recess and junction depth.

resistance. A further constraint on the dose and energy was to minimize the oxide grown over the heavily doped region. This is necessary to ensure that the contact region can be opened up later with the same etches used for the standard devices, to enable $TiSi_2$ formation.

The length of the resistor is controlled by a polysilicon plate which blocks the silicidation of the resistor area. Its width is determined by the silicon island defined by the

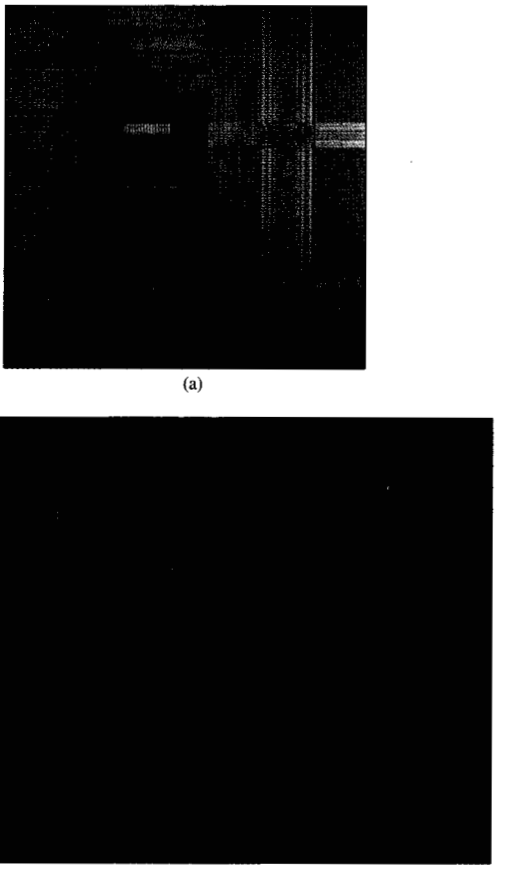


Figure 9

(a) CMOS 5X (scaled) version of microprocessor qualified with (b) 0.7-μm process.

active-region mask and thus is bounded by shallow-trench isolation. For high-value resistors, sets of small-value resistors are wired in series using the local interconnect. This allows changes in the resistance to be made later in the process, if required, by dropping one or more links.

The precision-resistor level is used to provide source terminations for drivers, clock terminations for clock signals, high-value bleeder resistors, and resistors for devices that protect against ESD (electrostatic discharge).

Design migration

For CMOS 5L, CMOS 5S, and CMOS 5X, each technology offers unique sets of advantages. At the same time, it is recognized that some users will want to migrate designs, in whole or in part, from one process to another. Ground-rule differences from one to another are, for the most part, minor, except for the availability of the local interconnect feature for CMOS 5S and CMOS 5X. This ground-rule commonality has been demonstrated by

Table 3 Process technology differences for three half-micron logic programs. (Table 2 compares device parameters.)

	Gate conductor	*n+ junction structure*	*p+ junction structure*	*Local interconnect*	*Precision resistor*
CMOS 5L	WSi_2 polycide	Phos/As LDD	Boron LDD	No	No
CMOS 5S	$TiSi_2$ salicide	Phos LDD	Boron LDD	Optional	Optional
CMOS 5X	$TiSi_2$ salicide	As abrupt	Boron abrupt	Yes	Optional

fabricating products in more than one technology. Blind switching of technologies is not always likely to be possible, however, since timing issues and overall circuit function are questions addressed by a larger combination of issues than just ground rules.

Migration from earlier technologies sharing a common feature set also has been demonstrated. The first qualification vehicle for CMOS 5L was a compressed early version of the IBM POWER RISC microprocessor; the design was originally laid out for a proprietary 1.25-μm CMOS process. For CMOS 5X, the first product demonstration vehicle was a 100/120-MHz version of the 601 RISC microprocessor built initially using a 0.7-μm technology. In this last instance, speed increased approximately 50%, while both die size and power consumption dropped (**Figure 9**). Similar process philosophies guaranteed design adaptability with a minimum redesign effort.

Summary

Three 0.5-μm CMOS logic technologies have been discussed. These three programs share extendable common process features: p− on p+ epitaxial substrates, shallow-trench isolation, $TiSi_2$-salicided diffusions, and dense fully planarized multilevel aluminum-based metallization processes. Process differences, summarized in **Table 3**, are driven by differing sets of device goals, power supply choices, schedule constraints, feature requirements, and performance demands for differing applications. Pre-existing technology elements have been adapted, improved, or supplemented in order to provide the highest possible performance options while maintaining optimal design migratability both from older technologies and from within the 0.5-μm family of CMOS logic offerings.

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Received June 7, 1994; accepted for publication November 28, 1994

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