A low-noise TTL-compatible CMOS off-chip driver circuit

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Low-noise TTL-compatible off-chip driver (OCD) circuits are very important, especially for low-power electronics, but scaled-down CMOS technology requires a lower operating voltage of 3.3 V, while most applications require 5 V. The dual power-supply requirement makes the design of OCD challenging, first because pull-up devices, especially p-MOS devices, must be able to handle an off-chip voltage of 5.6 V, which is higher than an on-chip V_{DD} of 2.8 V, and second because pull-down devices should be able to discharge a capacitive load of 5.6 V while operating at a minimum on-chip V_{DD} of 2.8 V. This extreme difference in operating voltage makes the circuits susceptible to ringing and performance degradation due to hot-electron effects. In this paper, we describe a low-noise OCD which has been successfully used in IBM second-generation 4Mb low-power DRAM (LPDRAM) and in other products. For pull-ups, two stacked p-MOS devices with floating n-wells are used, but they are operated in different modes depending on the supply voltage. The pull-down devices are basically composed of two stages, one of which is in the diode configuration with its gate and drain shorted together during the pull-down. Detailed circuit designs to achieve low noise while meeting the performance requirements are described.

Introduction

As CMOS technology improves, the need for chips operating with dual power-supply voltages (3.3 and 5 V) has drastically increased, especially for low-power electronics. Scaled-down CMOS technology requires a lower operating voltage of 3.3 V or less, while most applications still remain at 5 V. This dual power-supply requirement makes the design of OCD challenging and difficult for both pull-up and pull-down devices. For pull-up devices, the biggest challenge is being able to remain tri-stated while their drains receive an off-chip voltage of 5.6 V, which is almost twice the worst-case on-chip V_{DD} of 2.8 V. The requirements on the pull-down devices are no less daunting, because they should be able to discharge to ground a capacitive load charged to 5.6 V in an allowable time period determined by the chip performance requirements, while operating at a minimum on-chip V_{DD} of 2.8 V. These competing requirements and the extreme difference in operating voltage make the OCD highly susceptible to excessive ringing and performance degradation due to hot-electron effects, as is extensively documented in the literature.

In this paper, we describe a low-noise OCD which has been successfully used in the IBM second-generation 4Mb low-power DRAM and in other products with I/Os wider

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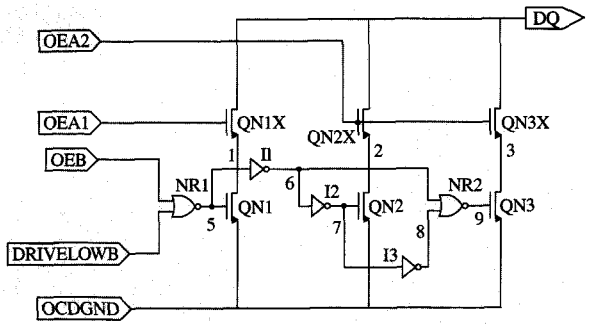

Figure 1

Schematic diagram of a conventional three-stage pull-down circuit, shown with control signals.

than the more traditional X1 or X4 I/Os. It operates with a nominal on-chip power supply of 3.3 V (worst-case, 2.8 V), while meeting the TTL interface requirements of a 5-V external bus. The pull-down devices are basically composed of two stages, one of which is a diode configuration, with its gate and drain shorted together during the pull-down. The other is a more conventional common-source configuration [1, 2]. Although the pull-down circuit has only two stages, compared to the more common three-stage implementation, the diode configuration used for the second stage is inherently more resistant during a pull-down to under- and over-shooting of the output due to ground bouncing. It is also more efficient in terms of area in pulling down a capacitive load charged to a voltage higher than the on-chip V_{DD}, because the gate is connected to the drain of the pull-down transistor to which the external voltage is applied. Consequently, the overdrive on the gate, especially during the initial stage of the pull-down, is larger than what would have been obtained if the gate were simply connected to the on-chip V_{DD}, as in the common-source configuration. The combination of these two factors substantially reduces the under- and over-shooting of the output node during a pull-down, as well as the bouncing of the on-chip ground node, while achieving the fast pull-down necessary to maintain the required access time of a chip.

For pull-ups, three stages, each of which is composed of two stacked p-MOS devices in floating n-wells, are activated in sequence, reducing power-supply bouncing and Ldi/dt much as the previously used circuit [3] would do. However, the previous circuit has severe limitations in operating with dual power-supply voltages, especially when on-chip voltage regulators are used to provide the on-chip V_{DD}. The new circuit is operated in different modes depending on the supply voltages, drastically reducing deleterious effects on the power supply and on-chip noise when the power supply is 5 V. It also has an improved control for the floating n-wells, which reduces the time period during which the n-wells float. This further enhances the latch-up resistance of the circuit.

Pull-down circuitry of low-noise off-chip driver

- *Conventional multistage pull-down circuit*

Figure 1 shows one of the widely used TTL-compatible n-MOS pull-down circuits. It is composed of three stages. The transistors QN1X, QN2X, and QN3X are activated when OEA1 and OEA2 become high. When DRIVELOWB and OEB are driven low, QN1, QN2, and QN3 are activated in sequence. The time delays between the activations of QN1 and QN2 and between those of QN2 and QN3 are determined respectively by I1 and I2 and by I3 and the NOR gate NR2. The device sizes are typically optimized for an expected capacitive load. Since the worst-case on-chip power supply is 2.8 V for a 3.3-V supply and the worst-case load is charged to 5.6 V, the pull-down device sizes are bigger than they would have been with a 5-V power supply, because the reduced overdrive on the gate requires a compensating increase in device size.

The effect of increased device size on the transient characteristic can be understood through the use of an equivalent circuit. A simplified equivalent circuit of this three-stage pull-down circuit is composed of the inductance of the bonding wiring and pad, the load and parasitic capacitances of the pull-down devices, and the resistance of the pull-down devices. For a given C and L, the resistance of the pull-down devices is smaller than its single-power-supply counterpart. As a result, the circuit, when operated with the dual power-supply voltages, has a higher oscillatory tendency for a smaller load, or a higher power-supply requirement with shorter-channel-length devices due to process variation.

- *Overview of low-noise pull-down circuitry*

In **Figures 2** and **3**, we show a new TTL-compatible pull-down circuit with much less under- and over-shooting than the previous circuits. In contrast to Figure 1, the pull-down devices are basically composed of two n-MOS devices, one of which is connected in the so-called diode configuration, with its gate and drain shorted together during the pull-down. The other is in the common-source configuration, as in Figure 1. Because of these combinations, the circuit is fully TTL-compatible, with better transient performance than the conventional circuit, as is shown later.

Another novel feature of the circuit is that both p-MOS and n-MOS devices are used for shorting the gate and

drain of the pull-down device. As a result, if the capacitive load is charged to a voltage higher than on-chip V_{DD}, the pull-down device in the diode configuration has a higher-than-V_{DD} voltage on its gate and a larger overdrive than would normally have been available on the chip. This gives an excellent pull-down characteristic when the capacitive load is charged to higher voltages.

Using both p-MOS and n-MOS devices in shorting the gate and drain of the pull-down device poses a problem when the OCD is tri-stated and the load is higher than the on-chip V_{DD}. A level-shifting circuit is used to meet the requirement.

• *Description of low-noise pull-down circuitry*

The new circuits are schematically shown in Figures 2 and 3. The only difference between Figures 2 and 3 is whether the n-MOS devices are stacked in order to reduce the hot-electron and oxide-reliability effects on the n-MOS devices. (For example, QN1A and QN1 in Figure 2 are stacked, but QN1 is used alone in Figure 3.) Whether or not the devices must be stacked depends on the application as well as on the specific technology used to implement the circuit. In the schematic, the node DQ is the output of the circuit and is connected to the external load. The circuit operation can be understood as follows, on the basis of Figure 2.

During standby (or in the high-Z state), OEB and DRIVELOWB are both high. OEA1 is low. Node 1, which is the output of NOR gate NR1, is low and QN1 is off. The inverter I4 inverts the signal at node 1 and keeps node 3 high. With nodes 1 and 3 low and high, respectively, the level shifter composed of QP1, QP2, QN5A, QN5, QN6A, and QN6 keeps node 4 low, turning QN2 and QN2A off. It also keeps QP1 on, which in turn keeps the gate of QP2 (node 8) at the same voltage as node DQ. QP2 is off, which isolates node 4 from node DQ. Thus, node 4 can be held low by the turned-on QN6A and QN6 while maintaining the high-Z state. Also note that QN5A and QN5 are off, and that QNP1 is on. Thus, node 8 is electrically connected only to node DQ and is properly tri-stated.

During pull-down, OEA1 goes high, turning QN1A on. As both OEB and DRIVELOWB change to low, node 1 rises to V_{DD} and node 3 discharges to ground. As node 1 rises, it turns on QN1, which starts to discharge node DQ toward ground. Also, QP1 and QP2 change their state from on and off to off and on, respectively. With QP2 now on, the gate of QN2A and its drain (node DQ) are shorted together in the diode configuration. Thus, node DQ is discharged through QN2A and QN2. Also, the low signal at node 3 further propagates through the inverter chain composed of I5, I6, and I7. Because of the odd number of inverters, the signal at node 3C is high and turns on QN4. With both QP2 and QN4 on, the gate and drain of QN2A stay shorted together, even though node DQ discharges to ground. Also, by delaying the turn-on of QN4, the potential hot-electron effect on QN4 is reduced because the charging of node 4 to the same voltage as node DQ is done primarily by QP2.

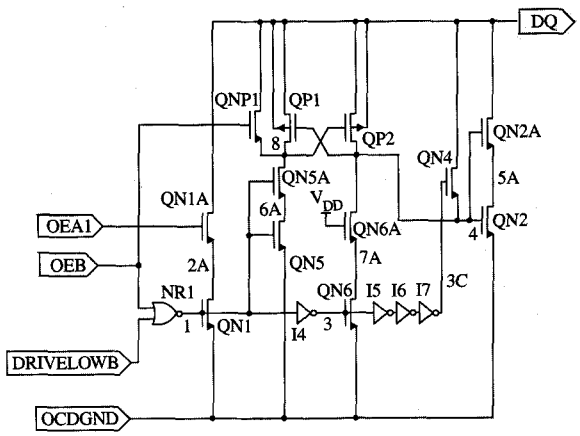

Figure 2

New pull-down circuit with stacked n-MOS devices for reducing hot-electron effects.

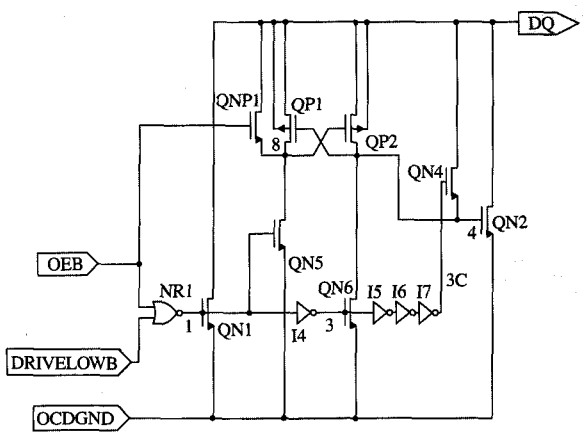

Figure 3

New pull-down circuit without stacked n-MOS devices.

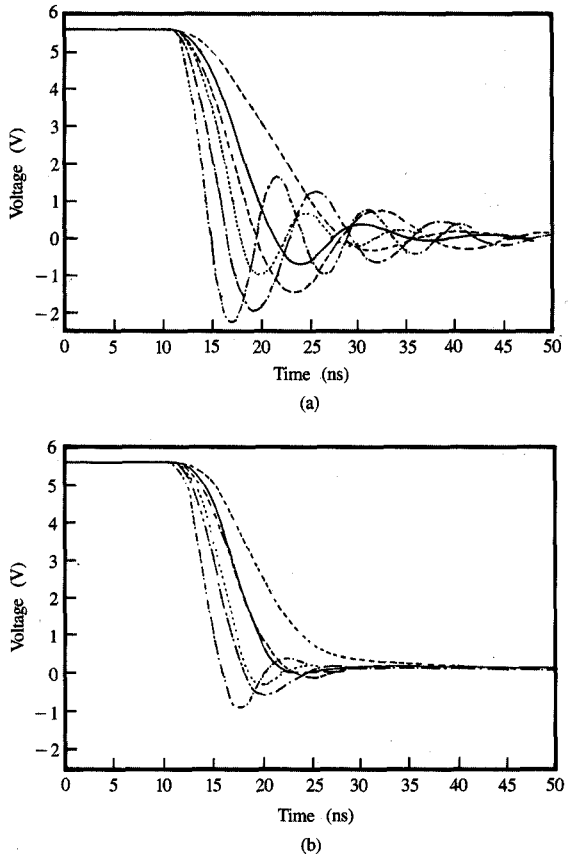

Figure 4

Pull-down waveforms for various load and operating conditions shown in Table 1: (a) conventional circuit; (b) new two-stage pull-down circuit. Improved circuit performance can easily be seen by comparing the envelopes of waveforms in (a) and (b).

Table 1 Transition times of the circuits in Figures 1 and 2 as a function of capacitive load and process. The transition times of the circuit in Figure 1 are longer for the fast circuit-operation conditions than for the slow circuit-operation conditions, which is counterintuitive. This is because of the larger ringing observed for the fast circuit-operation conditions, which takes longer to settle down to a voltage lower than 0.4 V.

Circuit	*100°C, 2.8-V V_{DD}, nominal process*			*22°C, 3.7-V V_{DD}, best process*		
	50 pF (ns)	*100 pF* (ns)	*200 pF* (ns)	*50 pF* (ns)	*100 pF* (ns)	*200 pF* (ns)
Figure 1	16.08	10.68	16.7	22.63	29.32	25.1
Figure 2	7.87	10.6	18.5	5.5	7.5	11.19

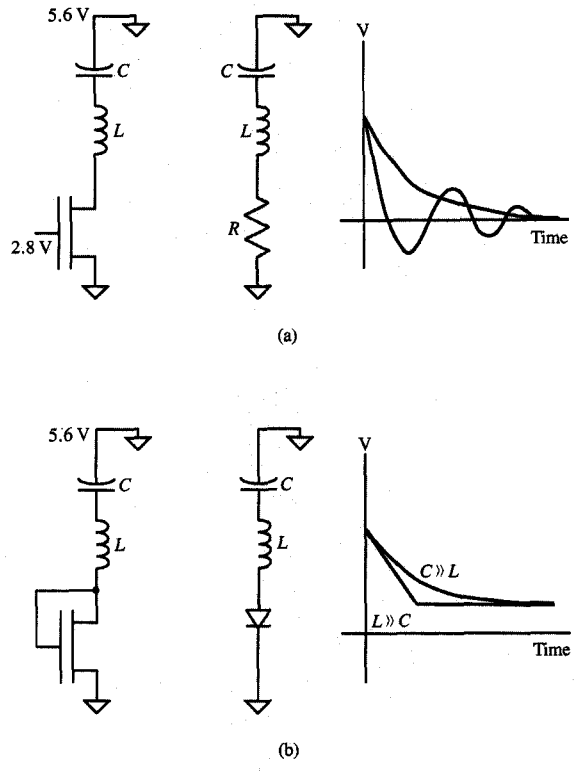

Figure 5

Simplified equivalent circuits of the pull-down circuit shown in (a) Figure 1 and (b) Figure 2.

- *Comparison of the two circuits*

Figure 4 shows the load waveforms of the conventional circuit shown in Figure 1 and the new circuit shown in Figure 2 for various load and process conditions. The conventional circuit has a tendency to oscillate if the load is small. For TTL compatibility, the transition time can be defined as the time between the activation of the pull-down circuit and the point at which the output becomes lower than 0.4 V. **Table 1** summarizes the comparison between the two designs, using a nominal capacitive load of 100 pF and a 0.6-μm CMOS technology. As can be seen in the table, a substantial improvement in the transition time is observed for almost of all the process and operating conditions for the new circuits.

The basic reason for improved performance is illustrated in **Figure 5**. A common-source n-MOS transistor pulling a capacitive load through an inductive package lead can be simulated as an *R-L-C* series circuit, as shown in Figure 5(a). Depending on the values of R, L, and C, the circuit will oscillate. Thus, as process and operating voltages

change, the transconductance of the n-MOS transistor, which is modeled by R, will change, and the circuit will often show an oscillatory tendency. If the load is discharged by an n-MOS in the diode configuration, the n-MOS transistor is always in saturation. Even though its waveform is still a function of L, C, and the transconductance of the n-MOS transistor, it lies between the two extreme cases ($L \gg C$ or $C \gg L$) shown in Figure 5(b) and does not exhibit any oscillatory tendency. In the actual implementation, the new circuit is composed of two stages, i.e., a common-source n-MOS and an n-MOS in the diode configuration for TTL compatibility. Thus, it shows some tendency to oscillate for extreme conditions, but far less than the conventional circuit because it has a common-source n-MOS transistor.

Pull-up circuitry of low-noise off-chip driver

• *Conventional multistage pull-up circuit using p-MOS devices in floating n-wells*

The pull-up circuitry of the TTL off-chip driver (OCD) which operates with the dual power-supply voltage has at least two challenging objectives: to meet the TTL requirements with both a 3.3-V and 5-V power supply, and to remain tri-stated even when it is driven by other 5-V chips. One way of achieving these objectives is to use the circuit shown in **Figure 6** [3], which has stacked p-MOS pull-up devices with floating n-wells [3, 4]. However, this circuit has severe limitations in operating with dual power-supply voltages.

On a chip operating with dual power-supply voltages, a voltage regulator is generally implemented so that most of the circuitry on the chip operates at the lower power-supply voltage. For example, for a dual power supply of 3.3 V and 5 V, the on-chip regulator will generate a V_{DD} of 3.3 V to 3.6 V if the external power supply is 5 V. The on-chip regulator is generally bypassed if the external power-supply voltage is 3.3 V. If we operate the circuit shown in Figure 6 with a 5-V external power supply without any modification, it would require a regulated V_{DD} (3.3 to 3.6 V) applied to node 28 in Figure 6. Applying a regulated V_{DD} to node 28 is very undesirable, because it would require a very large on-chip regulator to supply the large current needed to drive large external capacitive loads through QP1X and QP1. The other alternative would be applying 5 V to node 28 only, while operating the rest of the circuit from the regulated V_{DD}. For example, I1, NN1, and NR1 are operated from the regulated V_{DD}, but the source of QP1X, which is connected to node 28, is at 5 V. In this case, the circuit loses its high-Z state for a certain range of the output voltage between the ground and the power-supply voltage. More specifically, with 5 V applied to node 28, node B stays one threshold voltage drop ($|V_{TP}|$) below node 28. It is approximately 4.3 V, assuming a typical $|V_{TP}|$ of 0.7 V. If the output (data-out) is forced to approximately 4.0 V during the tri-state, transistor QP1 turns on because its gate is at 3.3 V but the source and drain are at 4 V or higher. Losing the high-Z state is not acceptable for TTL compatibility.

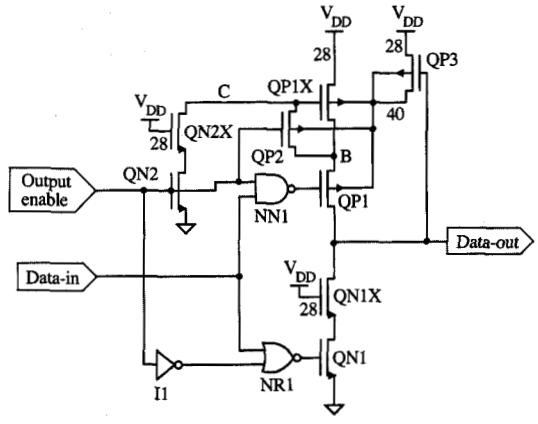

Figure 6

A CMOS off-chip driver circuit using p-MOS devices in floating n-wells [3].

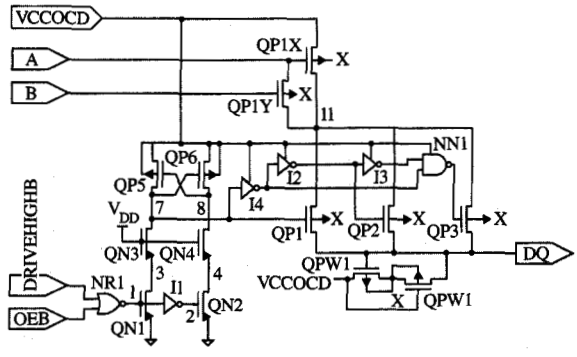

Figure 7

New pull-up circuit. The control circuitry is shown in Figure 8. Note that the p-MOS transistors in inverters I2, I3, and I4 are connected to VCCOCD, which is annotated by the extra port connections in their symbols.

• *Low-noise pull-up circuitry*

In **Figures 7** and **8**, we show a new OCD pull-up circuit with stacked p-MOS pull-up devices in the floating wells.

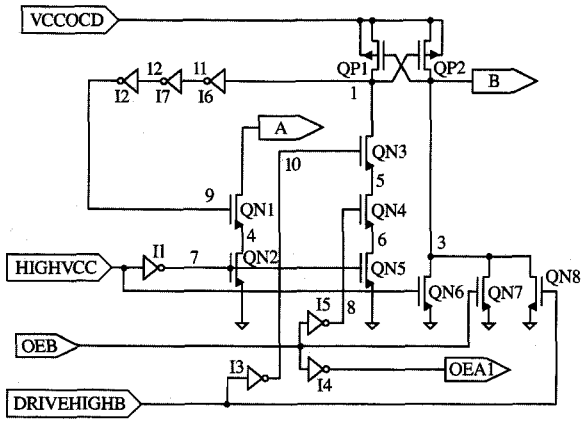

Figure 8

Control circuitry for new pull-up circuit.

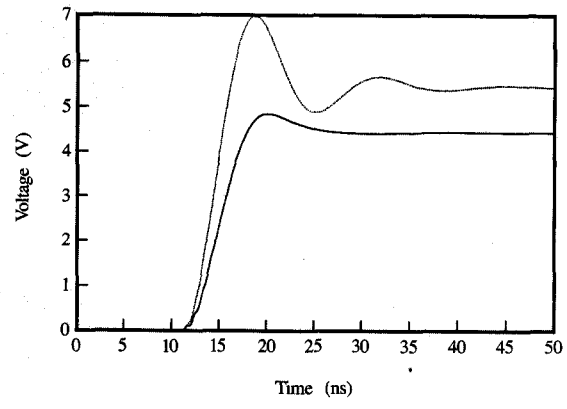

Figure 9

Waveforms of the output nodes during a pull-up. Solid line: new circuit; dotted line: circuit shown in Figure 6 [3]. Note the difference in the overshoot of the output node.

Figure 7 shows the pull-up circuit, which has three stages. Figure 8 shows the control circuit for the pull-up circuit shown in Figure 7. In contrast to Figure 6, a level shifter is used to control the gates of the bottom p-MOS devices of the p-MOS stacks. Also, in 5-V mode, the top p-MOS device has its gate and drain connected together. Consequently, the new circuit requires no voltage regulator while maintaining TTL compatibility. Having the gate and drain of the top p-MOS device shorted together in the 5-V mode limits the maximum pull-up voltage to one threshold voltage drop ($|V_{TP}|$) below the power-supply voltage. This results in a lower power dissipation and less ringing in the output waveform, as is shown later.

A more detailed description of circuit operation is as follows.

During standby (or in high-Z state), when OEB and DRIVEHIGHB are high, nodes 1 and B in Figure 8 are high and low, respectively. The high signal at node 1 is inverted by the three inverters I6, I7, and I2 to a low signal, which is applied to the gate of QN1. It turns QN1 off and node A floats.

In Figure 7, a low condition at node B turns QP1Y on, which causes the drain and the gate of QP1X to be shorted together. With DRIVEHIGHB and OEB high, node 7 is high and keeps QP1 off. The high condition at node 7 is also applied to QP2 and QP3 through the inverters I4, I2, and I3 and NAND gate NN1, keeping QP2 and QP3 off.

Note that the gates of QP1, QP2, and QP3 in Figure 7 are always at the same voltage as VCCOCD, which is supplied to the source of QP1X. Thus, it does not lose its high-*Z* state for a certain intermediate voltage, as did the previous circuit in Figure 6 in the 5-V mode.

During pull-up, in Figure 7, OEB and DRIVEHIGHB become low. Then, node 7 discharges to ground, turning on QP1 first. QP2 and QP3 are turned on in sequence by the inverters I4, I2, and I3 and the NAND gate NN1. The output node DQ is pulled up to the voltage at node 11. The voltage at node 11 is at V_{CC} in the 3.3-V mode or at $V_{CC} - |V_{TP}|$ in the 5-V mode. Control of node 11 is achieved by controlling QP1X and QP1Y. In the 3.3-V mode, HIGHVCC in Figure 8 is low. When DRIVEHIGHB and OEB become low, node A discharges to the ground, turning on QP1X. Also, node B rises to VCCOCD, turning QP1Y off. Thus, node 11 can go as high as V_{CC}. In the 5-V mode, HIGHVCC in Figure 8 is high. Even if both DRIVEHIGHB and OEB become low, node B stays low and node A continues to float. As a result, QP1Y stays on. The gate and drain of QP1X are connected through the turned-on QP1Y, so the voltage at node 11 stays at $V_{CC} - |V_{TP}|$ in the 5-V mode.

The advantage of limiting the DQ node to $V_{CC} - |V_{TP}|$ in the 5-V mode can easily be seen in **Figure 9**. The switching signal of the circuit in Figure 6, shown as a dotted line, has a big overshoot in its output waveform which can go as high as 7 V. This can be very detrimental to the receivers. The new circuit has a small overshoot and would not pose any problem to the receivers.

Implementation

The OCD circuit described has been designed and fabricated as the output driver macro of an IBM second-generation (4Mb) low-power DRAM (LPDRAM) and in

other products, using a 0.6-μm CMOS technology. The plot of the OCD is shown in **Figure 10**. Having been analyzed, characterized, and improved according to an IBM DRAM product qualification procedure, the circuit has remained essentially the same, with the exception of device size adjustment and the addition of another common-source pull-down stage in the pull-down circuitry for 16-I/O organization.

The true measure of how good an OCD is, in our opinion, is obtainable only from a comparison of the yield of two products based on the same technology, with similar design objectives, package constraints, and system requirements. No test-site implementation will reflect the actual operating conditions and other constraints as faithfully as the actual chip. The LPDRAM using the new OCD has passed internal qualification and is in production. In spite of a shorter period in production, its yield is higher with a longer retention time than that of a remapped version of the first-generation IBM 4Mb DRAM based on the same technology as the LPDRAM. Although we cannot attribute all of the reduction in noise and improvement in yield to the new OCD design, there is no doubt that it is one of the key contributors.

Summary

We have successfully designed, implemented, and tested a new low-noise, TTL-compatible, dual power-supply off-chip driver (OCD) for the IBM second-generation 4Mb low-power DRAM and other products. It has three stages of two-high stacked p-MOS devices in floating n-wells for pull-ups. They are operated in different modes, depending on the supply voltage. For pull-down, the circuit is basically composed of two stages, one of which is in the diode configuration with its gate and drain shorted together during the pull-down. The inherently stable nature of the diode configuration reduces the ringing of the output node due to process variations and changes in the operating conditions. This reduction in noise in both pull-up and pull-down has proved to be the one of the key contributors to the successful design of LPDRAM.

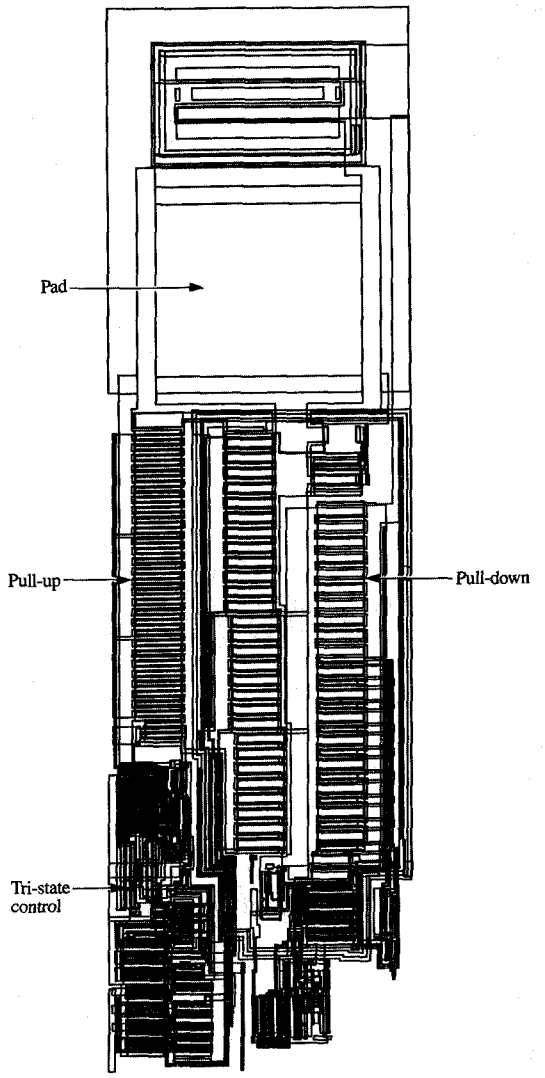

Figure 10

Plot of the OCD circuit shown in Figures 2, 7, and 8. The actual size can easily be deduced from the pad size, which is 110 × 110 μm.

Acknowledgments

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