

Overview of gate linewidth control in the manufacture of CMOS logic chips

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This paper is an overview of the methods used at the Burlington facility of the IBM Microelectronics Division to improve channel-length tolerance control in the manufacture of CMOS logic chips. We cover aspects of 1) the impact of channel-length control on chip performance, yield, and reliability; 2) our use of an electrical linewidth monitor which permits high-volume, accurate measurements to quantify polysilicon gate linewidth variability and its improvements; and 3) our efforts to reduce photolithographic and etching contributions to the linewidth variability.

Introduction

Dimensional control of MOSFET channel length is critical for manufacturing advanced CMOS logic chips. Scaling MOSFET devices improves performance by reducing chip dimensions (decreasing wiring delays) and by shrinking MOSFET gate lengths (increasing the current available to drive parasitic capacitances). In addition, as feature sizes shrink, more function can be added to a chip, reducing the need for slower off-chip communication. However, as performance improves, circuit-to-circuit timing and

matching issues become more critical, and as more chip functions are demanded, as in advanced microprocessors, physically larger chips must be produced. The matching issues and larger chip sizes increase the burden on manufacturing to continually reduce the variability of gate linewidth (hereafter frequently referred to simply as linewidth) over larger chip areas. **Figure 1** illustrates the importance of linewidth control; it schematically shows chip yield as a function of channel length, with yield loss due to poor performance at long-channel-length values, and due to leakage at short-channel-length values.

Although there are many sources of channel-length variability (e.g., the mask, exposure system, image processing, etching, sidewall spacer processing, source and drain dopant implantations, thermal cycles, and measurements), we concentrate in this paper on the contribution by the variability of the polysilicon gate linewidth—currently the dominant source of channel-length variability. The linewidth variability can be characterized by either electrical testing or scanning electron microscopy (SEM) measurements. We cover effects of channel-length variability on circuit timing, standby power, and MOSFET wear-out, and review our efforts on reducing linewidth variability, including those

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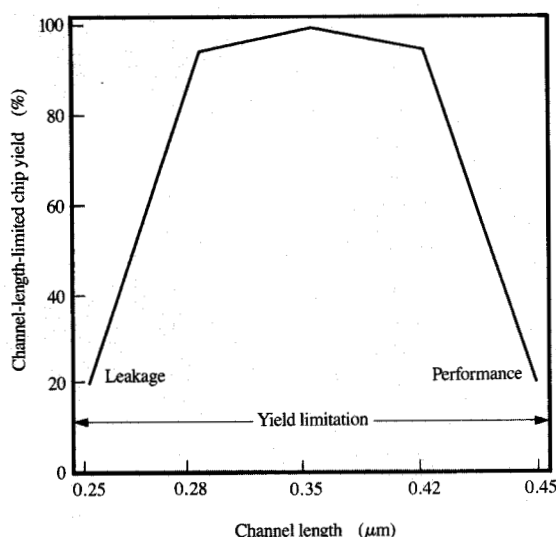


Figure 1

Schematic diagram of channel-length-limited chip yield as a function of channel length. Channel-length control must be tight enough to avoid yield degradation at either end of the channel-length spectrum. Reproduced from [16], with permission.

on linewidth measurements, analysis methods, and photolithographic and etching improvements.

For a chip to be functional, all of its MOSFETs must have channel lengths within a specified distribution. This requirement focuses attention on quantifying the parameters that drive channel-length variations within a chip, within a wafer, and lot-to-lot in a manufacturing line. The quantification of the control forces an underlying understanding of the random and systematic components driven by the fabrication processes on a microscopic and macroscopic level.

Components and chip impact of channel-length variations

Channel-length control is divided into two major components: chip-mean variation and across-chip linewidth variation (ACLV). Chip-mean variation consists of the root mean square of lot-to-lot, wafer-to-wafer, and within-wafer components, and results from statistical and systematic variations in manufacturing. For example, temporal variations in a manufacturing line introduce lot-to-lot variations; variations in a single-wafer lithography development tool produce wafer-to-wafer variations; systematic radial variations in a single-wafer etching tool cause a within-wafer effect. The ACLV is usually driven by systematic photolithographic and etching contributions.

The spacing between adjacent gate lines, for example, can cause a significant local variation in linewidth, which adds to the ACLV. Other effects develop over longer distances, of the order of a millimeter, and may be caused by mask variations, lens distortions or intensity variations in the photolithography equipment, or variations in etching loading. The boundary between within-wafer variability and within-chip variability is obviously determined by chip size; thus, as chip sizes increase, systematic within-wafer effects begin to have a significant impact on the ACLV. Partitioning the variability into chip-mean and across-chip components provides a convenient way to prioritize efforts to improve the variability. Wherever a value is presented in this paper for the above parameters, it will refer to their 3σ levels.

Of greater significance is that chip performance requires treating chip-mean and across-chip linewidth variations independently. Channel length is the largest contributor to variations of MOSFET performance, off-current (through short-channel effects on threshold voltage), and channel hot-electron wear-out. Chip-mean variations limit manufacturing yield and broaden the speed distribution for a given chip; the impact of the ACLV is more subtle. Controlling the across-chip linewidth for MOSFET gates is important for VLSI circuit behavior in four ways: circuit functionality, critical matching of timings between circuit paths, standby power at the fast end of the process window, and MOSFET wear-out.

Functionality for analog and analog-like circuits, such as current mirrors or sense amplifiers [1, 2], is directly limited by ACLV. If the matching between the MOSFETs is inadequate (the across-chip variability is too large), these analog circuits will fail. The risk of failure can be reduced by avoiding minimum-channel-length MOSFETs, but this approach will lower circuit speed. For memory sense amplifiers, more time may be required to develop an adequate signal to overcome the anticipated worst-case MOSFET mismatch, thus degrading chip performance.

Critical timings within a chip may also cause functionality failures. Various signal paths within VLSI chips frequently must arrive at a common circuit point (usually a latch) within a prescribed time window to ensure functionality. Circuit designers must intentionally slow the circuit to account for timing variations between paths due to imperfect channel-length control. Thus, the ACLV requires additional time to wait for (possibly) slow signals, and results in a chip performance degradation [3]. To demonstrate the ACLV effects, CMOS circuit performance was estimated using the familiar scaling law that speed increases inversely as channel length decreases. **Figure 2** shows an estimate of CMOS circuit performance vs. channel length for scaled ACLV and ACLV fixed at $0.1 \mu\text{m}$. Because circuit delays must be retimed to allow channel lengths up to $0.1 \mu\text{m}$ longer than nominal, circuit

performance increases inversely with the sum of the channel length and the $0.1\text{-}\mu\text{m}$ ACLV. (The estimate assumes $0.1\text{-}\mu\text{m}$ ACLV for both scaled and fixed ACLV at the $1.0\text{-}\mu\text{m}$ channel length.) At the shortest channel lengths, aggressively reducing the ACLV clearly results in faster circuit performance.

The chip standby current may exceed specifications because of linewidth variability, thus reducing test yields. The standby current, caused by subthreshold leakage from minimum-channel-length MOSFETs on a chip, can become significant if the fabrication process produces chips having channel lengths near the shortest allowed values; short-channel effects lower threshold voltages with decreasing channel length, and subthreshold currents increase exponentially with decreasing threshold voltage [4]. A naive estimate of this power could be given by multiplying the number of MOSFETs on a chip by the average subthreshold current per MOSFET. This simple estimate is a poor lower bound, because the exponential growth rate of subthreshold current with channel length results in significant weighting of the highest currents (shortest channel lengths). **Figure 3** illustrates the standby-current-limited yield for various ACLV levels. For a given circuit performance, represented by inverter delay, poorer ACLV results in lower yield; conversely, more tightly controlled ACLV allows improved circuit performance because of the resulting broadened yield window.

Guard-banding against field reliability failures is another significant concern for ACLV control. Because of channel hot-electron effects, n-type MOSFET (and, in some circumstances, p-type MOSFET) characteristics degrade with use. In essence, high electric fields generated at the drain edge of very short MOSFETs cause injection of electrons (or holes) with sufficient energy into the MOSFET gate oxide. These carriers damage the sensitive interface at the conduction channel, leading to device wear-out. Because this mechanism is highly sensitive to channel length [5], care must be taken to ensure that chips containing MOSFETs with unacceptably short channels are not delivered to customers. Relating in-line test structures to the wear-out behavior of the chip poses a significant challenge, because the chip may contain MOSFETs with channel lengths varying by as much as the ACLV from that of the test structures.

Because the ACLV is the random variation in channel length within each chip, one may be tempted to average it with the other variations in channel length when calculating the manufacturing latitude; this is a misleading assessment. For functional and reliable chips, all MOSFETs on all chips delivered to customers must conform to required specifications; and, because every chip carries with it its ACLV, it is clear that the manufacturing tolerance is the sum of the ACLV and the remaining linewidth variation.

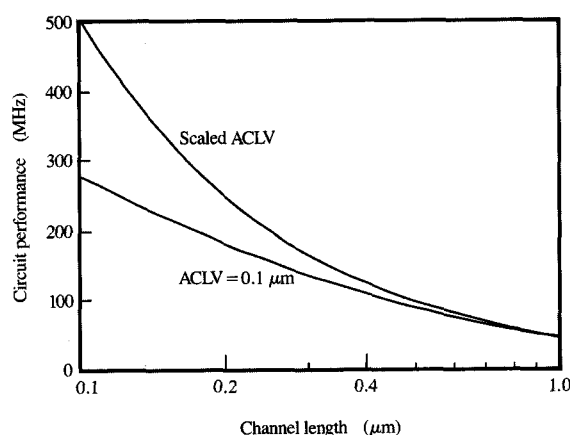


Figure 2

Illustrative estimate of circuit performance as a function of channel length. If the across-chip linewidth variation (ACLV) is not scaled down with the channel length, performance is significantly reduced.

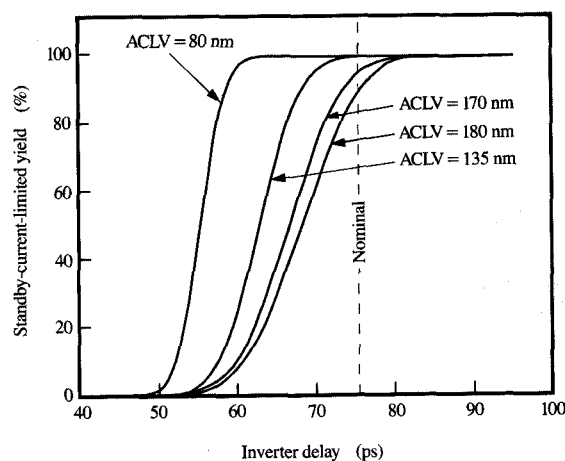


Figure 3

Illustrative standby-current-limited yield as a function of inverter delay, or, effectively, channel length. As the ACLV degrades, the yield window tightens.

Dimensional measurement

Because the ACLV effects become increasingly significant as device sizes are reduced, monitoring only the critical dimension (CD) sites in the scribe region between active

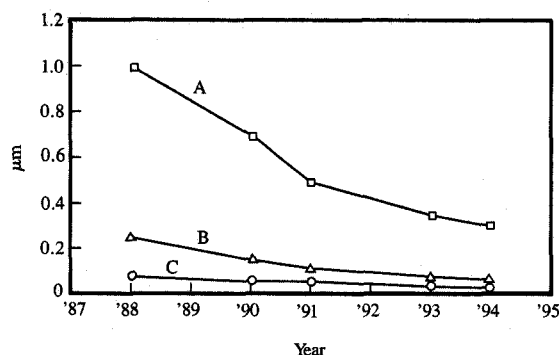


Figure 4

History of gate conductor linewidth and associated channel-length control: Curve A, nominal gate conductor linewidth; Curve B, specified overall channel-length variation; Curve C, specified ACLV.

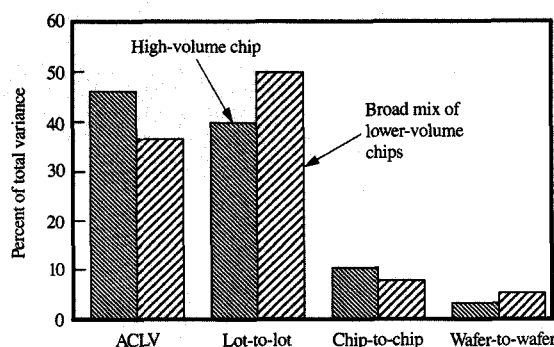


Figure 5

Typical components of linewidth variation. For the high-volume chip, the ACLV is the largest component. For a broad mix of lower-volume chips, the dominant component is the lot-to-lot variability.

chips provides insufficient detail on the total linewidth variation. The primary sources of gate-dimensional variance must be understood in order to continue the improvement in channel-length control needed to facilitate MOSFET technology advances. The history of the gate conductor linewidth and associated channel-length control is shown in **Figure 4**; nominal linewidth has shrunk by a factor of 4 in six years, with a comparable decrease in the

channel-length tolerances. We expect further linewidth reductions to continue at an accelerating pace to meet the demands of future high-speed chips.

To quantify process capability and characterize process improvements, a method is needed to obtain many CD measurements within each chip. Optical measurement capability does not have adequate precision, and the scanning electron metrology available when we began this work lacked the throughput to routinely characterize the variances. Therefore, conventional four-point probe resistor testing is used to measure polysilicon linewidths [6], and electrical linewidth measurement structures are designed to quantify the known sources of process variability: nested and isolated lines to investigate line proximity effects; lines in wide and narrow regions of local oxidation patterns to uncover topography effects; lines in both *x* and *y* axes to determine orientation effects; and lines placed at different sites to quantify influences of the mask and the exposure-tool lens used for patterning. The measured lines are at minimum design dimensions, and are made long enough to obtain accurate measurements. Because polysilicon resistance uniformity is key to the precision of these monitors, each measurement site contains a calibration resistor to determine localized polysilicon resistance variation. Wafers are tested directly after polysilicon gate etching and require approximately six minutes per wafer; measurement feedback can typically be provided within 24 hours. The measurement precision is within 3 nm.

To obtain electrical linewidth measurements, a polysilicon line must be conductive, its conductivity must be locally uniform, its associated gate structure must be electrically probable soon after processing (e.g., it must not have an insulating cap layer), and its cross section must be assumed to be rectangular. The gate conductors used in our CMOS chip families generally meet these conditions. If an oxide cap layer is present over the etched gate conductor, electrical testing is delayed until after the formation of contact holes and metallization. A greater reliance is then placed on physical SEM measurements, reducing the precision and volume of data.

We analyze our data according to our process unit size: lot, wafer, and chip. In addition, across-chip linewidth variation (ACLV) is monitored to determine the systematic components from line proximity effects, local oxidation topography, and chip field extremes. This ranking of error components is effective for monitoring progress and prioritizing improvement efforts. Typical components are shown in **Figure 5**; a distinct difference is seen when comparing the performance of a high-volume chip with a broad mix of lower-volume logic chips. Manufacturing a high-volume chip requires processing many lots of the same type; fabricating a broad mix of lower-volume logic chips requires processing many dissimilar lots.

The high-volume chip therefore displays better lot-to-lot performance, because statistical process control techniques can be used to minimize lot variability; the ACLV component is nearly half of the total linewidth variance. For the broad mix of lower-volume chips, the lot-to-lot variability is the most significant component; the influence of the ACLV on the total linewidth tolerance is diminished by the larger lot-to-lot variability.

Photolithographic effects

Initially, manufacturing chips with submicron gate lengths presented an appreciable challenge to the resolution capabilities of optical photolithography. Our capability was limited to 1.2 μm [the resolution limit of the 0.28 numerical aperture (NA) G-line (436-nm) steppers in use]. At first, the image size capability was extended by using a sidewall spacer on a mandrel as an imaging medium to transfer subresolution gate images to the polysilicon gate layer [7]. Although the process could be used to create subresolution gate images, it was deemed too complex for manufacturing and was replaced with a multilayer resist (MLR) process. In the MLR process, a polysilicon gate layer is patterned using the lowest of three layers: a well-hardened photoresist layer, an overlying oxide barrier layer, and an upper photoresist layer [8–10]. Although the MLR process was used temporarily, defects and difficulties in controlling dimensional biases during the sequential reactive ion etching (RIE) steps became serious manufacturability issues; the method also did not provide image-pitch scaling or a path to higher-density devices.

Improving chip performance and density has been made possible by scaling the numerical aperture and exposure wavelength of the lithographic system [6, 11, 12]. I-line (365-nm) steppers with NA values of 0.35 to 0.55 are used to produce chips containing gate structures of 0.45 to 0.80 μm , and remain a workhorse of submicron lithography. DUV (240–250-nm) processes are currently used to manufacture chips with sub-half-micron gate lengths. These systems have extended wet-development photoresist technology to current applications without resorting to more expensive RIE processing.

For I-line lithographic systems used in 0.5- μm to 0.8- μm technologies, thin-film interference effects introduce significant variability. The thin-film interference effects from photoresist thickness changes over local oxidation topography are minimized by sputter-depositing an antireflective titanium nitride layer onto the wafer substrates prior to photoresist application [13–15]. The effect of the antireflective coating (ARC) is illustrated in **Figure 6**; the ARC layer reduces the local linewidth variability from 300 nm to less than 50 nm by reducing the polysilicon reflectivity from 28% to 13%. For a 1- μm -thick I-line photoresist film with a 365-nm exposure wavelength, a 70-nm change in photoresist thickness causes a maximum-

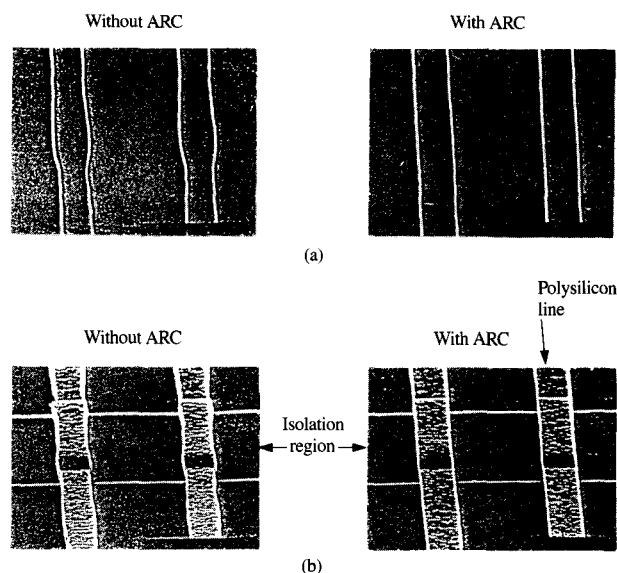


Figure 6

Illustrative effects of a sputter-deposited TiN antireflection coating (ARC) on photoresist-coated and polysilicon lines crossing over an isolation region containing 130-nm-thick edge steps, (a) before etching and (b) after etching and photoresist removal. The linewidth change resulting from thin-film interference effects is nearly eliminated with the use of the ARC.

to-minimum oscillation in reflectivity. Because the local oxidation isolation introduces a 130-nm topography range and the photoresist is nearly self-leveling when applied over this topography, there exists no optimum photoresist-coating thickness to suppress thin-film interference effects.

Once topography issues are addressed by using an ARC layer, other significant sources of ACLV in the manufacturing process can be uncovered. Some exposure tools are incapable of meeting ACLV requirements because of deviations in lens-field focus flatness, focus-system stability, and wafer-chuck flatness. Some of the deviations can subsequently be corrected by implementing more stringent tool-monitoring procedures and improving system design; however, by electrically characterizing ACLV performance, a reduced set of superior-performance tools can be identified for processing the critical gate conductor module. These superior tools are further optimized for the gate conductor layer by centering focus at the midpoint of the photoresist thickness. The electrical linewidth monitor also helps to identify sources of wafer-to-wafer linewidth variation. For example, variation between two separate developer modules incorporated within a single developer tool causes a bimodal wafer-to-wafer linewidth distribution.

Extension of our lithographic capability has continued by migrating to shorter-wavelength exposure systems.

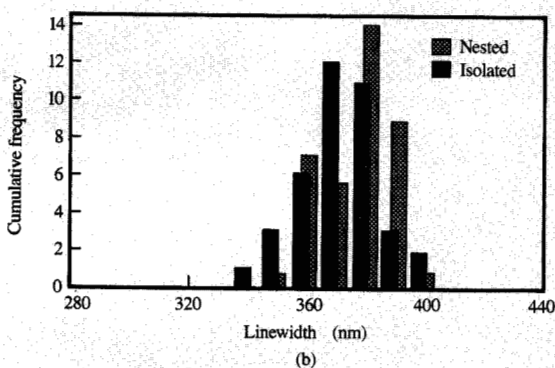
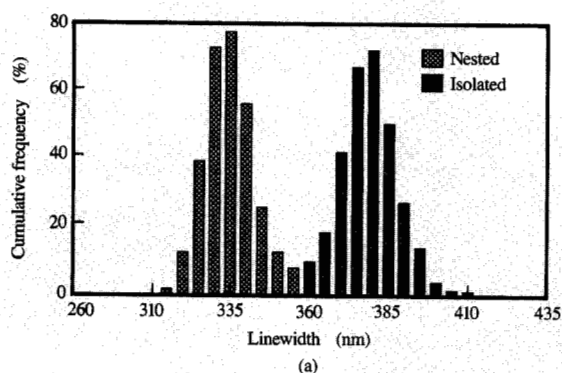


Figure 7

Illustrative linewidth distribution using a DUV lithography system with positive- and negative-tone photoresists: (a) use of a positive-tone photoresist results in a bimodal distribution with isolated images 30 nm larger than nested images; (b) use of a negative-tone photoresist results in an almost single distribution, with nested lines slightly larger than the isolated lines. Reproduced from [16], with permission.

After migrating from G-line (436 nm) to I-line (365 nm) exposure systems, DUV (240–250 nm) exposure is currently being used to produce sub-half-micron logic devices [16]. To improve the isolated-to-nested linewidth offset, we implemented use of a negative-tone photoresist for the gate conductor mask level [17] in conjunction with this wavelength shift. Diffraction effects for positive-tone imaging introduce a deviation between nested and isolated features of approximately 8%, with wider isolated lines [18, 19]. Negative-tone imaging provides roughly equal nested and isolated image sizes. **Figure 7** illustrates the linewidth distribution for both positive-tone and negative-tone imaging systems: The bimodal distribution of (a) clearly shows the isolated-to-nested offset in the positive-tone system, whereas only a single distribution can be discerned in the negative-tone results shown in (b).

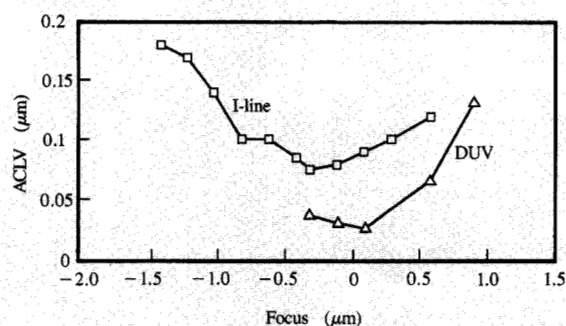


Figure 8

Illustrative effect of focus on ACLV for I-line (365-nm) and deep ultraviolet (DUV, 240–250-nm) patterning. As the focus is moved away from the optimum point, the ACLV degrades dramatically. The ACLV produced using a DUV lithography system is lower than that produced with an I-line system despite the tighter (0.7- μ m) pitch for the DUV system.

The systematic deviation of positive-tone imaging dominates the ACLV performance of that system, while the photolithographic-tool optics and reticle effects are the dominant factors for negative-tone imaging. By combining the use of DUV exposure and negative-tone photoresist, the ACLV was reduced by 50% (**Figure 8**), while simultaneously scaling image dimensions from 0.50 μ m (1.2- μ m pitch) to 0.35 μ m (0.70- μ m pitch). The figure shows that tight focus control is critical to meeting ACLV targets for both the I-line and DUV systems.

Etching Influences

Etching bias variability, defined as the difference between photoresist and etched critical dimensions, can be as large a contributor to the tolerance as the photolithography. Complex multilayer stacks (e.g., an upper insulator layer, a silicide layer, and a lower polysilicon layer [20]) create a difficult tolerance-control problem. These complex stacks are typically used in DRAMs, where long word lines require low resistivity, and in logic derivatives of the DRAM technology. Etching these stacks requires the use of several sequential plasma etching steps, each potentially creating sidewall passivation or polymer buildup, leading to increased linewidth variability, often larger than that introduced by the photolithography. The more common gate structure consists simply of a polysilicon layer, which is much easier to control. The trend in successive MOSFET technology generations has been to reduce polysilicon gate thickness from 430 nm in 1986 to 200 nm in 1994. This thickness reduction has resulted largely

from requirements to improve the gate-length control and planarity. For the single-layer polysilicon-gate structure, control can be quite good, with lithography and etching contributing equally to the linewidth variation.

The most serious etching tolerance issue is etching bias variation as a function of pattern density. For purposes of description, we can separate this into three types [21]: aspect-ratio-dependent etching (ARDE), where differences in linewidth exist depending on the proximity to adjacent features; microloading, where differences in linewidth exist for similarly designed images in the same chip, depending on local pattern factors; and macroloading, where differences in etching bias are created depending on the average loading on a wafer.

Aspect-ratio-dependent etching effects [21] dominate the variation in linewidth as a function of the line pitch for the micrometer-scale dimensions shown in **Figure 9**. For the multilayer stack, the fully isolated lines are more than

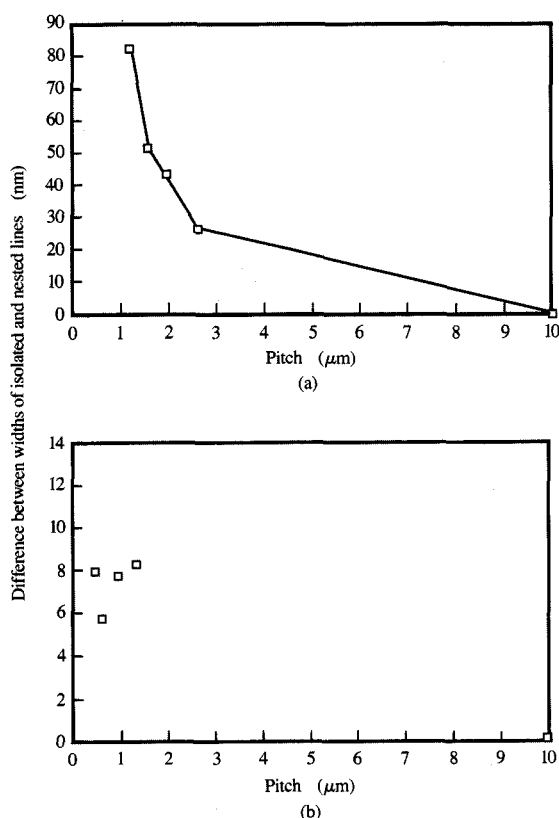


Figure 9

Illustrative influence of line pitch on the difference between the widths of isolated and nested lines for (a) multilayer stack; (b) polysilicon gate.

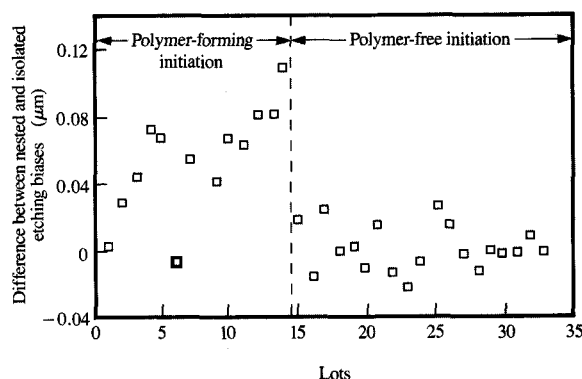


Figure 10

Illustrative effect of polymer-forming initiation step on the difference between nested and isolated etching biases. The widths of isolated lines increase significantly with respect to those of nested lines if a polymer-forming plasma environment is used to etch the antireflection coating and native oxide layers.

80 nm wider than lines at minimum pitch. For the simpler polysilicon gate, the offset between fully isolated and nested lines can be kept to less than 10 nm. Because every chip design uses a broad range of pitch features, it is impossible to escape this influence; hence, there is significant effort to reduce it to improve the ACLV. For conventional positive-tone processing, the effects are additive for photolithography and etching processes. As discussed above, isolated lines patterned with a positive-tone photoresist are wider than nested lines [18, 19]. The isolated lines would be expected to increase in width in etching as well, due to preferential deposition of etching products, photoresist by-products, or reactant by-products [22]; hence, using a negative-tone photoresist is clearly an advantage. Reported causes of deposition include photoresist by-products [23–26], etching by-product decomposition [27], or oxidation of the sidewalls in combination with etching by-product deposition [28, 29]. Polymer formation characteristics are also sensitive to the type of photoresist used [30].

By adjusting the etching process to minimize polymer or passivation deposition, the isolated-to-nested offset was reduced for a simple polysilicon gate. Of the various process sensitivities that were uncovered, the two most significant are shown in **Figures 10** and **11**. Figure 10 illustrates the effect on the difference between nested and isolated etching biases of using a polymer-forming step to remove the antireflection coating and native oxide layers. Polymer deposition results in an increase in the widths of isolated lines of up to 100 nm relative to those of the

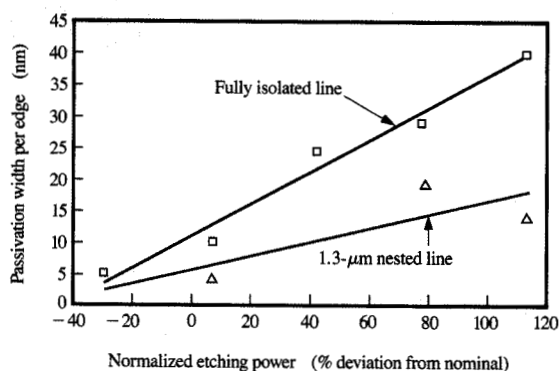


Figure 11

Illustrative effects of etching power on passivation buildup. As the power increases, the deposition of passivation increases, leading to linewidth growth. The effect is larger for a fully isolated line than for a line spaced $1.3\ \mu\text{m}$ from an adjacent line. For lines at minimum spacing, no buildup can be discerned.

nested lines. Figure 11 illustrates the effect of the etching power on the isolated-line growth; as the power increases, the amount of passivation on the isolated line increases significantly, while the increase in the passivation on the width of the nested line is small ($1.3\text{-}\mu\text{m}$ pitch) or unmeasurable ($1.0\text{-}\mu\text{m}$ pitch). The deposition results in a substantial increase in the width of the isolated line relative to that of the nested line.

Both micro- and macro-loading arise from the same mechanisms, where reactant or byproduct density is locally depleted or enhanced because of the surrounding environment [21, 31]. In this paper, we refer to microloading as the more subtle effect, in which changes in local photoresist density change the linewidth. Variations in circuit-design density, proximity to wafer edges (where chips may not be printed), kerfs, blank chips used for in-line diagnostics, or test chips with distinctly different densities, may cause perturbations in the plasma. The distance over which pattern variations may affect etching bias has been observed to be in the 1–10-mm range. For example, for a 64Mb DRAM chip, SEM critical-dimension measurements suggest the distance of influence to be about 2 mm [32]. To further understand this effect, we have fabricated wafers alternating columns of varying photoresist coverages with columns of electrical measurement chips [Figure 12(a)]. We then electrically measured linewidths with 2.1-mm granularity to determine the decay of the loading effect. The effect of the local perturbation on the linewidth for $0.35\text{-}\mu\text{m}$ -wide isolated lines is shown in Figure 12(b); the influence of the loading

decayed over about 6 mm, which is within a factor of 2 to 3 of the mean free path for our etching process. Nested lines were less affected, thus increasing the isolated-to-nested offset.

Macro-loading, which we define as the average loading on the wafer altering the etching bias, is a difficult problem for fabrication plants that manufacture many different

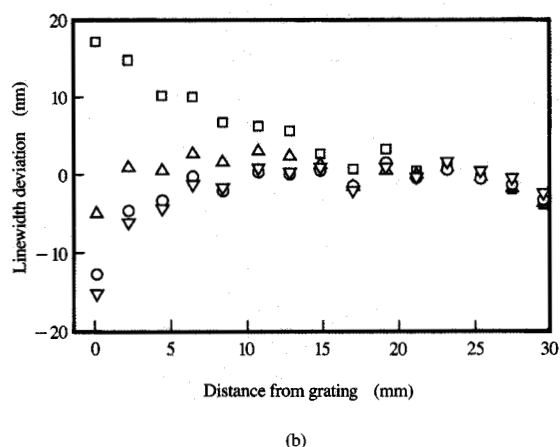
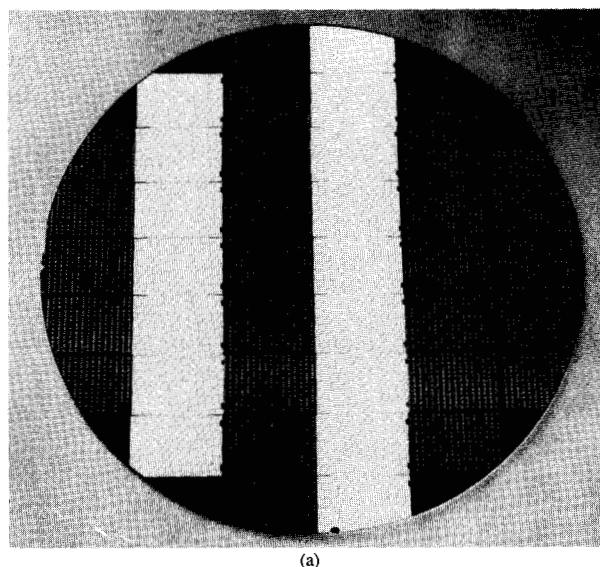


Figure 12

Illustrative effect of local loading on polysilicon linewidth: (a) Photograph of 200-mm-diameter test wafer used to measure the effect of local loading. Different exposures were used to achieve the indicated percentages of photoresist coverage next to a measurement test structure. Electrical measurements were made every 2 mm in a checkerboard pattern to provide statistics. (b) Measurements in the chips adjacent to the variable-pattern areas showed a change in linewidth decaying over about 6 mm. Increasing the photoresist coverage caused a relative increase in linewidth.

types of chips. Lot-to-lot mean control has been one of the greatest dimensional-control challenges in CMOS logic circuit manufacturing, and the macro-loading effect is a significant contributor to the problem, particularly for low-volume chips, as demonstrated previously in Figure 5. Even in the same process technology, it is common to have chip designs with polysilicon patterning as low as 5% (controller chips) or as high as 35% (dense gate arrays). Figure 13 illustrates the etching bias for a dielectric-silicide-polysilicon stack and a simpler polysilicon structure as a function of the patterning density. As the patterning density increases, the etching bias decreases by almost 200 and 70 nm, respectively. In either case, this is a major linewidth tolerance detractor. While the variations can be corrected by adjusting the photolithographic exposure dose, the required dose change may exceed the window available for tight ACLV control.

Differences in reactive ion etching chamber conditions cause additional image-size variation. Electrical-testing data reveal that etching bias, defined as the difference between photoresist and etched feature width, can vary by up to 100 nm between etching chambers. Even for a single chamber, the etching bias can drift by a comparable amount over a number of months. While the problem has not been entirely eliminated, it is being contained by modifying etching chamber cleaning schedules and using an RIE image adjustment process. For example, a brief oxygen etching process can remove as much as 50 nm of photoresist image width prior to the polysilicon etching step. The effects of the oxygen etching are illustrated in Figure 14. As shown, the linewidth can be controllably reduced by increasing the oxygen etching time (a), with no effects on the ACLV (b). However, the oxygen etching eventually degrades the within-wafer uniformity (c), setting an upper limit to such a gate-linewidth tailoring process.

The sidewall profile of the etched polysilicon is another critical dimensional parameter. For advanced logic technologies, we ensure 88 ± 2 -degree etched profiles to meet channel-length specifications. Unfortunately, the profile is strongly influenced by the aspect-ratio-dependent etching and micro- and macro-loading effects. Profile variability not only influences MOSFET channel-length control, but also detracts from the ability to precisely measure linewidth. Variable slopes change the results of four-point probe measurements, which assume rectangular profiles, and top-view SEM critical-dimension measurements, which depend on edge definition. Metrology permitting simultaneous measurement of polysilicon profile and linewidth (e.g., the two-dimensional atomic force microscope [33]) may make it possible to more effectively characterize and address this variability.

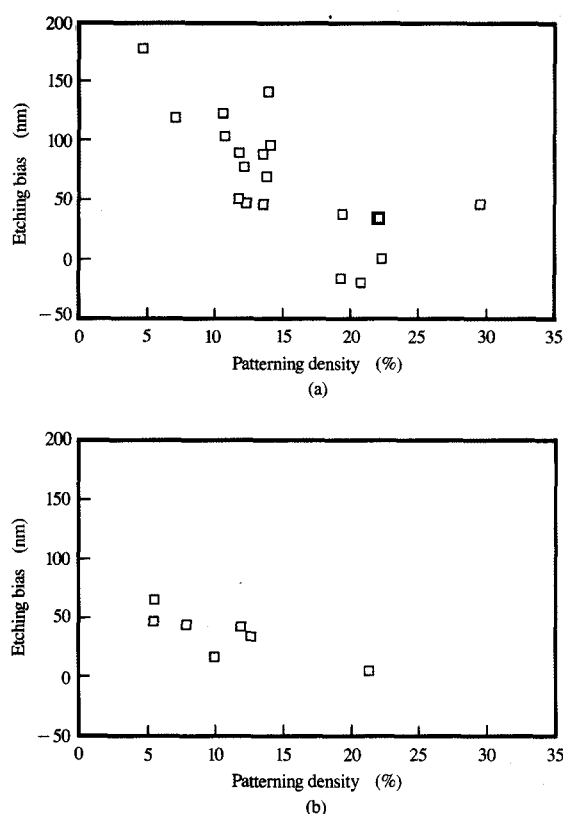


Figure 13

Illustrative effects of pattern density on etching bias for (a) multi-layer stack; (b) simpler polysilicon layer. In both cases, as the amount of patterning decreases, the etching bias increases. The etching bias variation is smaller for the simpler polysilicon layer.

Acknowledgments

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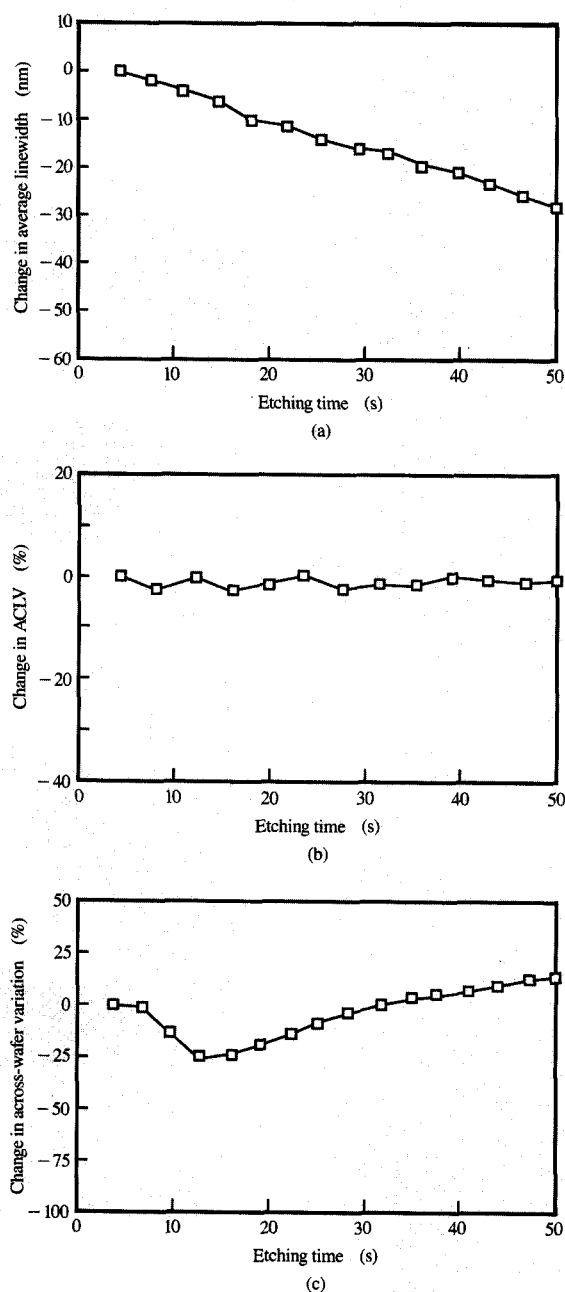


Figure 14

Illustrative effects of an oxygen-reactive ion-etching step on gate linewidth: (a) as the etching time increases, the mean linewidth decreases monotonically; (b) the ACLV is essentially unchanged as the etching time increases; (c) the across-wafer linewidth variation increases with etching time, setting an upper limit to such a gate linewidth tailoring process.

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