Attachment of Solder Ball Connect (SBC) packages to circuit cards

by M. D. Ries
D. R. Banks
D. P. Watson
K. G. Hoebener

IBM has developed an assembly process to attach a new family of Solder Ball Connect (SBC) integrated circuit packages to glass/epoxy cards using surface mount technology (SMT). The process provides nearly perfect yields for the resulting solder ball joint structures and ensures reliability by controlling wear-out due to metallurgical fatigue. The package, card, and process parameters found to most strongly influence the assembly yield and reliability are summarized, and unique test hardware and analysis techniques are discussed. Process considerations, analytical techniques, and test methods described for SBC packages should apply to other ball grid array (BGA) packages.

Introduction

Input/output (I/O) requirements for surface mount technology (SMT) integrated circuit (IC) packages continue to rise with increasing levels of circuit integration. Currently, IC chips with high numbers of I/O connections are predominantly supplied in SMT packages with connecting leads spaced closely around the perimeter. Extension of these packages to higher numbers of connections while keeping a small package size necessitates decreased lead spacings. Packages with leads spaced on centers as fine as 0.3 mm (0.012 in.) are currently being marketed [1]. However, the benefits of the resulting increase in packaging efficiency are offset by decreased assembly yields and increased assembly-process complexity, both adding to system cost. One alternative to packages with leads at the perimeter is a family of IC packages with high numbers of connections arranged in a rectangular grid, or array, on the bottom surface of the package. These surface mount array (SMA) packages promise significant gains in packaging efficiency while maintaining the assembly cost benefits associated with widely spaced SMT connections.

Solder Ball Connect (SBC) packages, which can be classified as ceramic ball grid arrays (BGAs), represent the first IBM entry into surface mount array packaging [2]. These packages were developed around ceramic substrates previously used to manufacture pin-in-hole (PIH) packages [3]. When any ceramic package is attached to glass/epoxy cards with ductile solders, the relatively high mismatch in thermal expansion coefficients between the package and the card is known to present risk for low-cycle metallurgical fatigue of the joints [4, 5]. To address this aspect of reliability for SBC, a new solder ball joint structure was developed by IBM for SBC packages. The work performed to characterize and control the package, card, and assembly process elements required to

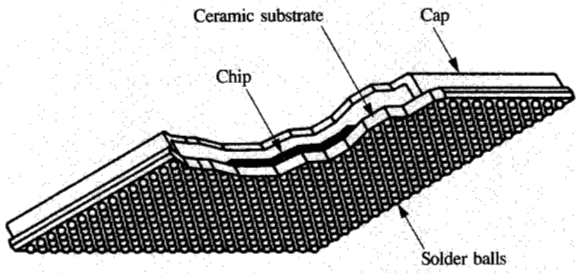

Figure 1

Solder Ball Connect package.

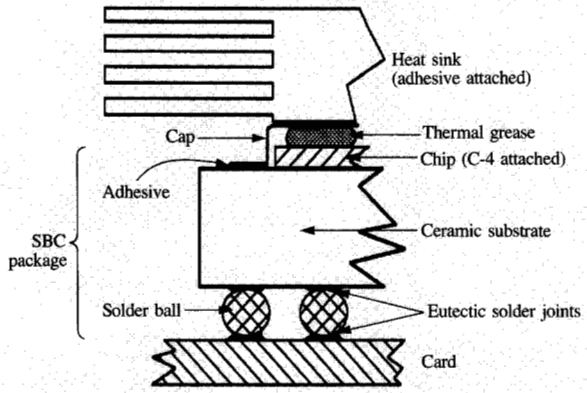

Figure 2

Schematic section of an SBC-to-card assembly. The SBC package elements are bracketed.

successfully manufacture these new structures is summarized in this paper. Test techniques and methodologies used are also described. Most of the considerations discussed for SBC apply to any BGA or SMA package.

- *SBC package description*

IC packages generally provide mechanical support for a chip, a means to bring wiring from finely spaced connections on the chip to widely spaced connections on external leads, and some form of protection for the chip from corrosive environmental and process chemical exposure. IBM manufactures a family of SBC IC packages ranging in size from 14 to 44 mm (0.551 to 1.732 in.) square, with corresponding numbers of leads from 100 to 1225. A 32-mm SBC package, for example, has a body 32 mm by 32 mm square and can provide as many as 625 I/O connections. Mechanical support for IC chips in SBC packages is provided by substrates composed of alumina ceramic. Wiring from the chip to external leads is accomplished by molybdenum circuit lines co-fired within the ceramic substrate body. SBC packages are designed for topside chip mounting, allowing a dense array of external SMT connection leads on the bottom side. As shown in **Figure 1**, the connections are laid out on a rectangular 1.27-mm (0.050-in.) grid and incorporate spherical standoffs. These balls are composed of 90% Pb/10% Sn alloy and are attached to the bottom side of the package with eutectic solder (37% Pb/63% Sn). Attachment of the balls to the card is made in a similar manner, again using eutectic solder during SMT card assembly (**Figure 2**). The high-Pb alloy, which melts fully at 300°C, was chosen to prevent the balls from collapsing during reflow of the eutectic paste (200–215°C) commonly used in SMT assembly processes.

- *SBC card design*

Circuit cards most widely used for SMT applications are fabricated as laminated structures of copper foil and epoxy-impregnated glass-fiber fabrics. SMT IC packages are attached to these cards by soldering the package leads to corresponding copper pads on the card surfaces. Circuit cards for typical SBC applications within IBM require high-density, multilayer technologies. The majority of SBC packages are being attached to cards having 6–10 conductor layers and ranging in total thickness from 1.32 to 1.83 mm (0.052 to 0.072 in.). These cards contain 0.30-mm (0.012-in.)-diameter plated-through-hole (PTH) vias.

Two designs for SBC card pads were considered: "via-in-pad" (circular copper pads surrounding the PTH vias) and "dog-bone" (copper pads offset from the vias), as shown in **Figure 3**. The advantages of the via-in-pad (VIP) design are that larger vias can be used, more surface area is available for signal lines, and electrical performance is marginally improved. However, cards with a VIP configuration require additional manufacturing steps to fill the vias. If left unfilled, vias can steal solder from SBC joints during card assembly, resulting in weak structures. In addition, existing methods of filling the vias (solder leveling, polymer injection, plating, etc.) add the risk of decreasing reliability. Both designs were tested, and dog-bone pads were selected for use in IBM products.

- *SMT assembly process*

A primary process-development objective was to ensure compatibility of SBC packages with the existing SMT assembly process as shown below:

1. *Screen paste* Solder paste applied to card through stencil.
2. *Place* Surface mount packages placed onto paste deposits.
3. *Reflow* Solder melted and allowed to wet package leads and card pads.
4. *Clean* Unwanted paste residues removed.
5. *Place PIH* Pin-in-hole (PIH) packages inserted.
6. *Wave solder* PIH package leads soldered.
7. *Clean* Unwanted paste residues removed.
8. *Inspect/repair* Solder joints inspected and/or repaired.

Development efforts were focused on identifying and controlling the elements of the package, card, and attachment process that most strongly influence SBC-joint reliability and manufacturing yields. These "key variables" were identified through a combination of modeling, experimentation, and analysis. Limits for these key parameters were then set after quantifying their influence on yield and reliability.

The remainder of this paper discusses unique test techniques established for SBC joints, the joint wear-out mechanism, and development efforts to optimize and control yield and joint reliability. The key variables controlling SBC assembly are then summarized, and this is followed by a report of yield performance in a manufacturing environment. A brief description of SBC rework is also included. Specific parameter limits and operating points for most key variables are considered proprietary, and are not detailed.

Test techniques and methodologies

• *Test modules and cards*

Several specialized test modules (electrically functional SBC packages), test cards, and experimental techniques were established to address the reliability and inspection challenges of SBC. The primary reliability concern for SBC is wear-out by low-cycle fatigue of joints. Since product lifetimes are measured in years, accelerated thermal cycling (ATC) is used to characterize the fatigue performance of SBC joints during a relatively short development cycle. Assemblies are cycled through temperature extremes wider than those expected in service, creating high strains within the joints. The acceleration of failure by this increased strain can be predicted from a knowledge of material properties, joint geometries, and wear-out mechanisms [6]. The predicted acceleration factor can then be applied to test data to project reliability under field conditions.

Predicting the SBC failure rate, however, is complicated by the variation in strain associated with joint position in the array. The strain is caused by mismatched rates of thermal expansion between card and package. The magnitude of the shear strain in a joint is roughly proportional to the distance from the joint to the center of the package (DNP, or distance from neutral point), so the probability of failure increases with increasing DNP.

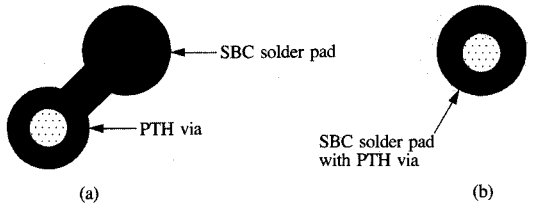

Figure 3

Card-pad alternatives for SBC assemblies: (a) Dog-bone design; (b) via-in-pad design. Dark regions represent Cu on the card surfaces. Shaded regions represent plated-through holes (PTH) in the card.

Cards for ATC testing of SBC assemblies were designed to simplify the collection and analysis of test data by grouping joints according to their DNP. An example of the wiring layout in a representative test card is shown in **Figure 4**. The wiring within the ceramic substrate and in the card consists of several concentric rings; within each ring, the DNPs of the joints are approximately identical. The joints within each ring are connected in series electrically by a "stitched" network. Since all of the joints within each network have approximately the same DNP, they are subjected to approximately equal strains and have equivalent risk for wear-out by fatigue.

These same wiring networks also prove effective for testing surface cleanliness. Residual ionic contamination on the card surface can lead to failure by electromigration or corrosion of metallic conductors under the influence of operating voltages. By biasing alternating rings on the ATC test card with dc voltages and monitoring for current leakage, one can detect the presence of undesirable ionic contaminants. This type of testing, referred to as insulation resistance or surface insulation resistance, is used to monitor the removal of flux residues and other assembly-related surface contaminants as an indicator of cleaning process effectiveness.

One drawback to the test card design just described is the limited number of testable joints in a module. A typical test card for ATC and insulation resistance has only 60% of the total number of joints wired, a practical restriction imposed by test equipment limitations. This lack of joint coverage becomes a concern in attempting to measure module attachment yields, since one can verify the

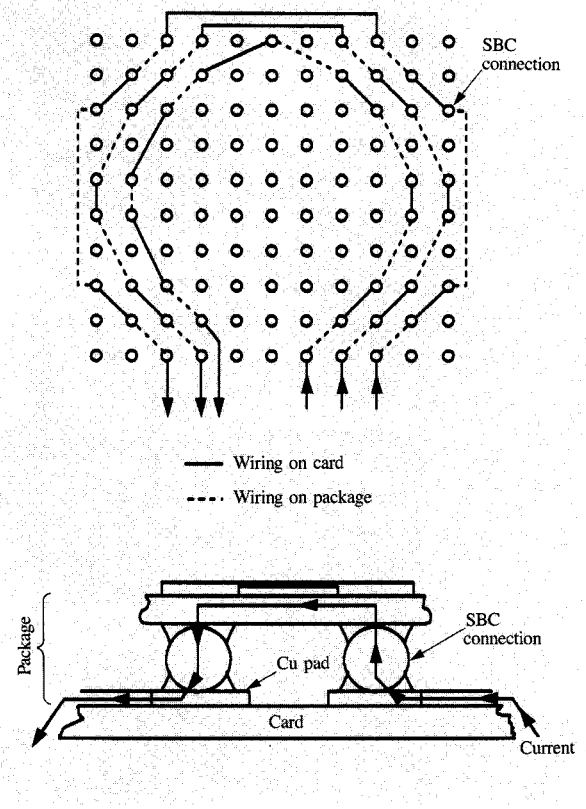

Figure 4

Representative SBC test card wiring for reliability testing. Joints on a single network are at approximately equal distance (DNP) from a hypothetical neutral point located at the package center.

integrity of only those joints that are wired. Open joints were observed as infrequently as one joint per 100 modules (one per 62 500 joints) during experimental yield evaluations. To increase confidence in the ability to detect opens, a unique test card was designed which allowed electrical test access to 98% of the joints in a module. By wiring virtually all of the joints into a single network, one can use a simple check of continuity to verify the integrity of the entire joint array when attachment yields are measured.

While the majority of development concerns could be tested using the two cards just described, several problems could be resolved only by the use of transparent glass packages. These packages were fabricated similarly to ceramic packages, except that transparent glass was substituted for the alumina substrate. Interior joints were therefore visible, allowing direct observation of interactions between solder paste deposits and the balls during and after placement. This also allowed measurement of placement accuracy relative to card pads and observation of solder reflow on a microscope equipped with a heated stage.

- *Inspection techniques*

Unlike joints on perimeter-leaded SMT packages, SBC solder joints (with the exception of those in the outer rows) cannot be visually inspected. Thus, many established inspection and analysis tools used for other SMT packages were found to have limitations when applied to SBC structures. Most notable is the difficulty in using X-ray inspection to image the eutectic joints in SBC assemblies, because the high-Pb-content solder balls are relatively opaque to X-rays.

ATC test performance was often correlated to joint structures by using cross-sectional analyses, but occasions arose when the limited view provided by the section was inadequate. A cross section through a package-to-card assembly allows observation of ATC-induced cracks on only those joints intersected by the plane of section. In contrast, mechanically prying the packages from the card after cycling often provides more information. Separation

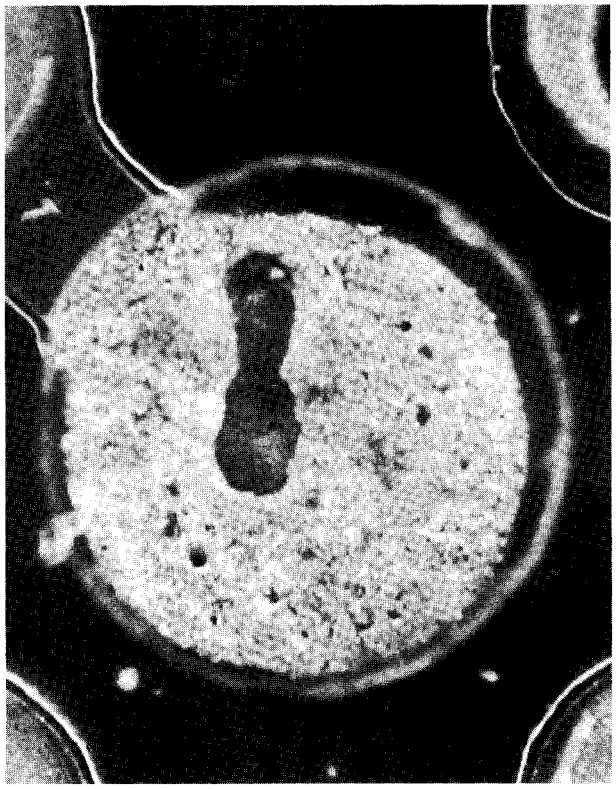

Figure 5

Defective joint revealed by prying the package from the card after testing. Dark region in center of pad was not wet by solder. The black area surrounding the pad is the surface of the circuit card.

of fatigued joints allows optical and scanning electron microscopic inspection of the entire crack surface, which is not possible by cross section. For example, **Figure 5** shows a joint defect that was revealed by prying the package from the card after ATC testing. Another use for the technique was to identify weak joints after initial attachment or rework. When pulled apart, strong joints lifted their associated copper pads from the card. In contrast, weak (or open) joints separated within the solder, providing a quick visual indication of joint integrity.

Wear-out mechanism

The SBC wear-out mechanism was well-characterized during the process development effort. In a typical fatigue failure, as shown in **Figure 6**, cracks begin in eutectic solder joints on both the package and card sides of the balls. Complete failure by through-cracking, however, is generally restricted to the card-side joint. Cracking begins near the card-pad/eutectic solder interface, but does not follow it. Instead, the crack migrates along coarsened Pb-rich phase regions of the joint toward the solder ball, then along the eutectic solder/solder ball interface, exiting through the eutectic solder on the other side of the joint. Cracks propagating through solder balls have not been observed. The initiation point and direction of crack propagation correlate with predictions of strain distributions from finite element models [7]. These models predicted that maximum strains occur in the eutectic solder joints, with relatively low strains developing within the solder ball. This wear-out mechanism is similar to cracking observed in other Pb/Sn joint structures [8].

In addition to crack propagation, an unusual "ratcheting" of solder balls was observed during accelerated testing from 0° to 100°C. Ratcheting is caused by solder balls moving from their original position as a result of stress relaxation during thermal cycling. In any single cycle, joints are plastically deformed at both temperature extremes. At the higher temperature, however, stress relaxation by metallurgical creep [9] results in slightly less deformation than occurs at the colder extreme. This effect accumulates over many cycles to produce the ratcheted deformation observed after testing. The effect, shown in **Figure 7**, is more pronounced at higher DNP as a natural consequence of the previously mentioned dependency of strain on DNP. Much less deformation was observed after ATC testing at lower temperature differentials, but the failure mechanism was identical.

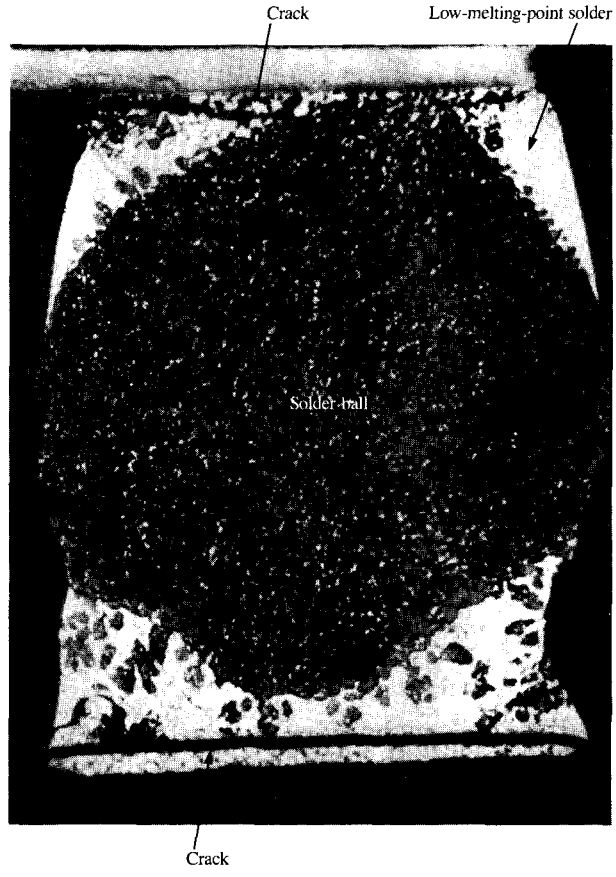

Figure 6

Cross section showing cracks in SBC joints after accelerated thermal cycling between 0° and 100°C.

Assembly process development

- *Process development for yield*

Typical IC packages with leads at the perimeter (e.g., industry-standard "quad-flat-packs") are placed onto screened solder paste patterns on cards and attached by reflowing the solder. Since the completed joints are fully accessible, defects can be detected and repaired, in most cases, by manual touch-up operations without removing the package. In contrast, defective joints in SBC assemblies are not visually detectable and must be repaired by module replacement. This difference results in an obvious need for high SBC-attachment yields.

The types of defects observed during assembly of SBC packages are not unlike those seen for other SMT packages. In general, opens and bridges are the principal defect categories. Open joints can be caused by package misregistration, missing solder (screen print defects), or failure of card pads or SBC balls to be wet by the solder. Bridging can occur between solder balls or between balls and neighboring card vias.

A ball must contact its corresponding solder-paste deposit to make a joint; similarly, two balls resting on the same paste deposit can produce a bridge after the paste is reflowed. It follows, then, that the probability of

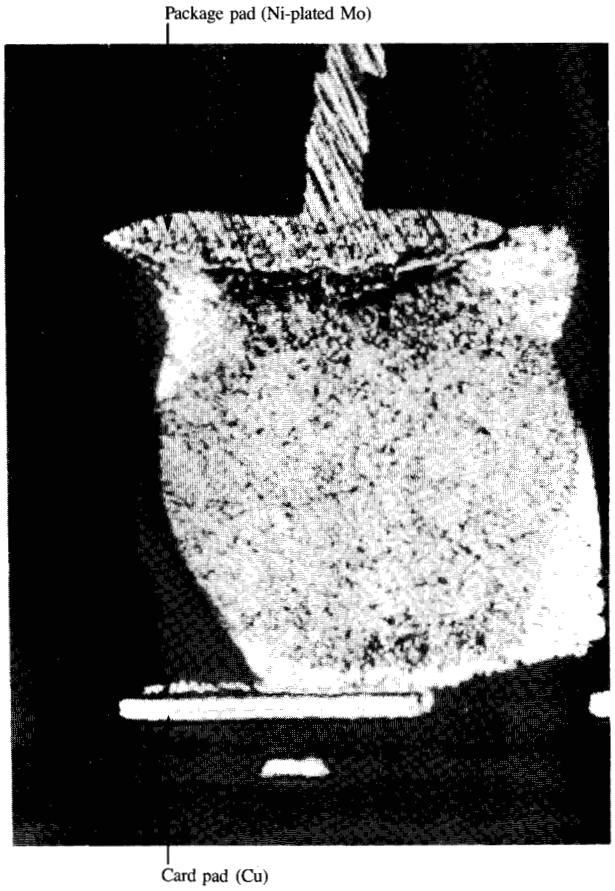

Figure 7

Cross section showing deformation from "ratcheting" of high-DNP SBC joint after cycling from 0° to 100°C.

generating a defect is most strongly influenced by geometric factors. Initial experiments to identify key factors influencing SBC-attachment yield were designed around expected sources of misalignment from the package, card, and assembly process. The effect of ball position relative to paste deposits and card pads was addressed in one multilevel experiment with the following variables:

Ball planarity	Vertical deviation of balls on a package from a plane.
Ball radial error	Radial deviation of an individual ball from its ideal X–Y grid location.
Paste deposit diameter	Diameter of screen-printed solder-paste deposit.
Paste deposit error	Misregistration of individual deposit with respect to its associated pad on the card.
Module placement error	Misregistration of entire package relative to associated site on card.

The 25-mm packages used in the experiment were attached to cards by means of the existing IBM SMT assembly process described earlier. Ball planarity and ball radial error were controlled during manufacture of the test modules by tooling designed to hold the balls in positions with known errors relative to the substrate. Bridges were detected by transmission X-ray, and opens were identified by inspection after prying modules from the cards.

Statistical analysis of the results indicated that ball radial error, paste deposit diameter, and, to a lesser degree, package placement error had significant effects on yield. Paste deposit error and ball planarity did not have significant effects within the ranges of these variables used in this test, although it is obvious that both could influence yields at error levels higher than those tested and should therefore be considered additional key variables affecting yield.

In similar experiments, other potential process influences on assembly yield were tested. Solder paste formulations, elapsed time between solder-paste printing and package placement, package-placement force, variations in reflow thermal exposure, and secondary heating by wave solder were all examined. None of these factors investigated appeared to influence yields as strongly as those variables already identified.

Specifications giving limits for the key variables affecting yield were established through a combination of approaches. In keeping with the goal of minimizing the impact of SBC on existing SMT assembly operations, an effort was made to retain existing specifications. For example, a specification for minimum paste height existed in the established IBM SMT assembly process. Since experimental evidence suggested that this limit would enable us to meet SBC yield objectives, no change was recommended. For the case of paste deposit error, existing specification limits for other packages were actually tighter than necessary for SBC. Since this error is controlled by paste screening and a single stencil is used to print deposits for all SMT packages being attached to a single card, the same specification was applied to SBC.

Other limits, such as those for ball planarity and radial error, were established experimentally. With data from the experiment described above, a mathematical model was generated which quantified the influence of these two ball position parameters on SBC joint yields. In one unpublished analysis by S. Wheeler[1], yield data from the experiment were fit by a least-squares method to a subjectively chosen exponential function, holding package

[1] IBM internal memo to S. Yu dated 8/28/90.

placement and paste deposit diameter effects constant:

$$D = 1.88 \times 10^{-5} e^{0.0191\varepsilon_r}, \quad (1)$$

where D is the fraction of packages defective, and ε_r represents the radial error in mm. Evaluation of Equation (1) with a proprietary value for the yield objective (fraction defective) produced the desired limit for allowable ball radial error. The limit for ball planarity on SBC packages was set by an identical procedure.

Mathematical modeling also proved useful in evaluating the influence of "Z-axis" geometric variables on yields. Phelan and Mahaney[2] developed a Z-axis model to assist in tolerance allocation among ball planarity, card site flatness, and solder-paste-deposit thickness. A Monte Carlo simulation of yield based on experimentally determined statistical distributions of Z-axis variables was utilized. While details of their procedure are contained in the report, it is significant to note here that the simulation validated the previously established specification limits for ball planarity and solder-paste-deposit thickness. More importantly, though, the simulation provided a method of establishing card flatness requirements. This limit is difficult to address experimentally, since it requires manufacture of cards with controlled distortion at SBC sites.

With the exception of solder-paste-deposit thickness, the key yield parameters described to this point have been controlled during package manufacture. One element occurring solely during card assembly is package placement error. As a result of the coarse 1.27-mm (0.050-in.) ball pitch, SBC packages are extremely forgiving of placement errors when compared to packages with perimeter leads spaced more closely (0.30 to 0.64 mm). The SBC tolerance for misregistration is greatly aided, as in other SMT packages, by a strong propensity for self-alignment of the packages with the card during reflow. This is an expected result of surface area minimization driven by the surface energy of molten solder [10]. Self-alignment of 32-mm packages was found experimentally to be capable of recovering up to 0.35 mm (0.014 in.) of placement error. Since this degree of placement accuracy is easily achieved in production environments with standard package placement equipment, process specification limits for package placement error were set slightly below this value.

• *Process development for reliability*

Both card-design and process variables were considered potentially influential on the life of SBC solder joints. Experiments were performed to determine the significance of some of these variables, including SMT pad type (dog-bone versus via-in-pad) and secondary thermal exposure after initial package attachment reflow. The secondary thermal exposure can occur in a normal assembly sequence during adhesive-cure operations and during wave solder of a card bearing SBC packages. Results of experiments were evaluated by taking cross sections of 25-mm packages after ATC cycling from 0° to 100°C at three cycles per hour. After cycling, metallographically mounted packages were sectioned along diagonals, exposing 19 SBC joints for measurement (two balls at each DNP and one center ball). Individual cracks on both the package side and the card side of the balls were measured and counted for analysis. Results indicated that secondary thermal exposure did not significantly affect joint reliability, but via-in-pad structures were slightly more reliable than joints attached to dog-bone pads. This improvement in reliability associated with VIP pads was not, however, significant enough to offset the negative aspects of this card structure previously described in the subsection on SBC card design.

Examinations of thermally cycled joints indicated that the distance between the card pad and the solder ball, or "gap," might influence SBC reliability. Gap size is a function of many variables in the SBC joint structure: package-side solder volume, card-side solder volume, package-side Pb dissolution into molten eutectic solder, solder ball diameter, solder ball planarity, ceramic substrate flatness, card site flatness, and package attachment reflow time. Gap measurements consistently showed high variability, with averages ranging from 0.01 to 0.06 mm (0.0003 to 0.0018 in.) and standard deviations from 0.01 to 0.04 mm (0.0003 to 0.0016 in.).

To determine the influence of gap on reliability, a test was run using packages that had some of the balls mechanically flattened, effectively increasing the gap. In a related effort, packages in which most of the solder balls were composed of 37% Pb/67% Sn rather than the normal 90% Pb/10% Sn solder were attached to cards. The rationale was that if gap contributed to thermal cycling failure, the cause was rooted in the presence of an interface between the eutectic solder and the 90% Pb/10% Sn balls. When eutectic balls which melted at lower temperatures were substituted for the 90% Pb alloy, the balls would melt at the same time as the paste deposit and solidify into a joint of uniform composition. Thus, the interface was removed from the structure, and an effective gap of 0.91 to 0.94 mm (0.036 to 0.037 in.) was generated. Some solder balls on each package were composed of higher-melting-point 90% Pb/10% Sn to prevent collapse of the all-eutectic joints.

Results of these tests, however, indicated that neither flattened packages nor eutectic ball packages had significantly different reliability from the normal structures. Despite the absence of a eutectic solder/solder ball interface, crack propagation in eutectic ball samples

[2] G. Phelan and V. Mahaney, "Application of Z-Axis Model for Solder Ball Connect Product," *Technical Report TR-01.C666*, IBM Endicott, August 1992.

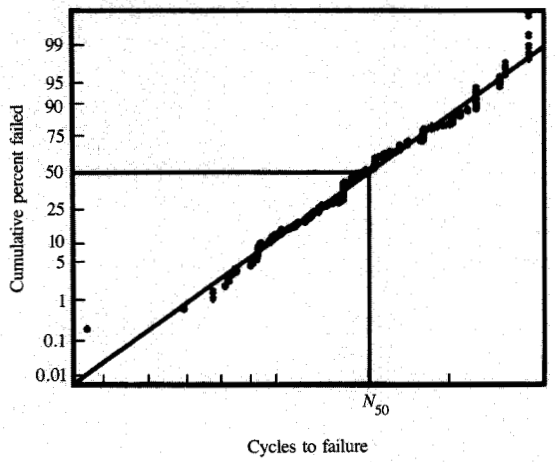

Figure 8

Fatigue life distribution for SBC joints under ATC.

proceeded through roughly the same part of the joint as with normal solder balls. The size of the gap between solder ball and card pad, therefore, was not found to be a factor in reliability performance.

Additional experiments showed that most assembly process variables had little effect on SBC reliability and should not be considered "key" variables. For example, secondary thermal exposures from adhesive cure, wave solder, and encapsulant bakes did not significantly affect joint lifetimes. Neither did variations in flux formulation nor reflow methods (infrared, convective/infrared, and vapor-phase).

Several variables that have an obvious influence on reliability are already controlled by existing SMT assembly specifications and, while considered key to SBC reliability, did not require significant development effort to identify. These included existing limits on card- and joint-reflow time and temperature. Similarly, SBC package manufacturing considerations yielded limits for solder ball diameter, solder ball cleanliness, and package-side pad diameter, all of which must be controlled to ensure SBC assembly reliability.

- *Joint structure optimization*

As concluded in the previous section, assembly process variables had little influence on joint reliability. In contrast, SBC solder joint reliability was found to be strongly affected by joint geometry and structure in a series of pivotal experiments that examined the fatigue life of SBC assemblies built with varying card-pad diameters, package-pad diameters, and card-side solder volumes.

Before discussing these experiments, it is necessary to provide some additional background on SBC reliability models. Low-cycle fatigue of SBC joints has been modeled using a modified Coffin–Manson relationship relating cycles-to-failure to strain magnitude [11]. At any given level of strain, the joint-to-joint variations in fatigue lives of SBC solder joints are well represented by lognormal failure distributions (**Figure 8**). Test populations can be characterized by the lognormal parameters N_{50} (mean life) and σ (standard deviation, which correlates with the slope of the cumulative failure distribution). Failure distributions, in conjunction with acceleration factors from the Coffin–Manson model, allow field reliability to be projected from accelerated laboratory tests. Typically, N_{50} is large compared with the useful life of most systems that include SBC modules. Therefore, if σ is small, the probability of failure of any joint in a system during the useful field life is very small. On the other hand, if σ is large, the probability of any failure occurring during the system lifetime is appreciable.

Finite element modeling of joint strains by Corbin [7] predicts that maximum mean life will be achieved when the card-pad diameter equals the package-pad diameter. Since high N_{50} and low σ values are desirable, **Figure 9** summarizes the results of a series of tests designed to quantify the influence of card-pad diameter and package-pad diameter on SBC joint reliability. It is apparent that larger card-pad diameters and smaller package-pad diameters extended the mean lives of SBC solder joints. However, smaller package-pad diameters also increased σ, which in turn decreases projected field reliability.

Solder-paste-deposit volume on the card side was tested for influence on reliability at the same time as pad diameters. The volume was experimentally varied over only a range expected to occur in a production environment. Over this limited range, card-side solder paste volume had no significant effect on SBC joint reliability, but a significant interaction between solder volume and card-pad diameter was identified. This interaction was explored more fully in work performed by Phelan and Wang [12] to assist establishment of specification limits for these key variables. Their work showed that once the card-pad diameter is established, joint reliability is strongly dependent on the minimum cross section, or fillet diameter, of the card-side joint. Joint diameter, then, can be specified as a product characteristic controlling reliability. The minimum cross section effectively establishes the minimum distance through which a crack must propagate to make the joint fail. Printed solder-paste volume is the primary process variable controlling the joint cross section. As solder volumes are increased on a given card-pad diameter, joint shapes change from concave to convex. For concave joints, the minimum cross section, which controls reliability, is at the

Table 1 Primary influence of key SBC parameters and variables.

Parameter/variable	*Influence*
Modules	
Ball diameter	Reliability
Ball cleanliness	Reliability and yield
Ball attachment temperature	Reliability and yield
Ball attachment time	Reliability and yield
Pad diameter	Reliability
Ball planarity	Yield
Ball radial error	Yield
Cards	
Pad diameter	Reliability
Coefficient of thermal expansion	Reliability
SBC site flatness	Yield
Assembly process	
Solder paste volume	Reliability
Paste deposit thickness	Yield
Paste deposit error	Yield
Module placement error	Yield
Reflow joint temperature	Reliability and yield
Reflow card temperature	Reliability

fillet. Conversely, when solder volumes are increased sufficiently to produce convex joints, the card pad controls wear out, since the minimum joint section is at the card. This work, then, provides an understanding of the observed interaction between solder volume and pad diameter, supporting the conclusion that both variables are important for SBC reliability.

Though it would seem desirable to specify the largest possible card-pad diameter and solder volume, additional considerations add practical constraints. For example, limits of card manufacturing processes restrict the maximum card-pad diameter. Similarly, the maximum solder volume is limited by an associated risk for yield loss due to shorts.

As noted previously, reliability could be maximized by equalizing pad diameters on the card and package. Once the card-pad diameter had been established, it became apparent that the package-pad diameter could not be reduced to the same dimension because of constraints related to manufacture of the package. Establishment of specification limits for the key variables controlling SBC reliability therefore involved some trade-offs. Nevertheless, resulting joint structures exceeded the reliability requirements of the anticipated applications. In fact, the cumulative probability for failure of 32-mm SBC packages by thermal fatigue wear-out in a typical high-performance desktop product was projected to be below 1 ppm at the end of the expected product life.

- *Key variables*

In summary, **Table 1** lists the key variables for SBC assembly and their primary influence.

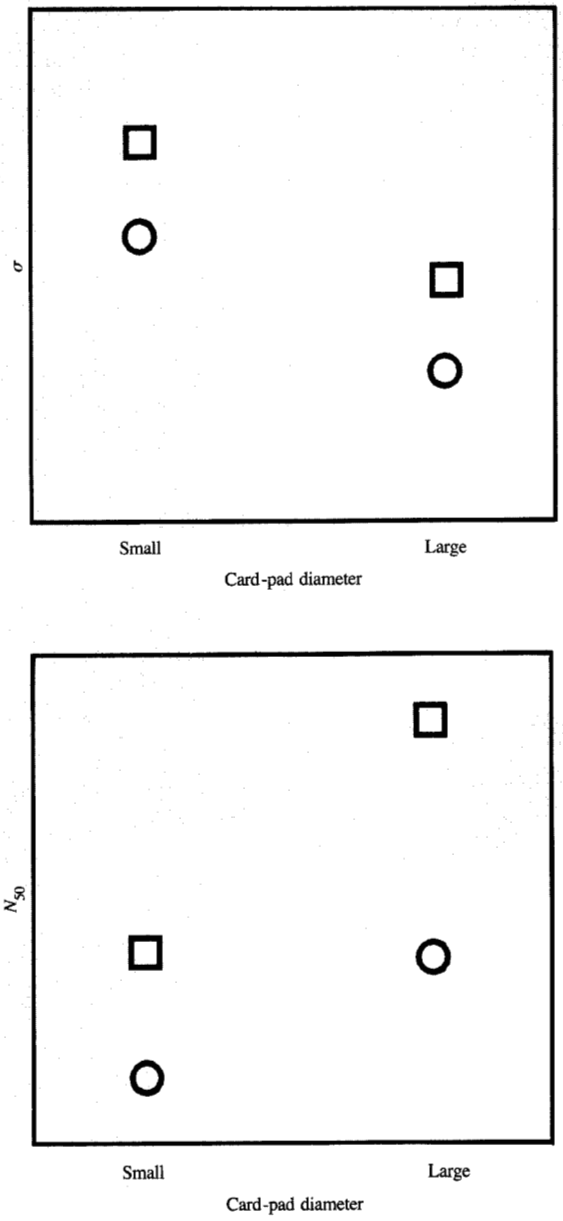

Figure 9

Influence of pad geometry on SBC reliability. Plots show that increasing the card-pad diameter extended joint life and reduced variability, independent of package-pad diameter. Also shown is an improvement in life resulting from decreased package-pad diameter relative to card-pad diameter.

Yield

Experience in manufacturing environments to date has proven the SBC attachment process to be capable of producing joint defect rates in the part-per-million range. Control of the key variables just summarized has resulted in an extremely robust assembly process. In one series of assembly trials conducted in the IBM Toronto high-end memory manufacturing line, over 450 32-mm SBC modules (285 000 solder joints) were assembled with zero defects, supporting an estimated yield exceeding 99.7% per module. This low level of defects is significantly below that experienced when attaching packages with narrowly spaced perimeter leads. It is not unusual for a 0.4-mm (0.016-in.)-pitch package with a high number of I/O connections to have first-pass card-attachment defect rates greater than 10%.

Rework process

Regardless of the high first-pass yields, a viable rework process for SBC is required to support product development, recover from manufacturing errors, and allow upgrades to product cards. Unlike first-pass assembly, rework of SBC packages required development of a unique process. The high thermal mass associated with thick ceramic packages posed special challenges. The process that was developed makes use of a hot-gas reflow tool for removal and re-attach operations.

As shown below, rework parallels initial assembly in many respects:

1. *Remove package*	Module is heated and lifted from card.
2. *Dress SBC card site*	Remaining balls are removed.
3. *Touch up card pads*	Bridges are removed and non-wet pads are restored.
4. *Flatten site*	Site warpage is removed and card pads are planarized.
5. *Apply solder*	Solder paste is applied to new package.
6. *Place package*	Package is placed on card site.
7. *Reflow*	Package is heated to form joints.
8. *Clean*	Process residues are removed.

Whole-card preheat is needed to assist reflow, especially on thick cards. Because the eutectic joints on both sides of the solder ball are molten during package removal, high-melting-point solder balls are left attached to the card at random. These balls and residual solder are removed by exposing the site to a fountain of molten solder. Heat from the solder fountain locally deforms the site where the SBC package was removed, necessitating a site-flattening step. This operation also flattens the highest solder domes on the card, preventing package module skew during placement. Application of solder paste to a reworked SBC site on a populated card is difficult, so solder paste is screened directly onto the solder balls of a package before the module is loaded into the hot-gas rework tool. As in initial assembly, care must be taken to provide adequate solder paste volumes to ensure yield and reliability of the reworked SBC package. The package is then placed on the card, reflowed, and allowed to cool undisturbed.

Summary and conclusions

SBC packages, like other SMA packages, increase the density of I/O connections when compared to packages with perimeter leads. A new solder ball joint structure, which is fully compatible with existing SMT processes and exhibits exceptionally high yields, accommodates thermally induced strains during product operation and ensures the high field reliability of SBC assemblies.

New procedures were established for SBC to aid development of the assembly process and test for reliability. Redesigned test cards, which grouped SBC joints into concentric electrical test networks according to their probability of failure, were used to improve ATC testing efficiency and to evaluate surface cleanliness of the completed SBC assemblies by monitoring the electrical resistance between adjacent ATC test networks. Additional test cards were designed to enhance measurement of assembly yields by providing a single electrical continuity check for 98% of the joints on an SBC module-to-card assembly. Specialized hardware and analysis techniques were used to overcome limitations of conventional inspection methods when applied to SBC structures. Prying packages from cards after ATC cycling often proved to be a more valuable technique for joint failure analysis than conventional cross-sectioning.

The wear-out of SBC joint structures proceeded by propagation of low-cycle metallurgical fatigue cracks through the solder joints, not through the balls. In addition, a "ratchet" deformation of SBC joints was observed after ATC testing which resulted from stress relaxation during elevated-temperature test cycles.

Nearly perfect first-pass assembly yields in IBM SMT card assembly production facilities were achieved by identifying and controlling key package and process variables. Package and solder-paste-deposit geometries, planarity and radial error of the ball, and card site flatness had the most influence on yield. In addition, process variables such as solder-paste-deposit thickness, paste deposit error, and package placement error strongly influenced SBC attachment yield. First-pass SBC attachment yield was greater than 99.7% in trials conducted in an IBM production facility, which greatly exceeds typical first-pass yields for alternative package technologies with equivalent numbers of perimeter leads.

High reliability for SBC assemblies was also achieved by a "key variables" approach. Product reliability objectives

were exceeded by increasing solder volume and pad diameters. Reliability of SBC-to-card assemblies is also influenced by ball diameter, ball cleanliness, and solder reflow times and temperatures.

Since SBC packages are ceramic ball grid arrays, most of the methods described in this paper to develop and test the SBC-to-card attachment process apply directly to other surface mount array packages. Many of the process variables and package parameters found to influence SBC attachment yield and reliability are expected to have a similar influence on other surface mount array package attachment processes.

Acknowledgments

The authors have reported on the efforts of a great number of individuals at several IBM locations. We gratefully acknowledge the contributions of all of those people to the successful development of the SBC assembly process. We are especially grateful to B. Arrington, R. Behun, J. Benenati, T. Caulfield, M. Cole, J. Corbin, M. Cretekos, R. Darmoni, R. Eklund, D. Ellison, D. Foster, D. Glinski, C. Heim, S. Iannone, E. Ingalls, P. Isaacs, W. Jimenez, E. Jungman, D. Kelley, C. Kephart, A. Kiehle, L. Klober, R. Lewis, T. Lyons, E. McLeskey, D. Mead, G. Phelan, J. Potenza, H. Quinones, M. Quirk, S. Rooks, T. Rosenmayer, F. Sucato, J. Tomaine, S. Tran, K. Vanderlee, S. Wang, S. Wheeler, M. Winton, S. Yu, and A. Zubelewicz.

References

1. R. Ray, "High-Density and Very Fine-Pitch IC Packages: A Technology Assessment," *Proceedings of the Eleventh IEEE/CHMT International Electronics Manufacturing Technology Symposium*, IEEE, Piscataway, NJ, 1992, pp. 151–158.
2. F. F. Cappo, J. C. Milliken, and J. M. Mosley, "Highly Manufacturable Multi-Layer Ceramic Surface Mounted Package," *Proceedings of the Eleventh IEEE/CHMT International Electronics Manufacturing Technology Symposium*, IEEE, Piscataway, NJ, 1992, pp. 424–428.
3. *Microelectronics Packaging Handbook*, R. R. Tummala and E. J. Rymaszewski, Eds., Van Nostrand Reinhold, New York, 1989, pp. 476–492.
4. R. E. Reed-Hill, *Physical Metallurgy Principles*, Second Edition, D. Van Nostrand Co., New York, 1973, pp. 823–824.
5. *Microelectronics Packaging Handbook*, R. R. Tummala and E. J. Rymaszewski, Eds., Van Nostrand Reinhold, New York, 1989, pp. 803–826.
6. K. C. Norris and A. H. Landzberg, "Reliability of Controlled Collapse Interconnections," *IBM J. Res. Develop.* **13**, 266–271 (1969).
7. J. S. Corbin, "Finite Element Analysis for Solder Ball Connect (SBC) Structural Design Optimization," *IBM J. Res. Develop.* **37**, 585–596 (1993, this issue).
8. R. Satoh, K. Arakawa, M. Harada, and K. Matsui, "Thermal Fatigue Life of Pb–Sn Alloy Interconnections," *IEEE Trans. Components, Hybrids, Manuf. Technol.* **14**, No. 1, 224–232 (1991).
9. R. E. Reed-Hill, *Physical Metallurgy Principles*, Second Edition, D. Van Nostrand Co., New York, 1973, pp. 841–887.
10. S. K. Patra and Y. C. Lee, "Modeling of Self-Alignment Mechanism in Flip-Chip Soldering—Part II: Multichip Solder Joints," *Proceedings of the 41st Electronic Components and Technology Conference*, IEEE, Piscataway, NJ, 1991, pp. 783–788.
11. T. Caulfield, J. Benenati, and J. Acocella, "Cost-Effective Interconnections for High I/O MCM-C-to-Card Assemblies," *Surface Mount Technol.* **7**, 18–20 (1993).
12. G. Phelan and S. Wang, "Solder Ball Connection Reliability Model and Critical Parameter Optimization," *Proceedings of the 43rd Electronic Components and Technology Conference*, IEEE, Piscataway, NJ, 1993, pp. 858–862.

Received March 16, 1993; accepted for publication June 14, 1993

Michael D. Ries *Hewlett-Packard Company, 3404 East Harmony Road, Fort Collins, Colorado 80525.* Mr. Ries joined the IBM Boulder Development Laboratory after graduating with a B.S. in metallurgical engineering from the Colorado School of Mines in 1976. He worked on a variety of projects for copier and printer products, including materials support and assembly process development for ink-jet and LED printheads. While at IBM Technology Products, Mr. Ries focused on SMT assembly process development. He holds one patent and has received three IBM Outstanding Technical Achievement awards. Mr. Ries was an Advisory Engineer in Assembly Process Design; he is currently employed by the Hewlett-Packard Company.

Donald R. Banks *Motorola Inc., 3501 Ed Bluestein Boulevard, Austin, Texas 78762.* Mr. Banks joined IBM in Austin, Texas, in 1988. He received a B.S. degree in metallurgical engineering from the Montana College of Mineral Science and Technology in 1984 and an M.S. in materials science and metallurgical engineering from the University of Notre Dame in 1986. Mr. Banks has published technical papers on intermetallic compound growth, circuit board solderability, and solder joint corrosion. The work presented in this paper was carried out while the author was a Staff Engineer in the IBM Assembly Process Design organization. He is currently a Process Technologist in the Motorola Advanced Package Development and Prototype Laboratory.

David P. Watson *Planar Systems, Inc., 1400 Northwest Compton Drive, Beaverton, Oregon 97006.* Mr. Watson is currently employed by Planar Systems. When the work presented in this paper was performed, he managed the Area Array Assembly Process Development Department in the IBM Assembly Process Design organization at Austin, Texas. Mr. Watson joined IBM in 1979 and has made significant contributions to developments in printed wiring board, SMT,

TAB, and area array surface mount technology, including two key patents. He received the B.S.M.E. degree from the California Polytechnic Institute in San Luis Obispo in 1979, and the M.S.M.E. degree from the University of Texas in Austin in 1987.

Karl G. Hoebener *IBM PC Company of the Americas, 11400 Burnet Road, Austin, Texas 78758 (HOEBENER at AUSVMV).* Mr. Hoebener joined IBM in 1968. He has worked in all phases of first- and second-level packaging technology in East Fishkill and Austin. He holds four patents and has received one IBM Outstanding Technical Achievement Award. He is currently an Advisory Engineer in Panel Early Manufacturing Involvement.