

X-ray lithography in IBM, 1980–1992, the development years

by Alan D. Wilson

The IBM X-ray lithography research and development program is outlined, from a personal perspective, covering the period from the inception of the program in 1980 through the development of IBM's own storage ring for X-ray production in 1992. The following aspects, among others, are discussed: origins of the program; acquisition of an X-ray port at Brookhaven National Laboratory; masks for X-ray lithography; development of special tooling for X-ray lithography, including a wafer stepper, a precision e-beam X-ray mask writing system, and a superconducting (dipole) electron synchrotron installed in the IBM Advanced Lithography Facility (ALF) in East Fishkill, New York. Key device programs were conducted to increase understanding of the X-ray lithography process and confirm its utility.

Introduction

In mid-August of 1980, IBM Fellow Alec Broers summoned four lithography researchers to a small

conference room in the IBM Armonk headquarters: Janusz Wilczynski, Mike Hatzakis, Warren Grobman, and myself. Broers had recently been instructed by the IBM Corporate Technical Committee (CTC) to initiate an X-ray lithography development effort. Grobman was to head the project; Hatzakis, a resist expert, was to develop an X-ray resist; Wilczynski, as an optical lithography and tooling expert, was to develop an alignment system; and I was to develop a stepper system. This was quite a distinguished crew: Broers was an IBM Fellow, Hatzakis and Wilczynski later became IBM Fellows, and Grobman had a number of accomplishments in lithography and science. The goal of the Armonk meeting was to establish a cross-departmental effort on X-ray proximity printing lithography.

IBM Research had had a good science effort in X-ray lithography during the 1970s, largely thanks to the team of Ralph Feder, Eberhard Spiller, and John Topalian [1]. X-ray lithographers were concerned with 1) reducing the penumbral blur caused by a finite source size and a greater-than-zero mask/wafer gap; 2) minimizing the component of overlay error caused by the nonzero mask/wafer gap and the variation in this gap due to

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mask/wafer flatness; and 3) competing with optical lithography in throughput.

The establishment of a program was a formidable task, since half of this distinguished group seriously questioned the need for and the viability of X-ray lithography. Grobman, however, had convinced the CTC that an X-ray lithography effort should be started because of impending resolution limits of optical lithography, and that the IBM X-ray effort should be based on an electron synchrotron rather than conventional X-ray sources [2].

In 1980, 16Kb (kilobit) memory chips fabricated using ~5-6- μ m ground rules were the standard in high-volume production, and 64Kb chips were just being introduced in the market. The hottest microprocessor was the Intel 8080, and the Intel 8088 was soon to be available in quantity. One year after that August organizational meeting, in August 1981, the IBM PC would be announced, although computers were still a province of data processing organizations and not yet on every desktop. In lithography, tooling consisted of 1 $\times$ magnification scanners and the last vestiges of contact printing; optical steppers were just beginning to emerge (an outgrowth of optical pattern generators for mask making); and e-beam lithography tools were either slow or expensive or both, but fully capable of resolution and overlay requirements for chips envisioned for the late 1980s.

Optical lithography, in 1980, was very poorly understood by the experts. On the basis of historical trends and current difficulties with existing tooling and technology, the limits of lithography were thought to be about 1-1.25 μ m for optics. X-ray lithography, consequently, was targeted for entry around 1 μ m, the perceived limit of optical lithography.

At the onset of the program the strategic advantages of X-ray lithography were stated to be high resolution (better than optical lithography), throughput superior to that of e-beam technology, better resist-processing characteristics, and potentially lower defects (no multilayer resists).

When the IBM X-ray lithography program began, it was solely a Research Division program. Grobman consolidated a small conventional (i.e., nonsynchrotron) X-ray lithography group and several additional staff members into a storage ring (synchrotron) project and moved my e-beam tooling effort into his organization. There were no representatives from the technology divisions for the next five or six years.

We spent the remainder of 1980 developing a financial and technical program plan for X-ray lithography based on synchrotrons, considering a number of basic questions: Where were exposures going to be done? What should the mask be made from, and how would it look? How would we develop a stepper/aligner system, and what would be the role of vendor assistance in this regard? What would be the staffing needs (the initial group included only six

people) as the program progressed? And finally, what should the test vehicle be?

It was recognized early in the drafting of our program that we were targeting manufacturing—not device prototyping, but full manufacturing. Our manufacturing divisions would eventually be our customer. Consequently, throughput at reasonable rates, 30-60 wafers per hour (equal to optical lithography), would be essential. From the point of view of technology, this would put increased emphasis on four salient factors:

1. High-flux sources for manufacturing: synchrotron radiation.
2. Mask areas larger than one inch square: Chips in 1980 were only about 1/30th of an inch square.
3. Fast aligner/steppers: System throughput of more than 30 wafers per hour would be required.
4. Time: The new technology should be ready for manufacturing between the middle and the end of the next decade, i.e., 1985-1990.

Figure 1 illustrates the anticipated lithography needs from the last half of the 1980s to the year 2000. There was a great deal of opportunity beyond the expected 1- μ m optical limit, and this is what lithographers were focusing on.

Environment

The lithography scene at the initiation of the IBM X-ray lithography research and development program in 1980 was one in which 16Kb memory chips were the production standard, with pilot runs of 64 Kb. These were produced largely with 1:1 ring-field projection scanner tools having a printing resolution of ~2 μ m. Anyone who has been connected with manufacturing can confirm that production of memory chips is near chaos in the first year or so because tool, process, and design are stretched to the limit. IBM has always had an insatiable demand for memory. Consequently, we have always sought any and all means possible to gain the competitive edge in memory chip production. We funded, directly or through purchase agreement, many lithography efforts during the 1980s: Perkin-Elmer 1:1 scanners; GCA, Canon, Nikon, and Censor reduction optical steppers of different magnifications; electron-beam systems; and X-ray lithography. It is likely that IBM had, among its numerous research, manufacturing, and development sites, multiple copies of every conceivable lithography tool ever created. Our strategy was "if in doubt, try it out."

At Research there has always been a feeling that lithography has played a dominant role in the advance of memory chip technology, and that it remains an area fertile for future advances. It is accepted that for over twenty years semiconductor technology has grown in complexity

and performance at a formidable rate of 25% per year because of innovation in lithography. Lithography permitted this unprecedented growth in chip power over such a long time span because fresh technology was constantly being invented and deployed. And it is not over; every three to four years the wiring ground rules are reduced by 0.707, and the memory capacity in bits quadruples.

By 1985–1986 IBM was making 1Mb memory chips in high volume with optical lithography at $\sim 1.1\text{-}\mu\text{m}$ minimum feature sizes. Three years or so later 4Mb DRAMs were in volume manufacturing and, in late 1992, 16Mb chips with $0.5\text{-}\mu\text{m}$ ground rules were jointly produced in volume by IBM and Siemens in a new plant in France, again using optical lithography. Currently, 64Mb chips are being made in East Fishkill, again with optical lithography. In 1980 wafers were ~ 2 in. in diameter, with a transition to ~ 3 in. or 4 in. anticipated or under way. Wafers 8 in. in diameter were unheard of and were not discussed by anybody. Today, 10 to 12 years later, 8-in. wafers are the standard in IBM manufacturing. The bottom line is that over 12 years (1980–1992), chip complexity grew at unheard-of rates, past all perceived limits: Minimum cell area shrank $50\text{--}100\times$, and wafer area grew about $50\times$, for a total wafer complexity of about $3000\times$! The price of memory in cents per bit dropped from 0.03¢ to 0.000015¢ per bit, a reduction of $\sim 2000\times$. Early in this era, we embarked on our risky technical program to address the lithographic needs of the mid to late 1980s and beyond.

My first role in this program was as manager of a stepper development effort that also included an e-beam mask-patterning/writing effort. This responsibility began in August of 1980. In June 1983 the X-ray program manager, Warren Grobman, left the program, and I assumed full responsibility. In early 1985, my responsibilities expanded again with the chip-patterning programs for Research added to the X-ray program. The X-ray effort had about 20 people and the e-beam effort about 25. I continued to manage the chip lithography program until October 1990 and remained involved technically with the “Helios” electron storage ring until its final acceptance at East Fishkill early in 1992.

Key elements

At the onset of our X-ray lithography program we identified several key elements: masks, exposure systems, and test vehicles, i.e., chips. To illustrate the interrelationships of many variables, I devised a Venn (logic) diagram (Figure 2) as a means of illustrating for a wide audience, ranging from staff from the Chairman’s office to visitors at Research, the complexity of interrelationships among the many elements of the program. As we can see from this logic diagram, any research and development program for X-ray lithography has many

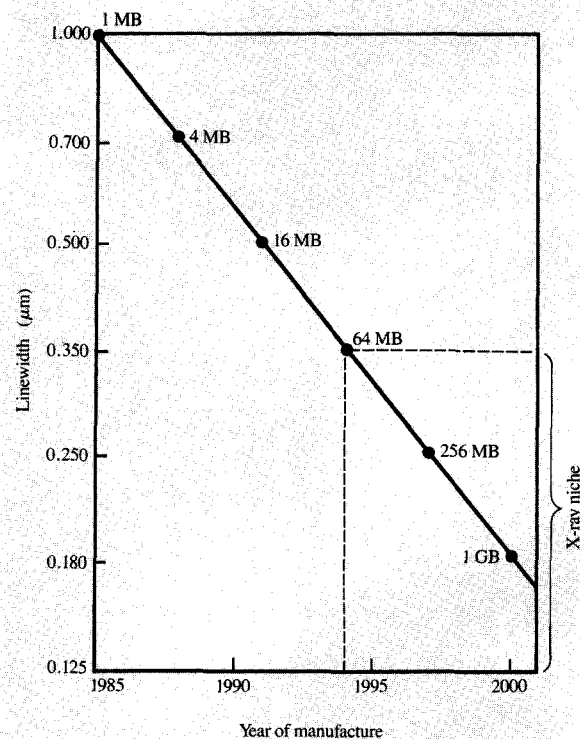


Figure 1

Projected lithographic requirements for dynamic random access memory (DRAM) from the last half of the 1980s to the year 2000, and the target therein for applying X-ray lithography.

variables and much interplay among them, all of which must be taken into account in each technology decision.

• Masks

An X-ray mask consists of a thin support material, or membrane, which is transparent to X-rays, upon which an absorber is selectively placed in a one-to-one relationship to the pattern desired on the wafer. In the early stages of the program, boron nitride (BN) was the material most frequently talked about as a mask material for X-ray lithography. We had no significant experience with BN, nor any equipment or facilities to grow a thin membrane. Grobman, in what turned out to be a fortuitous decision, chose silicon because IBM had a wealth of knowledge about Si and could make thin membranes from boron-doped silicon with our existing equipment and facilities [3]. This was a most critical decision because, unknown to us at the time, BN would be found to suffer extreme radiation damage under modest doses of $\sim 5\text{--}10\text{-kJ/cm}^2$ X-rays, while silicon doped with boron did not suffer significant damage

X-Ray Lithography

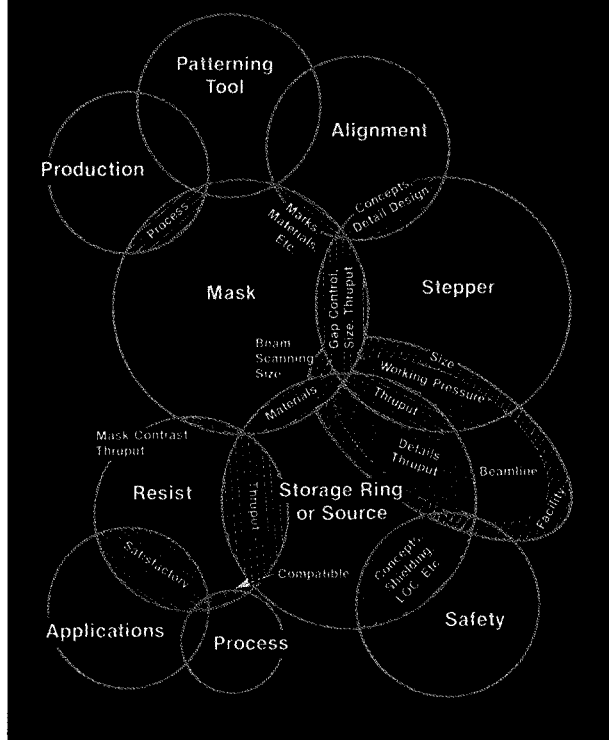


Figure 2

Venn (logic) diagram devised early in the X-ray lithography program, showing that the technology includes many variables, all of which must be considered in every technological decision.

under high X-ray doses. However, silicon membranes were not without problems. They transmit very poorly in the visible light spectrum where our alignment system was intended to work, and they were also, as we initially fabricated them, prone to warpage and thus were not very flat. The problem of poor transmission of visible light by silicon membranes was solved by etching through the silicon substrate and membrane and supporting alignment marks on a polymer film.

We would go on to understand the mask technology and to produce many mask blanks at Yorktown, and, subsequently, to initiate transfer of this technology, in 1987, to the IBM Burlington mask facility, where production has continued to the present day.

Several important problems encountered in mask fabrication and use were mask flatness, Au absorber stress that influenced pattern distortion [4-10], and alignment through a nearly opaque substrate that was also rough on one side. Besides Si membranes, we also developed SiC

and diamond as alternative mask substrate materials [11-13].

My managerial and technical approach, as head of the program, was to understand the technical issues as best I could and then, on the basis of the data, set a direction for understanding the problem more fully and/or accepting a solution we had in hand and proceeding to the next problem. We all realized that in a research and development program there were many interesting diversions to consider, but focus had to remain on the ultimate goal of establishing and demonstrating the key elements of X-ray lithography.

We generally published all our technical findings in a timely manner, withholding only a few proprietary/trade secrets that were unique. Our goal was to make devices to test X-ray lithography, not to perfect a solution to each and every problem. Consequently, we left many issues for later refinement, particularly in the area of masks. The success of our mask process depended on the development of a fairly repeatable procedure coupled with measurements to select good usable substrates for key device pattern levels. All masks were measured for pattern-placement accuracy, and this, along with final flatness, was the bottom-line measurement.

Masks for our 0.5- μ m CMOS device program were fabricated by a self-appointed team consisting of the e-beam patterning tool owner, the device and mask process owner, the substrate plating and flatness process owner, and two lab assistants. This informal team carried out the task of delivering to the device program exposure system, over a one-year period, two complete sets (ten levels each) of masks that exceeded our overlay requirements. This was a remarkable achievement. **Figure 3** shows an example of the accuracy of the overlay of the masks fabricated. It can be argued that this overlay result was good enough for lithography at one generation smaller than our 0.5- μ m device program.

Associated with masks is the lithographic tool used to pattern the masks. I had been intimately connected with development of IBM e-beam vector-scan round-Gaussian-beam lithography tools and had just about finished our latest vector-scan tool, VS-5, at the onset of the X-ray program. It was unique in the vector-scan series because it had 1) a new x - y stage from Yosemite Laboratories, Berkeley, California, which used "Roline" drives that drove the x - y stages in the center and thus minimized the stage yaw; 2) a new computer control system and software; and 3) advanced pattern-generator, registration, and stage-control laser interferometer subsystems. I was convinced that if X-ray lithography were to be successful, we would have to have unlimited access to e-beam patterning of masks. Having just completed an evaluation of vector-scan technology for optical mask patterning, I concluded that we needed our own e-beam system,

which would probably have to be tailored to satisfy the requirements of X-ray lithography. After an analysis of the needs of contending organizations, IBM Research senior management dedicated VS-5 for the X-ray program. This decision was vital to the success of subsequent device programs.

VS-5 was made capable of writing an X-ray mask as accurately as a Nikon 2I optical metrology tool could measure. The device programs we conducted were not compromised in overlay in any way by mask patterning. Device programs were based on 0.5- μm minimum feature sizes, and the VS-5 tool was capable of generating a set of masks with a 3σ mask-to-mask registration (whole set) of $<0.1\ \mu\text{m}$ and probably as little as $\sim 0.06\ \mu\text{m}$. Essential to achieving this overlay were stable electronics and a laser interferometer; a clean room, specially designed and built [14], with a temperature-, sound-, and vibration-controlled environment for the tool; kinematic mounting of the mask substrate [15] in the patterning, measuring, and exposure tools to avoid clamping and induced distortion; and, finally, a very user-friendly, flexible, sophisticated control software system, along with superb operators and engineers. The patterning tool was continually improved, with major and minor enhancements implemented by and in close cooperation with the system operators and e-beam lithography developers.

I realized early in the use of vector-scan systems that system performance in terms of fast writing of fine features over large areas was best accomplished, for research and development needs, by a combination of medium-size field patterning (200–1000 μm) and a precision laser table for stitching of these subfields, with which approach any size mask or chip could be written (our unique proximity connection software was applicable within the subfield and across subfield boundaries) [10]. In addition, we needed better field-emission electron sources than the LaB_6 we were using. With LaB_6 we were unable to achieve a small enough spot size with a beam current adequate for a stepping rate of $\sim 5\ \text{MHz}$. Moreover, for X-ray masks, the X-ray mask team recognized that 25 kV was too low an electron-beam energy for patterning of X-ray masks using single-layer resists. We initiated a development program broken into three phases: 50 kV and 100 kV using LaB_6 , and then, ultimately, a 100-kV thermal field-emitter system [16, 17]. The final system could generate 0.15- μm features with good linewidth control in $\sim 1\ \mu\text{m}$ of resist. Electroplated images also had excellent linewidth control. Since the use of a low-atomic-number substrate caused only low electron backscattering, only simple proximity correction was required to produce vertical sidewalls in the single-layer resist. These characteristics resulted in the use of $\sim 100\text{-kV}$ electrons for additive masks (gold plating) with a thermal field emitter providing $\sim 100\text{--}200\text{-\AA}$ spot sizes with a current density of 1000–5000 A/cm^2 .

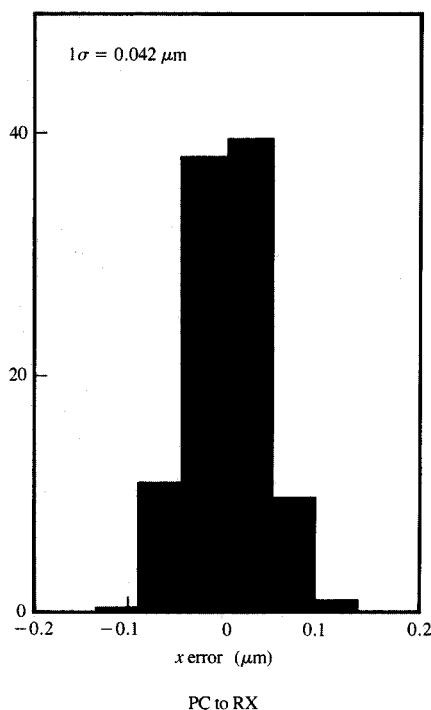
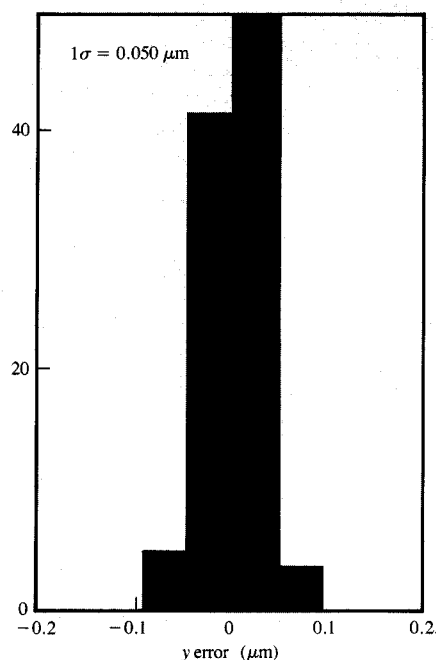


Figure 3

Accuracy of the mask-to-mask alignment for the ten-level 0.5- μm CMOS X-ray lithography test chips was measured using a Nikon 2I optical metrology system, data from which are shown in the example above for the alignment of the polycrystalline silicon wire level (PC) with the underlying recessed oxide level (RX).

- *Mask repair*

It was recognized that X-ray masks would have to be repaired; that is, it would not be practical to produce a mask that did not have a few clear or opaque defects. We needed to initiate a small but viable research effort focused on how to repair X-ray masks as well as how to inspect them, both before and after repair. Because X-rays interact with substrates much differently than do visible light or electrons, one thought was to inspect X-ray prints of the masks and look for repeating defects [9]. For mask repair, a focused ion beam effort was initiated under A. Wagner. This program established the principles, tools, and process for repair of both clear and opaque mask defects in gold-plated (additive process) absorbers on thin single-crystal silicon, SiC, and diamond membrane substrates* [18].

- *Exposure system sources and beamlines*

In 1978, Brookhaven National Laboratory (BNL) embarked on the fabrication of the National Synchrotron Light Source (NSLS), comprising two storage rings, one for hard X-rays and one for soft X-rays, the latter known as the vacuum ultraviolet (VUV) ring. In October 1980, Grobman and I went to Brookhaven to take a look at the early construction phase of the VUV ring. The dipole magnets had just been placed on the floor, and plumbing/cabling trays were about to be installed. The user hall was empty. A map of the ring illustrated a few uncommitted ports. Grobman's plan called for piggybacking on Port U8, a surface science port being implemented by D. Eastman of IBM Research. We then met with Eastman to coordinate floor space and access to the U8 port. I felt that the space I had been allotted was inadequate for a stepper, and suggested to Grobman that since it would be next to impossible to implement an X-ray lithography stepper on U8, we ought to ask for a separate dedicated port. The problem was obtaining funding to implement a port with a front end and a beamline. The front end, placed physically between ring port and beamline, comprises safety devices to protect the storage ring from beamline vacuum failure. This consists of both a fast valve and a radiation shield. Grobman subsequently got Port U6 assigned for lithography and induced DARPA to assist with beamline development and use. This turned out to be a salient step along the road to testing X-ray lithography: Port U8 became highly congested and, in retrospect, we did indeed need all the space around Port U6 for a temperature-controlled clean room for the stepper.

Thus U6 became the source of our X-rays. **Figure 4** shows the BNL VUV ring in 1987 with many science beamlines and the IBM beamline and clean-room hutch

installed. It should be noted here that we also had a water-cooled "conventional" X-ray source at Yorktown [19], but we were convinced that the maximum output one could ever expect from such a source was ten to a hundred times less than that required to expose resists suitable for the thick, slow, robust resist materials required in device manufacturing. Consequently, we needed a powerful X-ray source.

Grobman began to design the beamline on the X-ray port at Brookhaven [20], shown schematically in **Figure 5**. I obtained assistance for him from our Central Scientific Services Department at Yorktown for drafting and basic mechanical design, and in November 1982 we exposed our first high-resolution mask on Port U6. The mask had been patterned on VS-5. Many studies were subsequently made on Port U6 of resist characteristics while we developed an X-ray stepper suitable for device fabrication [21].

The beamline on Port U6 was unique in the field of synchrotron-generated X-rays in that it was essentially a large pipe sealed by a thin (18- μ m) Be window membrane spanning a 2-in.-diameter circle [22, 23]. The potential for a vacuum failure was great; should that happen, the ring would fail. From the onset, our beamline had many safety features built in; as I recall, we only brought the ring down once, and this was caused by a maintenance operation/operator error involving bypassing the safety interlocks.

As the stepper we had designed was nearing completion by the vendors, we designed and had similarly constructed a triangular-shaped, temperature-controlled, controlled-access clean room to house the X-ray stepper and electronics shown in **Figure 5**.

Our 13-year association with BNL during the X-ray program gave us a unique opportunity to become familiar with key elements of storage rings, beamlines, and the operation of such a facility. We purchased and installed a trailer at BNL for our staff and had from one to three people located there for periods of one to five years. Many people commuted to BNL, 90 miles from the Thomas J. Watson Research Center, on a regular basis, with one Researcher making 104 trips in one year of the device program! An X-ray group we had formed in 1987 in the General Technology Division (GTD) at East Fishkill to receive the results of the Research X-ray lithography program began to set up a second beamline (U2) for X-ray lithography at Brookhaven, both as a learning experience and to provide increased exposure capacity for device development programs.

- *Stepper*

At the outset of the X-ray lithography program, it was universally recognized that we would have to develop a wafer stepper to perform at the end of a beamline. There were no vendors of ready-made equipment for X-ray lithography with an X-ray stepper for sale. There was

*A. D. Dubner and A. Wagner, "The Role of Adsorption in Ion Beam Induced Deposition of Gold," IBM Thomas J. Watson Research Center, Yorktown Heights, New York, unpublished work.



Figure 4

By 1987, the IBM lithography beamline and clean room had been installed amidst numerous science beamlines around the vacuum ultraviolet (VUV) ring of the National Synchrotron Light Source (NSLS) at Brookhaven National Laboratory (BNL), Upton, New York. Lithography clean room with stepper is at right (arrow).

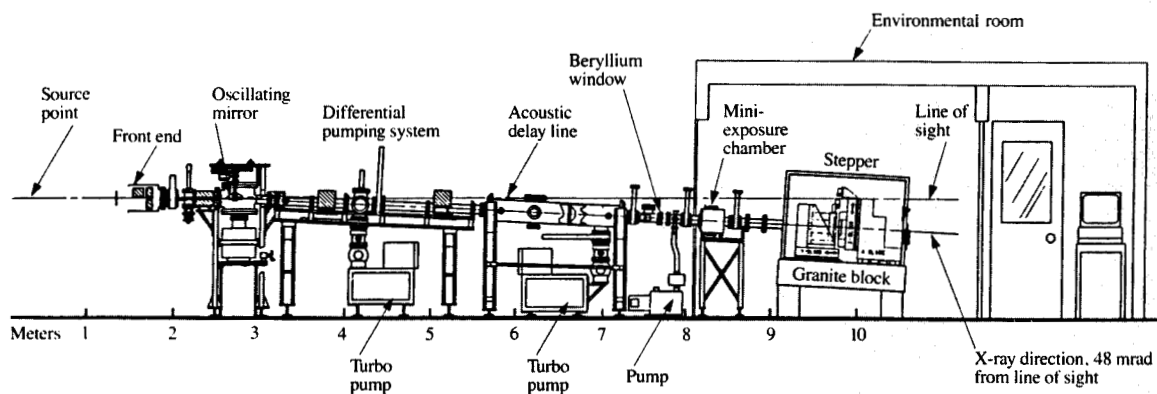


Figure 5

Elevation view of the IBM beamline at NSLS, including the beamline controls and the stepper at the end of the beamline.

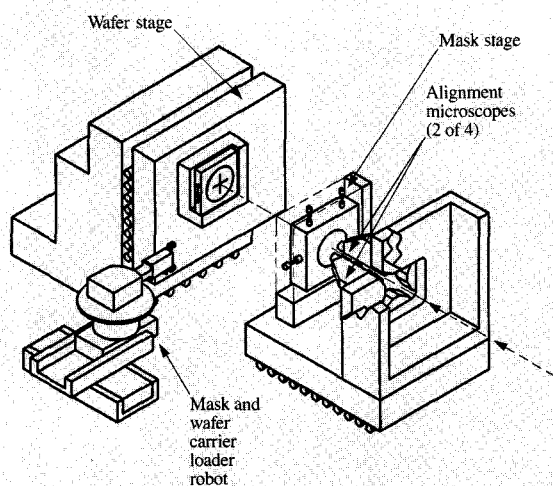


Figure 6

Wafer-holding and -stepping stage and gap-setting/mask-and-alignment system stage designed for the X-ray exposure system at BNL.

neither a suitable stepper in existence nor any in development in 1980. Our central goal was to obtain a stepper/aligner that could be used to conduct the device-making experiment necessary to establish the viability of X-ray lithography. The stepper had to work, but it was to be a development- rather than a production-type system. The program called for holding a $3\frac{1}{4}$ -in. wafer in a nearly vertical plane. Most lithography tools at that time, whether optical, e-beam, or conventional X-ray, held the wafer in the horizontal plane. An exception was the Perkin-Elmer 1:1 ring-field projection equipment, which scanned mask and wafer together, held vertically, through a slit illumination system on a cushion of air. Here was an example that it could be done!

Grobman calculated that the mask had to be heat-sunk to the wafer via a thin film of He gas. For proximity printing of $1\text{--}0.5\text{-}\mu\text{m}$ mask images, it was also computed that the mask/wafer gap should be less than $100\text{ }\mu\text{m}$, probably $40\text{--}50\text{ }\mu\text{m}$, so that the gap would be suitable for proximity printing and yet wide enough so that mask and wafer would not accidentally collide.

A stepper must serve many functions: holding masks and wafers; moving the wafers with respect to the mask; providing the means to align masks and wafers with each other; exposing a mask pattern onto a wafer; exchanging masks and/or wafers; and terminating the beamline as it absorbs the thin line of radiation present at this stage.

Our first thoughts on the stepper were to have air-bearing-type stages inside a large chamber that would be kept at a pressure of about one-third atmosphere. As a precaution against beamline Be window breakage, we did not wish to go to a full atmosphere of pressure. A specification for the stepper was composed, and a vendor was selected to build the system. About nine months into the vendor program, it became clear that the firm was in financial trouble and would be unable to supply our X-ray stepper. Quickly we began to search for a vendor who could build this one-of-a-kind system. A new vendor was located, but they did not possess air-bearing technology of the kind required, so we built the system with more conventional crossed rollers and V-way stages. This system was delivered to Yorktown in February 1983, about a year later than we had planned, largely because of the failure of the previous vendor. The stages of this stepper had 7 in. of travel, and the standard wafer size at IBM was, by this time, 5 in. The stage system used laser interferometers to couple wafer and mask stages together. It was gargantuan, measuring five feet square and about six feet high, and weighing in at nearly three tons. To this basic x - y stepper we had to add an alignment system and mask/wafer holding-and-exchange devices. **Figure 6** illustrates the wafer-holding and -stepping stage as well as the gap-setting/mask-and-alignment system stage.

Masks were held in an adjustable carrier that allowed prealignment of the mask with a reference system so that the alignment marks would be within capture range of the alignment system. This carrier was kinematically mounted in the stepper on a unique flexure stage that provided minute translation and rotations for alignment of mask with wafer. The alignment stage is moved by piezoelectric motors, which have motion feedback sensors and, because all movements are accomplished with flexure structure, motion resolutions of the order of $0.01\text{ }\mu\text{m}$ are attainable over a range of $\sim 5\text{ }\mu\text{m}$. We designed a small robot that grasped and placed the mask and wafer carriers on their respective stages with better than $0.25\text{-}\mu\text{m}$ repeatability.

Holding the wafers in the X-ray stepper was a challenge, because the wafer had to be held in the vertical plane. The pressure in the stepper chamber was less than an atmosphere—typically about a one-third atmosphere of helium—not enough to use a classic vacuum chuck. Also unique was the process by which one wafer was exchanged for another. Our solution was to make a combination wafer chuck—a vacuum chuck to flatten the wafer at one atmosphere—and then, using electrostatic principles, to hold the wafer to the wafer carrier flat and rigidly. This worked well because electrostatic forces are inversely proportional to the gap between mask and wafer. The chuck was fabricated from a circular disk of silicon ~ 1 in. thick. A pin pattern was etched into the silicon, and the whole Si surface was coated with thick SiO_2 (silicon

oxide). The wafer was contacted on the back side by a pin plunger through the chuck silicon base. This hole was also a means of pulling a vacuum on the chuck. This combination chuck solved both flatness and holding problems [24]. The silicon vacuum/electrostatic chuck was mounted in a carrier, made adjustable for prealignment. When a wafer was loaded into the stepper, it was first prealigned on this carrier; then the wafer, chuck, and frame were placed on the stepper stage.

A prealignment subsystem independent of the stepper was fabricated to initially prealign both masks and wafers in their respective carriers prior to insertion into the X-ray stepper. Prealignment to within $\sim 1 \mu\text{m}$ was required so that the alignment system could capture the alignment marks.

The stages in the stepper were made from granite, and all alignment and wafer-mounting hardware was fabricated from a special high-nickel-based cast iron with low coefficient of expansion. Linear electric motors moved the x - z axis of the stepper. Because the chamber was backfilled with He gas, the He-Ne laser interferometer needed no compensation for atmosphere effects, since the index of refractions at $6328 \text{ \AA}$ for He is nearly 1.0. Hence, the He gas provided not only a low-absorption environment for the X-rays, but also a nearly vacuum equivalent for the laser interferometer linking the wafer stage to the alignment stage support frame, in addition to the necessary medium to heat-sink the mask to the wafer. This latter capability is very important, because with a synchrotron one can expect X-ray power from 1 to 50 W down a beamline.

● Alignment system

Historically, alignment of masks with wafers has been one of the major problems of all lithography systems. Alignment for X-ray proximity lithography posed special challenges. Masks and wafers are not in the same plane, but are separated by $20\text{--}50 \mu\text{m}$. Potentially, a mask area greater than 1–4 inches square would be desired. There was very limited space for alignment hardware, and there were no working and proven alignment systems in existence that could easily be extended for X-ray proximity lithography.

Initial responsibility for the basic alignment system rested with J. Wilczynski. He had recently designed and installed a dark-field system on a prototype $5\times$ optical stepper that had been under construction for a number of years, and this system appeared to be implementable for X-ray lithography. We had some unique obstacles to overcome, such as focusing on masks and wafers that were in different planes.

My approach was to set a basic ground rule that the alignment system should meet two requirements: First, alignment information from mask and wafer should be collected in real time, essentially simultaneously (i.e., not

first focusing on mask and collecting data, then physically moving alignment head and refocusing on wafer). I was worried that movement of the alignment head could distort the system, and that such movement would take time and thus would affect throughput and also introduce a time lapse in seeing where mask and wafer are relative to one another. Second, alignment of wafer with mask should be measurable at any time, even during exposure. (Some early commercial optical steppers required moving the wafer in order to find out how well the mask was aligned with the wafer. This was not an attractive feature: To misalign a system in order to see if it was aligned correctly did not seem judicious.) Because of the vital importance of alignment in layer-to-layer overlay, it was critical that a new entry such as X-ray lithography be able to align very well and, if necessary, to do so during the exposure process in order to minimize final overlay errors.

The technical goal set for the alignment system was, therefore, to focus simultaneously on mask and wafer and to scan mask and wafer marks together in either the x or the y plane. The basic principle was to arrive at an alignment null when the mask was aligned with the wafer.

A decision had to be made between bright- and dark-field systems and also between those using white incoherent light and those using laser light in one form or another. It was always necessary to reevaluate our goal of getting to the point of being able to test X-ray lithography on fully integrated device runs and balance that goal and the work of each subsystem against the overall project goal. We could not afford to make each subsystem optimal and high-risk; we had to be prudent in our selection of options and directions. To meet the technical objectives outlined above for the alignment system, we first chose a dark-field approach as providing the greatest possibility of being able to see the alignment marks in any of the typical semiconductor layers/process steps. Second, on the basis of positive experience with relatively simple incoherent illumination in dark field on the prototype optical stepper, incoherent light was selected. Third, to focus on mask and wafer without moving the optical system, we used an optical approach that caused the wafer alignment marks to be imaged in front of the mask by the mask/wafer gap of $40\text{--}50 \mu\text{m}$ [25]. This was accomplished by using an $\sim 1.1\text{-cm}$ -long glass focus shifter cemented to the mask/wafer reference mask. Fourth, the scanning of each axis separately, and of mask and wafer alignment marks together, was achieved by using thin ($\sim 1\text{-mm}$) glass plates in the alignment microscope optical path; these were caused to oscillate a few angular degrees by galvanometer motors: one each for the x and the y axes. The alignment system is described in detail in [25]. **Figure 7** illustrates a finished single-alignment microscope, as well as alignment principles including the focus shifter glued to the alignment reticle.

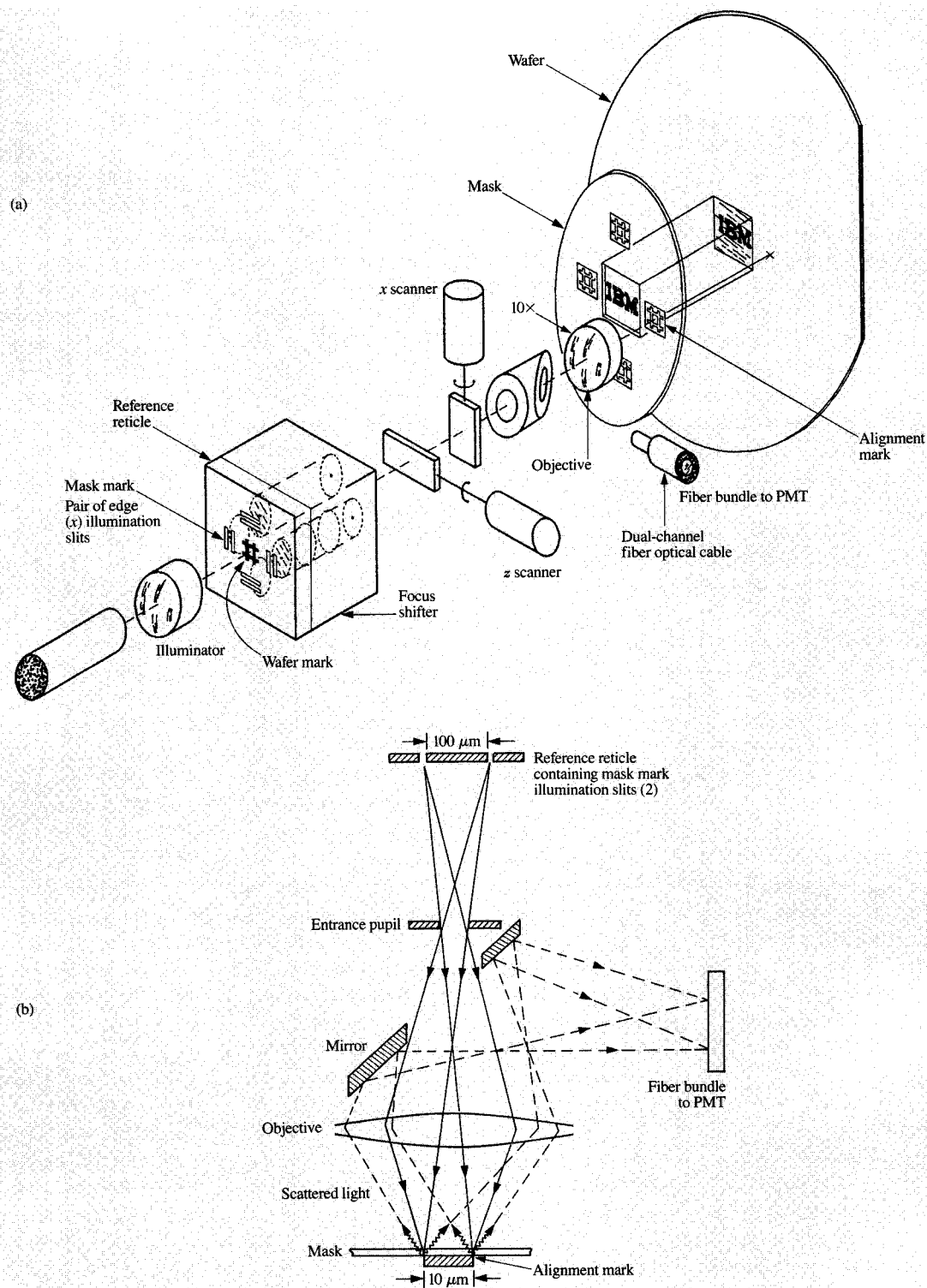


Figure 7

X-ray alignment system at BNL: (a) principal alignment mechanisms; (b) optics. One of four alignment microscopes is shown in exploded view in (a), and the optical ray paths for a single set of illumination slits are shown in (b).

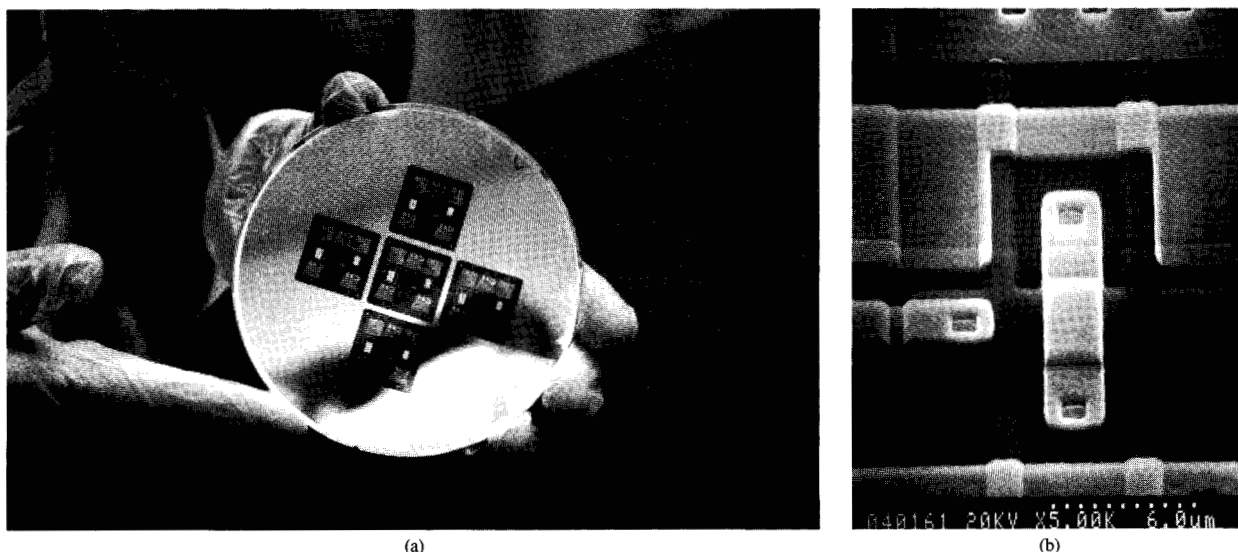


Figure 8

A very large (one inch square) chip fabricated for the project: (a) actual device wafer; (b) closeup of features.

Four alignment microscope heads were mounted around the exposure window on the mask. Spacings of the alignment microscopes on either axis were adjustable so that the alignment marks could be located in the kerf area of the wafer. Scattered light from the alignment marks was detected by photomultiplier tubes (PMTs), and closed-loop software generated x - z and θ correction signals for the piezoelectric/flexure stage on which the mask resided. Many technical/fabrication problems had to be solved before the alignment system could be made to function, including 1) using fiber optics to couple light to and from the alignment microscopes; 2) design/fabrication of the $1\text{-mm}^2 \times 1.1\text{--}1.2\text{-cm}$ -long focus shifter and prevention of high-voltage breakdown of photomultiplier tubes in one-third atmosphere of He; and 3) basic signal acquisition and analysis accomplished via a PC-based control and software system. (It should be noted that the PC was not on the market until a year after the X-ray program began. We first started with Series/1TM computers, but after my first look at the PC in August 1991, we terminated the Series/1 effort and based the stepper control system on the new IBM PC.)

The overall stepper was a combination of IBM and vendor designs and technology. It was the first X-ray stepper to be used to fabricate complex CMOS devices, circuits, and test chips using synchrotron radiation [26].

• Device program

In 1984–1985, three to four years after we initiated the X-ray lithography program, we embarked on its most

ambitious and most necessary phase: complex device fabrication. The success of this phase would require integration of all of the key elements: the synchrotron source, beamline, stepper/aligner, masks, resist-coated wafers, and a device test vehicle. At the beginning of the program we had targeted this technology for $1\text{-}\mu\text{m}$ dimensions. By the time we had attained the ability to do a real device program, it was clear that $1\text{ }\mu\text{m}$ would not suffice; rather, $0.5\text{ }\mu\text{m}$ would be required—two memory generations beyond our target. This would be difficult because masks, stepper imaging, and patterning all had to perform at twice the level for which the system had been designed. With the stepper operational at Brookhaven and a supply of a few mask blanks on hand, we initiated a CMOS device program with preliminary MOS results possible after four mask levels, CMOS results available after eight levels, and, if we ever got that far, a total of ten levels, including a second-level metal, for a full test chip. The plan was that the last two levels would be done optically. All levels would use original alignment masks put down at the “zeroth” level. Our experimental chip would be about one inch square, with $0.5\text{-}\mu\text{m}$ ground rules. At this time the first 1Mb chips with $1\text{-}\mu\text{m}$ ground rules were nearing final release to production. We were trying to fabricate a very large chip, one inch square [see photo of actual device wafer, **Figure 8(a)**—about six times the size of chips in manufacturing, with ground rules two generations ahead of business-as-usual manufacturing, using a *totally* different technology with $2\text{-}\mu\text{m}$ -thick membrane masks, X-rays, and a prototype stepper/aligner.

1988 X-ray Lithography Activity at BNL U-6

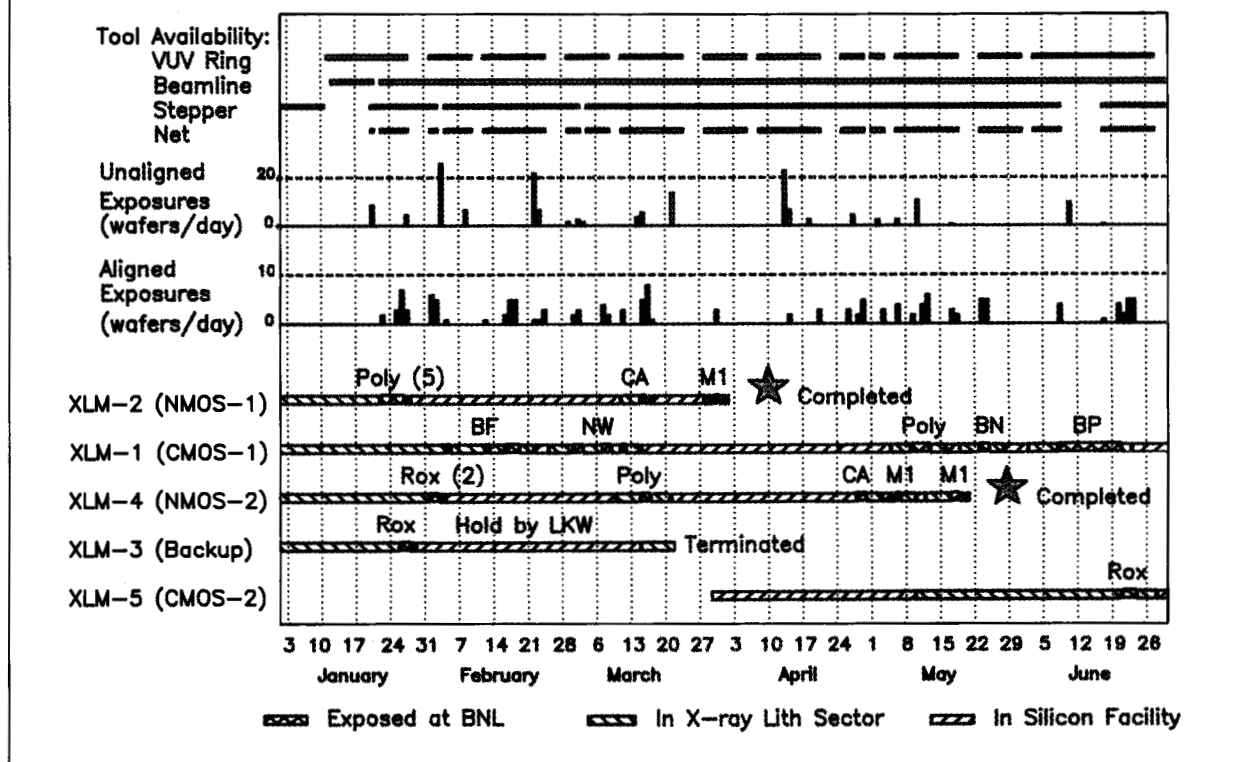


Figure 9

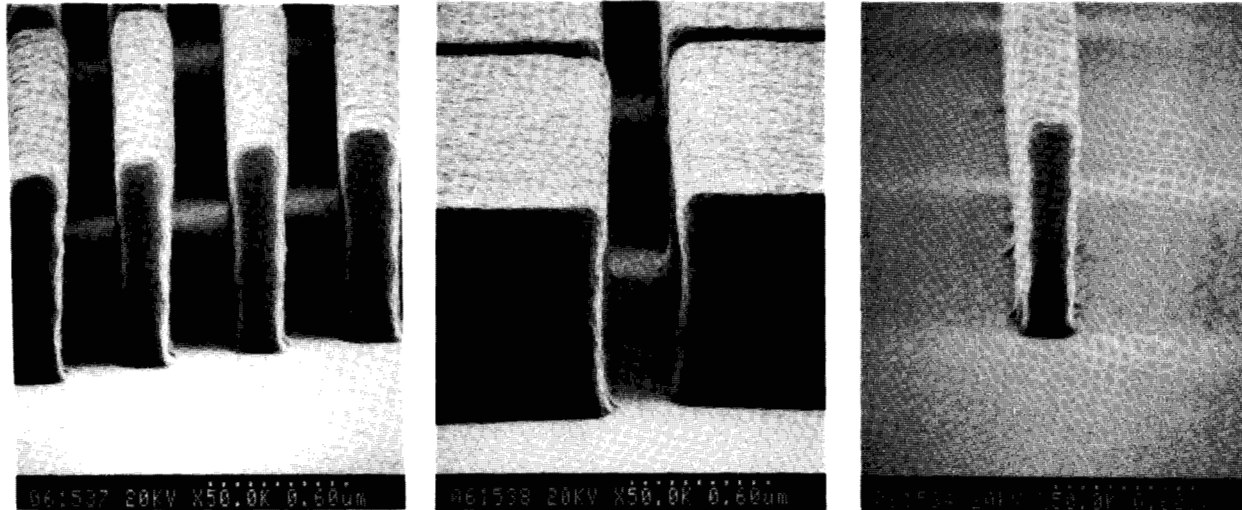
AND chart showing location of problems and how quickly they were solved, including ring, beamline, and stepper availability; net system availability, and what the exposures were for—what level process was being tested or developed or what device level was being exposed.

As a team of about ten people, over a two-year period, we fabricated two full sets, with ten masks in each set, and made improvements in stepper/carrier/e-beam clamping of masks, resist characterization, and stepper/aligner software. On April 1, 1987, we completed our first four-level MOS device. During the next year we completed the next four levels and obtained striking CMOS results with exceptional linewidth control; observed that low-atomic-number defects (e.g., carbon, Al, Si), in the 0–2- μ m size do not print [27]; and achieved excellent mask-to-mask overlay [8, 26]. We had fabricated eight-level CMOS chips, with 0.5- μ m ground rules, over one inch square [28–30], the probable equivalent of a 64–128Mb memory chip. That was not all. The process group we were working with asked us to do the last two levels by X-ray, because they had observed in the previous eight levels that subsequent processing of X-ray-exposed resist images was easy and robust. Images were clear and crisp [Figure 8(b)]. We made the last two masks and finished the device run.

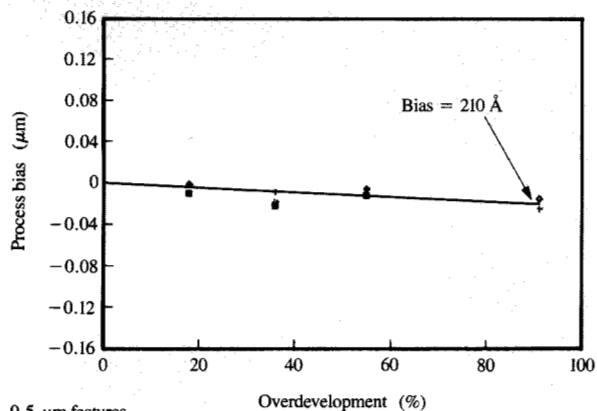
We had made complex, fully scaled CMOS devices with 0.5- μ m ground rules before our optical counterparts had reached the same level using a long-established technology. Our yield was also acceptable: not 100%, but acceptable. The principal goal of the X-ray program had been achieved. (During this device program we also initiated transfer of mask-making for the corporation to the IBM mask-making facility in Burlington, VT.)

One technique we used to manage this very ambitious and difficult program, with the added complication of the lithography section being located about 100 miles from the central laboratory and process line, was the development of the Wilson AND Chart, illustrated in Figure 9. Each Friday afternoon I held a project progress working meeting. Each key element of the project was presented—achievements and problems. It soon became apparent that many difficulties were arising with respect to exposures: for example, getting process work from Yorktown to Brookhaven and getting subsequent device exposures from

X-ray-exposed TNS
0.25 μm , 40- μm gap

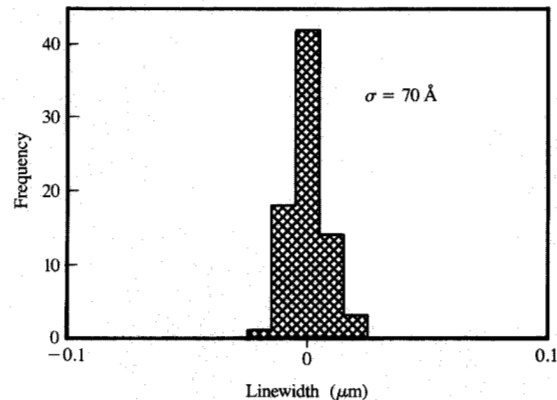


(a)



0.5- μm features
TNS resist
X-ray-exposed at BNL storage ring

(b)



(c)

Figure 10

Image quality: (a) 0.25- μm images of isolated lines, spaces/gaps, and equal-line pairs at equal doses of *same mask/image exposure*, in thick single-layer resist; (b) process latitude (linewidth change with overdevelopment), indicating why we experienced extreme robustness with X-ray-exposed resist; (c) critical image size control of ~ 70 Å.

Brookhaven back to Yorktown during the window of resist lifetimes (which were a function of humidity, temperature, and time); X-ray beam availability; personnel scheduling; and stepper up-time. The AND chart displays how quickly we solved these and other problems: It showed (a) ring, beamline, and stepper availability; (b) net system availability (the conjunction, or ANDing, of ring, beamline, and stepper—divided into the X-ray beam-test/unaligned exposures and aligned/calibrated

exposures in numbers per day); and (c) what these exposures were for; i.e., what level process was being tested or developed or what device level was being exposed. From the AND chart, which was updated weekly, we could see where problems remained, as well as how effective we were at making use of the X-rays, stepper, beamline, etc. Our program progress was remarkable; during the device effort, only twice was there any need to rework a lithography level, and this was due

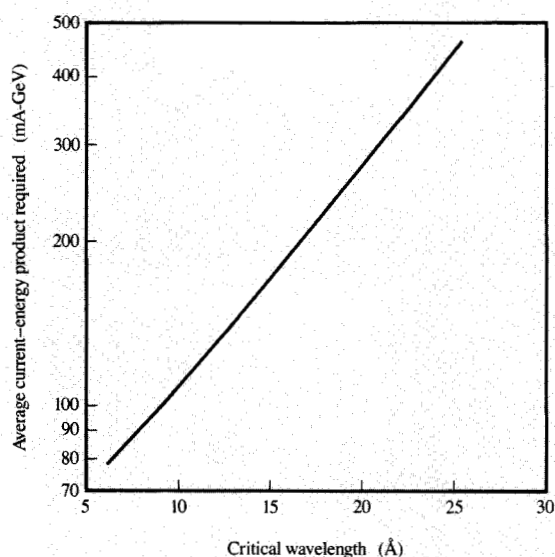


Figure 11

Specifications needed for the ring X-ray output flux, expressed in terms of electron energy, electron current, and critical wavelength of the emitted radiation, to supply a flux of 100 mW/cm².

to outdated resist. (On the AND chart in the parentheses following a level is the number of times a level was exposed. Only two levels had to be exposed more than once.) I know of no other lithography process that can claim such a robust resist process. The device program produced many results, but I would like to emphasize particularly the performance of resist as an image-transfer mechanism in X-ray lithography: Note the image quality illustrated in **Figure 10(a)**, showing 0.25- μ m images of isolated lines, spaces/gaps, and equal-line pairs at equal doses of *same mask/image exposure*, in thick single-layer resist. This is a process unmatched by optics or e-beam. Equally remarkable is the lack of image bias of less than 200 Å at 100% overdevelopment! **Figure 10(b)** shows why we experienced extreme robustness with X-ray-exposed resist; **Figure 10(c)** shows critical image size control of ~ 70 Å. Simply put, no other lithographic process, be it optics, ions, or electrons, can match this image transfer process for process control in thick resists.

Perhaps it would be instructive here to review where others were in development of X-ray lithography at the time we completed our historic eight-level CMOS chip. Many companies had small X-ray lithography efforts, but none had built a device of more than 2–4 X-ray levels, had a workable mask technology, or were as active as we were on a beamline source of X-rays. Commercial systems

using conventionally generated X-rays were in early development and manufacture. The Fraunhofer-Institut in Berlin was the first group to seriously explore X-rays for lithography using synchrotron radiation, and the Fraunhofer-BESSY Group was building a compact storage ring [31]. NTT had the two storage rings at the Atsugi-Shi site in Japan [32], and AT&T had a conventional X-ray source program [33, 34].

IBM synchrotron

For X-ray lithography to be viable in IBM, we needed to explore acquiring our own X-ray source. As with masks, this too was pursued during the device program implementation. Early in 1982, Grobman and I were starting to learn about the physics of synchrotrons. Our interest in a synchrotron ring for IBM was kindled by reports from Munich of the design of a tabletop machine called Kleine-Erna. Our consultants did a few simple preliminary designs largely exploring the footprints of different dipole configurations: size, fields, and number of magnets. In October 1983, I hosted an SPIE meeting at Brookhaven National Laboratory, where these topics were presented and discussed [35]. At this meeting we encountered Peter Williams of Oxford Instruments, a superconducting magnet supplier, who later shaped our project significantly. Having been asked to direct the X-ray project in June 1983, I was beginning to evaluate where we were on the key elements of the system and, after the Brookhaven X-ray meeting, concluded that we needed to examine a ring for IBM more thoroughly. We began this serious inquiry by visits to established rings in this country and in Europe. Perhaps not being part of the synchrotron establishment was beneficial: We could ask questions and find out what really made rings *good* and what did not, as well as who the real experts were. Armed with this information, we asked ourselves what the specifications for the ring should be. The key was to establish the flux needed at a port, and the spectrum of the X-ray radiation [23]. John Warlaumont reduced this to a single graph, **Figure 11**, relating current required in a ring vs. critical wavelength for a given flux output at a standard port. As an invited participant at numerous X-ray lithography workshops and conference sessions, and a “legitimate industry” representative on lithography, I was invariably asked “What should a ring for industry be?” My answer was this: It should fit on a truck; plug into a wall socket; be reliable and available to operate 20 out of 21 shifts per week; have sufficient average output capable of sustaining a stepper throughput of more than 30 wafers per hour using an insensitive (having a sensitivity of ~ 100 mJ/cm²) X-ray resist; be capable of being debugged/commissioned and assembled at the vendor, shipped intact to an IBM site, and rendered operational in a reasonable time at full specifications.

Developing a ring for IBM was, to say the least, an ambitious project, such as is usually done only by government-sponsored laboratories with vast direct and indirect resources. As we began to consider a number of vendors for this project, we were seriously counseled by synchrotron leaders at various laboratories that it would not be possible for us (IBM and vendor) to design, build, commission, and operate a ring! I am glad we did not take this advice too seriously. Not being ring experts ourselves, but perhaps recognizing that there are many ways to achieve a given X-ray flux from a synchrotron, we elected to generate a basic set of specifications that essentially characterized the flux we needed and the general operating performance of the ring we were interested in, rather than detailed design objectives and specifications. Further, we decided to evaluate several potential vendors—teams of industrial and governmental laboratory people—with paid design studies. We contracted with several such teams to design a ring to our general *performance* specifications, using their technology and intellectual insight on how best to achieve our goals. These IBM-paid design studies explored the physics of the ring, the mechanical, vacuum, electrical, rf, performance, safety, and cost aspects of the vendor's design. The studies became a basic element for a response to a formal request for quotes (RFQ). This work was completed in December 1985.

On one of many flights back to New York after a vendor dipole magnet visit to Europe, Warlaumont and I were struggling with how we would measure the progress of a vendor building the ring, should that ever happen. We hit upon what became a fundamental ingredient of the contract: inclusion of a series of checkpoints whereby we would pay the vendor, per the fixed price agreements of the contract, only when requirements that we could measure were met: e.g., vacuum, $X\%$ final injection current, $X\%$ final stored current.

While we were readying the X-ray stepper at Brookhaven for device work, exploring the ring option, and making X-ray masks, J. Matisoo and I were also making the rounds of IBM sites and HQ management, keeping staffs and management posted on both our progress and our directions. In the spring of 1986, a formal RFQ for our potential ring vendors was generated, allowing us to sharpen our focus on the need for a partner in semiconductor manufacturing. This next step comprised a major change in the character of the program: inclusion of the IBM General Technology Division. Until then, the program had existed exclusively within IBM Research. (Although we had GTD assignees on resist and mask technology resident at Research and a good dialog existed between our divisions, there was no formal interdivisional program.) This new partnership commenced in July 1986; added to the program were R. Hill from GTD and four people from his area, as well as a new Ph.D. hired to

handle the accelerator storage ring physics. With support of GTD behind us and the ring design studies completed, we drafted specifications for a proposed ring for IBM, and Research Purchasing issued a formal RFQ for the ring from three vendors. I organized a whirlwind visit to all three. Our team was unusual; it was made up of Warlaumont and myself from the technical side of IBM Research, R. Glowina, a buyer, R. Schall, a superconducting magnet expert in IBM Instruments Division, R. Hill and G. Lesione of GTD, and two representatives of an external lithography tooling company we had asked to join us and evaluate the tooling design and the viability of the vendors' manufacturing capability. We visited six institutions in five days, all in Europe.

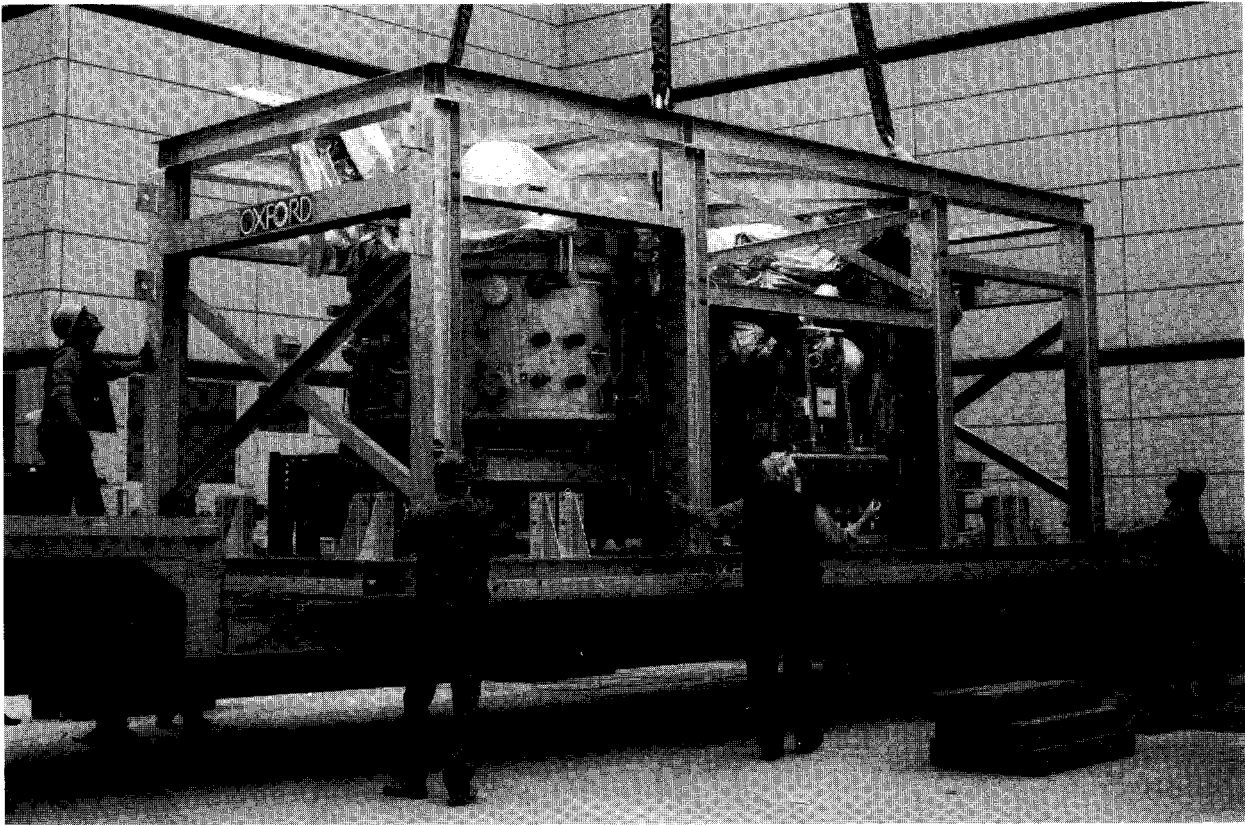
The designs that the vendors had evolved were all different in detail but similar overall: Each was based on a dipole superconducting magnetic design. By early fall 1986 we had detailed responses to our RFQ, including prices and delivery schedules. We next convened a team of external experts to study the physics of the ring proposals and a group of internal people representing different aspects of tooling and manufacturing to evaluate all other aspects of the proposals. Our selection was made, and on March 17, 1987, the contract was awarded to Oxford Instruments, represented by Peter Williams, the person who had unexpectedly appeared at our SPIE Brookhaven Conference in 1983.

Oxford proposed a superconducting dipole system with a cold bore. The magnet turned out to be difficult to construct but had excellent performance. The Helios 1 ring was completed and commissioned at Oxford, England, in October 1990. During the design and building of the synchrotron we visited Oxford and the Daresbury team every four to eight weeks over a period of three and a half years. The ring was shipped to IBM in March 1991 and arrived at East Fishkill on March 29, 1991. It fit on a truck, as shown in **Figure 12(a)**, and we slid it into ALF that same day [**Figure 12(b)**]. **Figure 13** shows the ring from one end, with its 16 ports being readied for attachment of beamlines.

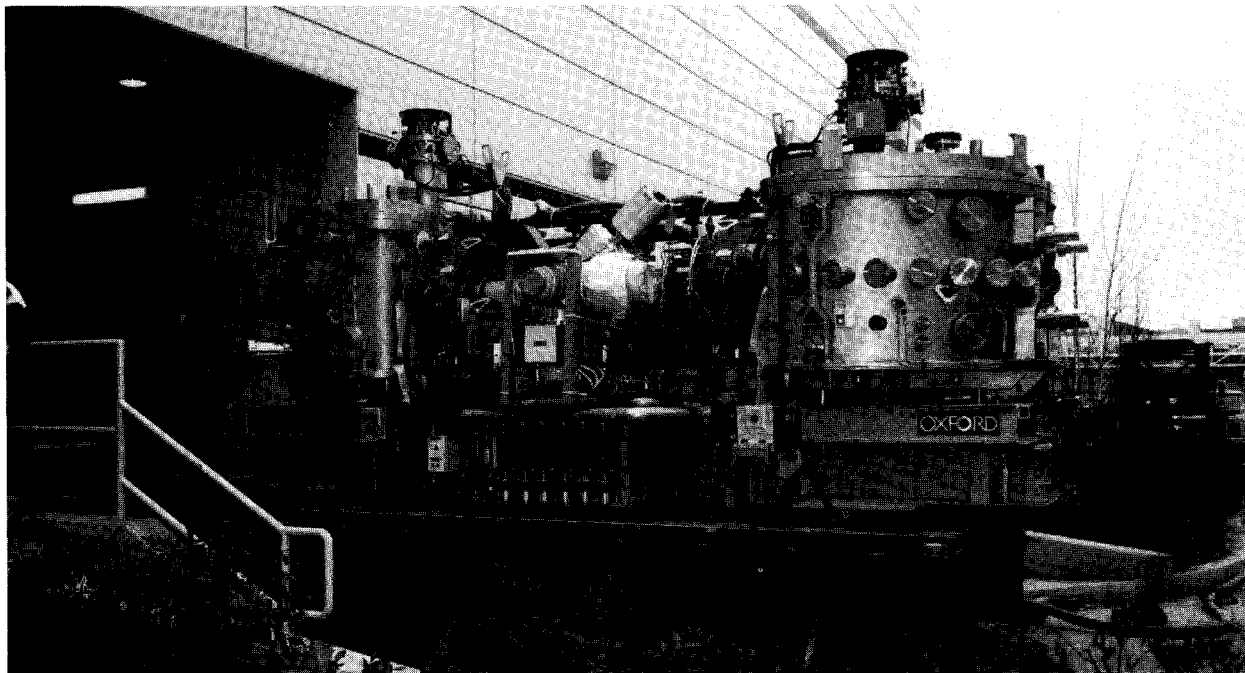
The first beam was stored on or about May 20, 1991, and final specifications were met in January 1992. Our goal had been met and, in fact, exceeded, because the ring performs beyond specification [36]. Critics who thought design alone would not work were wrong. IBM and Oxford as a development team commissioned the Oxford ring in record time and with a very high level of performance.

Advanced Lithography Facility

In the summer of 1987, after the ring was on order from Oxford Instruments, we began the process of acquiring a building to house the storage ring. Research, East Fishkill, and the IBM Real Estate and Construction Division gathered an informal team that started at first principles



(a)



(b)

Figure 12

The ring was shipped to IBM in March 1991 and arrived at East Fishkill on March 29, 1991. It fit on a truck (a) and was slid into ALF that same day (b). Part (b) reprinted with permission from [36].

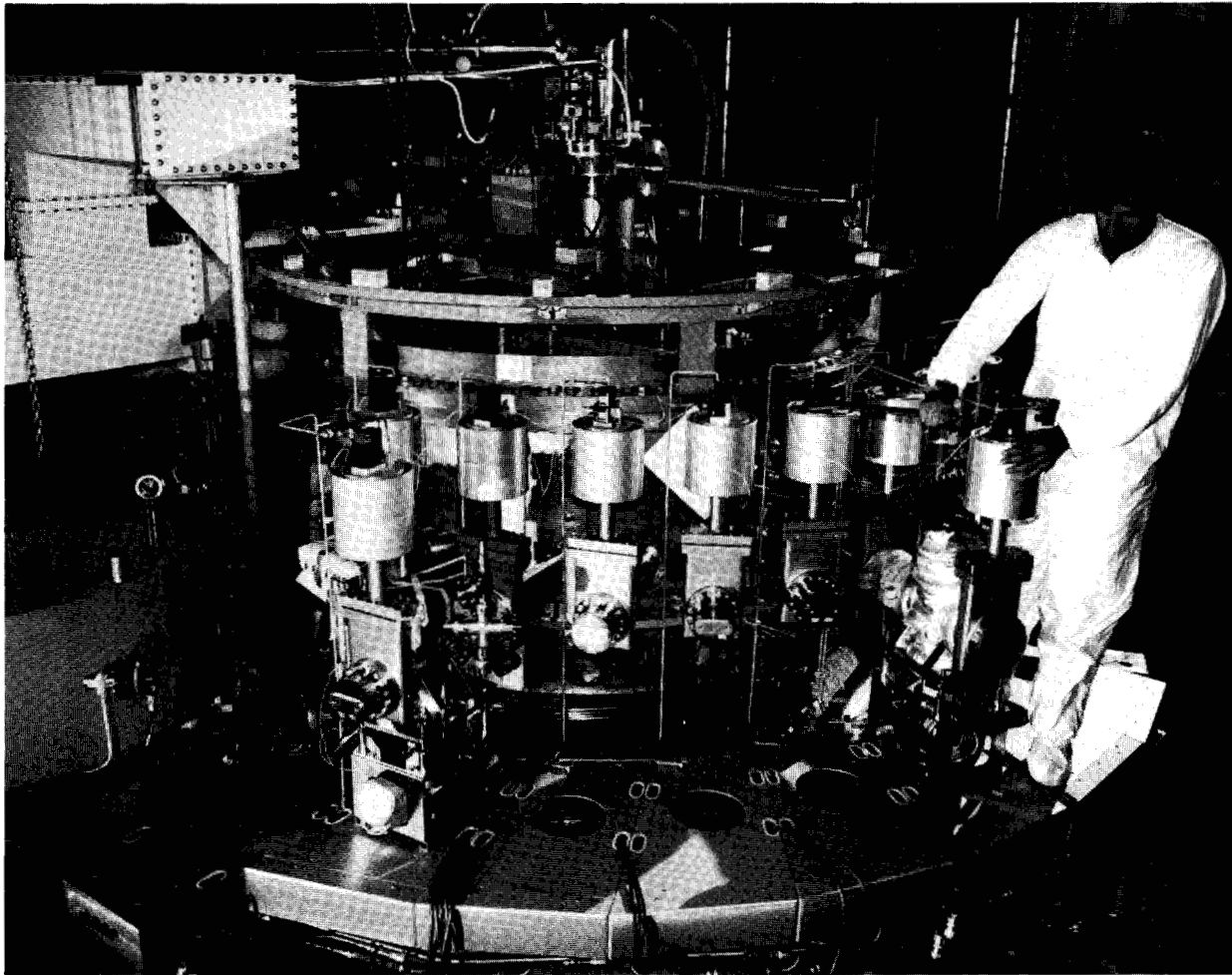


Figure 13

The ring installed in ALF, seen from one end, with its 16 ports being readied for attachment of beamlines.

and began the project of layout concept and radiation evaluations, considering cost vs. performance issues, and developing a schedule to match Oxford's progress. The Advanced Lithography Facility (ALF) [37] met all technical aspects of the project, and it was on schedule and under budget.

Integration

By 1988, the primary elements of X-ray lithography had been established [16, 26, 28–30, 38–40]. Our research effort had provided the central planning function for the program from its inception in the late summer of 1980 until 1987–1988, illustrated in **Figure 14**. To a large extent, we have met the goals of this integration plan: the ALF, ring, masks, etc. are at a manufacturing stage today. We had executed a very complex device program at Brookhaven

on the VUV ring, which tested the research masks, stepper, resists, and beamline. Our counterparts in GTD, who had been organized into an X-ray lithography department, then had to acquire first-hand experience with X-ray lithography in preparation for ALF, the Oxford ring, and all the other aspects that follow. The advanced mask laboratory in Burlington was fabricating all of our mask blanks by late 1988, thus establishing such a supply for IBM.

The program for an X-ray stepper was taken over by R. Hill and his team in GTD East Fishkill. We encouraged them to seek short- and long-term solutions for both a prototype and a manufacturing stepper. GTD needed experience using X-ray lithography and elected, with our encouragement, to set up a second beamline at BNL to test a Suss stepper and provide an exposure facility for

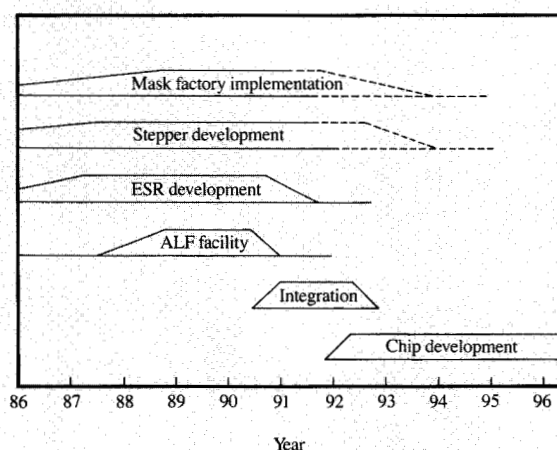


Figure 14

Modified bar chart tracing the explicit accomplishments of the project and their integration to bring the project to a stage suitable for manufacturing.

GTD. A device program was designed around this beamline by IBM Burlington and East Fishkill and executed successfully. We now had two established beamlines on the BNL VUV ring capable of X-ray lithography.

Integration of the key elements first accomplished by Research had now been achieved by an independent group from our technology division [41, 42]. The next step was to accomplish this at East Fishkill in ALF [37, 43]. A plan for the integration process was established and largely executed according to our joint GTD/Research plan. First exposures were made in ALF on December 18, 1991, printing 0.33- μ m lines. Research's task was completed.

Closing remarks

This twelve-year X-ray lithography research and development program established a number of milestones in X-ray lithography. Beamline and wafer stepper technology and demonstration hardware (tooling and test wafers/runs demonstrating that the technology was feasible) were developed. Silicon-membrane and gold-absorber-based mask technologies were demonstrated. This included precision e-beam pattern-writing tool development and requirements and their application in mask fabrication for device programs, and also included the development of focused ion-beam technology and hardware for mask repair. Resist classification and characterization for the X-ray lithography exposure process and its use in the device program were developed. Device

chip demonstration and fabrication were verified via the ten-level CMOS large test chip experiment, in which all levels were exposed with X-rays. The defect insensitivity of X-ray lithography was observed and demonstrated. The development of an X-ray source comprising a compact superconducting storage ring, or synchrotron, and the ALF facility, including building, clean rooms, steppers, etc., was completed. Finally, we furthered the understanding of technology limits and error analysis in X-ray lithography.

We also established that a complex program such as this could successfully be executed in a research environment and transferred to a development and technology area. Communication, mutual respect, and skilled workers, as well as involvement with our GTD "customer" at a critical stage, were key to this process.

In some ways it was also a great social experiment and experience. Many people made contributions and sacrifices. It was, in total, a team effort that achieved our ultimate and original goal, and, in fact, exceeded that goal by establishment of the technology outside the Research Division. I personally enjoyed being a part of this significant and dynamic event.

Acknowledgments

Many people contributed to the IBM X-ray lithography research and development program. Some contributions were made within short time spans, some over the entire twelve years of the program; some were outstanding contributions of strategic significance, and others were solid contributions of tactical importance. Unfortunately, there is not space in these pages to list individually all who contributed, and so a list of their organizations must suffice: Anorad Corporation, Brookhaven National Laboratory, IBM GTD Burlington and East Fishkill, IBM HQ, IBM Research, and Oxford Instruments.

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