

Electrical connections to the thermal conduction modules of the IBM Enterprise System/9000 water-cooled processors

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In a complex multichip carrier such as the thermal conduction module (TCM) of IBM high-performance mainframe processors, the interfaces between chips and their substrate as well as between the substrate and its printed circuit board must support a large number of electrical connections. Since chip, substrate, and board typically comprise very different materials, the electrical connections between them must be able to accommodate considerable thermally induced mechanical stress during assembly and use. This paper describes the pin attachment, chip attachment,

wire bonding, and laser deletion processes used for forming the electrical connections to the glass-ceramic/copper/polyimide/copper substrate of the thermal conduction modules of the IBM Enterprise System/9000™ water-cooled processors.

Introduction

In a TCM, electrical connections are established between chips and their substrate by means of soldered connections [1] designated as C4s (controlled collapse chip connections). Wires designated as EC (engineering change) wires are

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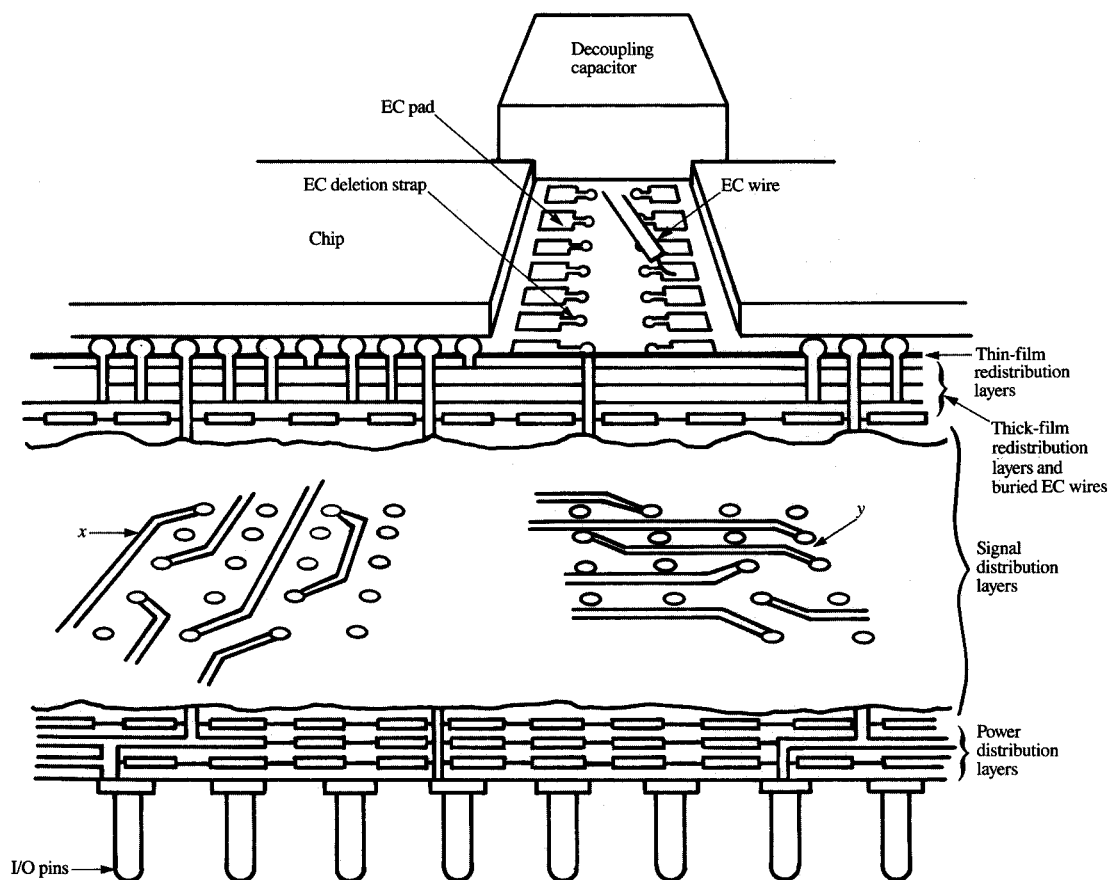


Figure 1

Schematic of the glass-ceramic/copper/polyimide/copper substrate used in the IBM ES/9000 water-cooled processors.

used where necessary to establish additional connections, and I/O pins are used for connecting to the next level of assembly. For the purpose of this paper, the term *interconnection* is used to designate electrical connections to the substrate. The types of interconnections used in the TCMs of the Enterprise System/9000™ (ES/9000™) water-cooled processors can be seen in the schematic of **Figure 1**. Those used for its chips, decoupling capacitors, and EC wires can be seen above, and those used for its I/O pins below.

Figure 2 indicates the sequence of steps used to achieve substrate interconnection. Following formation of the polyimide/copper multilayer structure on the surface of the glass-ceramic/copper substrate [3], pin attachment generally represents the final substrate-level process. Engineering change wires are added, and surface

conductor deletions are performed in order to provide any customization that may be required to achieve the current design level. Finally, chips and decoupling capacitors, each containing C4s, are attached, creating a functional module. During processor development, modules are optimized, requiring many replacements of chips and EC wires.

The packaging methods used for most large [4, 5] and some mid-range [6] computer systems recently developed outside IBM also make use of a multichip carrier approach. In the methods used by NEC [4] and Hitachi [5], chips are first mounted onto a single chip module, and multichip carriers are then used as boards. This results in a greatly reduced chip I/O density at the multichip carrier level. In the method used by DEC [6], chips are bonded directly to a multichip carrier by means of high-density

TAB (tape automated bonding). Although neither of the above methods results in the high chip I/O density achieved using C4s, a novel separation of signal and power connections is incorporated in the DEC systems through the use of flexible edge connectors. The larger systems produced by IBM, NEC, and Hitachi incorporate I/O pins, attached directly to the bottom surface of their respective multichip carriers, to achieve both signal and power connections.

The development of means to achieve substrate interconnections for the ES/9000 water-cooled processors posed several significant challenges. By comparison with their predecessors, the IBM 3090™ processors, in addition to the considerable increase in the numbers of all types of interconnections required per substrate, new materials were introduced, creating a number of new interfacial conditions to be satisfied. Table 1 provides an overview of the relevant design, materials, and process changes that were implemented. These process changes are described and the basis for them is presented in the balance of this paper. In several instances data have been normalized or presented in only general terms, because some aspects of this work are currently confidential.

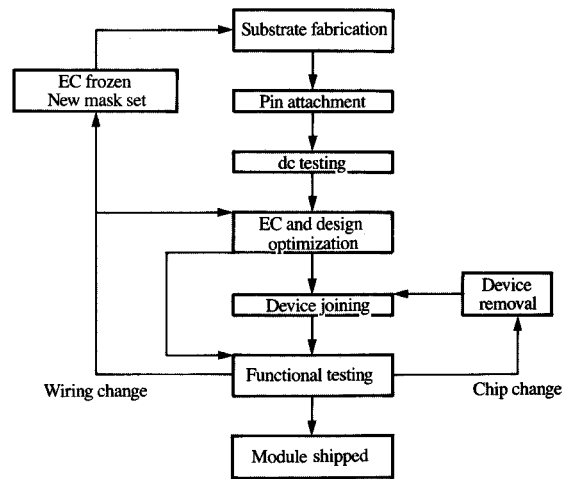


Figure 2

Sequence of steps for achieving substrate interconnection. From [2], reproduced with permission.

Table 1 Interconnection-related aspects.

Aspects	Processors	
	3090*	ES/9000 water-cooled models
Substrate material	Alumina/Mo	Glass-ceramic/Cu/polyimide Cu
Thermal coefficient of expansion ($\times 10^{-6}/^{\circ}\text{C}$)	6.5	3.0
Surface metallization		
Bottom-surface metallization (BSM)	Mo-Ni-Au	Cr-Cu-Ti-Au
Top-surface metallization (TSM)	Mo-Ni-Au	Cr-Cu-Ni-Au
Deposition process	Screen and plate	Photolithography and evaporation
Design factors		
Pins per module	1800	2772
Pin DNP† (mm)	51	74
C4s per chip	179	648
C4 size/spacing (μm)	125/250	100/225
C4 DNP† (mm)	2.8	4.1
Components	Chips	Chips and capacitors
EC pads per chip	96	228
EC pad size (μm)	300	220
Buried EC wire (BECW) for coupled noise	No	Yes
Active area (cm^2)	95	121
Materials/process		
Pin shape	Nail head	Tapered head
Pin solder deposition	Screened paste with flux	Preattached preform, no flux
EC wire diameter (μm)	56	38
EC deletion	Pulsed ruby laser	Pulsed excimer laser

*Note: All 3090 models are water-cooled.

†DNP: Distance from neutral point

I/O pin attachment

Input/output (I/O) pins are used to achieve electrical connections from TCMs to a printed circuit board. Pins are hard-soldered to the module, but must withstand multiple mechanical insertions into mating bifurcated springs on the printed circuit board [7]. Pin shank diameter, elastic modulus, minimum yield strength, and surface metallization requirements permit the pins to open the spring at a reasonable load and experience adequate wipe for reliable electrical contact, without suffering permanent offset in overall shape. In addition, the pins must withstand processing and handling stress. These pin requirements are generally the same as previous requirements [8].

As shown in Table 1, the TCM described here contains 50% more I/O pins, requiring a 40% increase in distance between the outermost pin and the geometric neutral point (DNP). Pin pitch and I/O pad diameters remain unchanged. Pattern distortion during sintering with the higher-DNP design precludes the use of plated, sintered-in I/O pads. I/O pad metallization consists of a vacuum-deposited thin-film pad which accommodates sinter distortion. The structural base is a glass-ceramic/copper substrate, which provides less strength and toughness than the previously used alumina/molybdenum substrates [3]. In addition, the excellent match in TCE (thermal coefficient of expansion) between the glass-ceramic/copper substrate and its silicon chips, while beneficial for C4 reliability, increases the thermal mismatch between the I/O solder fillet material and the substrate.

While optimization of the geometry of the pin-attachment regions of the alumina/molybdenum substrate focused on reducing stress in the solder to limit solder fracture [9, 10], optimization for the glass-ceramic/copper substrate was focused on reducing process stress in the substrate itself.

• Optimization of I/O pin joints

Reilly and Shih [11] have provided an excellent review of key parameters to be considered in managing pin-joint stresses.

Use is made of the hard solder Au-20 wt% Sn eutectic (melting point: 281°C) for the alumina/molybdenum substrates because of the high room-temperature strength and modulus of this material ($E = 75$ GPa, $\sigma_y = 13$ MPa)¹ [10, 11]. Because of present mechanical requirements, use of the Au-20 wt% Sn eutectic was continued.

An elastic finite element model of the pin/joint/pad system was developed using the previous TCM pin-joint geometry, but assuming the presence of a thin-film I/O pad on a glass-ceramic base. Results of this analysis suggested

a sharp peak in stress concentration near the edge of the I/O pad, of the order of the bulk strength of the ceramic.²

Bulk ceramic strength measurements were shown to follow a Weibull distribution, determined to be dependent on the amount of surface area stressed. This was interpreted as indicating that ceramic strength is governed by the distribution of surface flaws. Stressing of a smaller-area sample would therefore decrease the probability of including a flaw of critical size, effectively increasing the statistically expected strength of the sample² [12].

Using as the area stressed the narrow annulus projected from the finite element stress peak, and using the measured distribution of bulk strength of the glass-ceramic, Fu and Sura² have used the following form to predict the strength probability distribution for the substrate beneath an individual pin:

$$P = 1 - \exp \left[-A \left(\frac{\sigma}{\sigma_c} \right)^n \right], \quad (1)$$

where A is the area stressed, σ is the local fracture strength, and σ_c and n are the Weibull parameters. Assuming that fracture occurs when the applied stress exceeds the local fracture strength, a normalized plot of the predicted frequency of substrate fracture as a function of applied stress can be generated, as shown in Figure 3. To eliminate the possibility of ceramic fracture, various geometry and process aspects were optimized.

Following the guidelines outlined by Goldmann [9], pin head and I/O pad diameters were maximized within the constraints of pad spacing and manufacturing tolerances. A significant, expected [13] reduction in substrate stress was achieved by reducing solder volume, but this led to a considerable increase in solder fractures during pin tensile testing. However, by introducing a taper into the pin head geometry [14, 15], it was found that solder volume and consequently solder-induced substrate stress could be reduced significantly with no increase in solder fracture. Nail-headed vs. taper-headed pins are compared schematically in Figure 4.

The I/O pad metallization includes an adhesion layer such as Ti or Cr, a wettable reaction layer such as Ni, Ti, or Cu, and a top layer of Au to enhance wetting to the AuSn eutectic. As indicated in Table 1, Cr-Cu-Ti-Au was selected. A Cr layer several hundred Å in thickness was found to give adequate and highly reproducible adhesion between the I/O pad and the glass-ceramic. The Ti and Au layers are both of the order of 1 µm in thickness. Ti and Au couple to form a complex reaction barrier, with Ti-Au compound formation at Ti grain boundaries impeding further Au diffusion. The Cu layer, several µm in thickness, adheres well without reacting to both Ti and

¹ N. G. Ainslie, retired; formerly IBM Research Division, Almaden; private communication.

² Y. Fu and V. Sura, IBM General Technology Division, East Fishkill facility; private communication.

Au, and serves to accommodate some of the thin-film stress [15, 16].

Additional aspects of the I/O pad metallurgy optimization are currently confidential.

• Optimization of I/O pin attachment

Further refinements were made to the pin attachment process for manufacturability, durability during chip attachment cycles, and process control.

Because solder volume had been reduced, precise control of solder volume was required to ensure good fillet formation. This was achieved by attaching a prefabricated spherical solder preform to the head of the pin [17], thereby reducing variation in volume to less than $\pm 10\%$ as measured by weight. (The earlier screened solder paste process typically resulted in variations greater than $\pm 25\%$ of nominal.) A cross section of a pin with a preattached solder preform is shown in **Figure 5**.

To minimize voids in the solder structure, the pins were attached without flux in a 10% forming gas atmosphere (to minimize tin oxide formation). This also eliminated the need for post-soldering flux-residue cleaning operations.

Pin attachment is achieved in a furnace reflow process in which the full array of 2772 pins is fixtured in an assembly constructed of graphite having a TCE closely matched to that of the glass-ceramic/copper portion of the substrate. Pins with preattached preforms are weighted during reflow, ensuring good contact.

In contrast to soft solders, which are typically reflowed with 30–50°C of superheating [18], the Au–20 wt% Sn eutectic is typically reflowed at about 100°C above its melting point to ensure good fillet formation. Joining profiles were optimized to take maximum advantage of the stress relaxation known³ to occur in this eutectic at temperatures above 150°C.

Use of the above approaches—and others—led to the development of a relatively robust pin-joint structure. Process monitoring, involving pin tensile tests, has demonstrated that fractures occur in the shank of the pin at loads which exceed 50 newtons, far in excess of functional requirements.

Chip attachment and replacement

As previously, chip attachment and replacement are achieved by using the “flip-chip” C4 soldering method. Chip replacement requires preparation of the site from which a chip was removed for reattachment, and permits TCMs to be upgraded as more advanced chips become available. The TCM that is described here, in addition to permitting the interconnection of up to 121 semiconductor chips, can accommodate 121 C4-terminated capacitors.

³ See footnote 1.

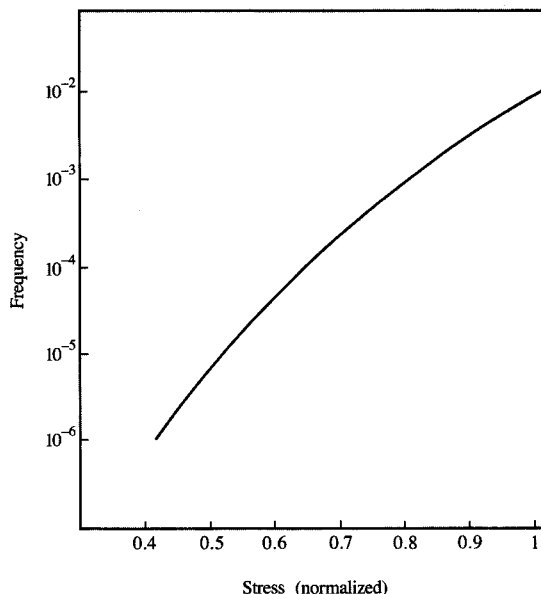


Figure 3

Predicted frequency of substrate fracture as a function of applied stress, applying Equation (1).

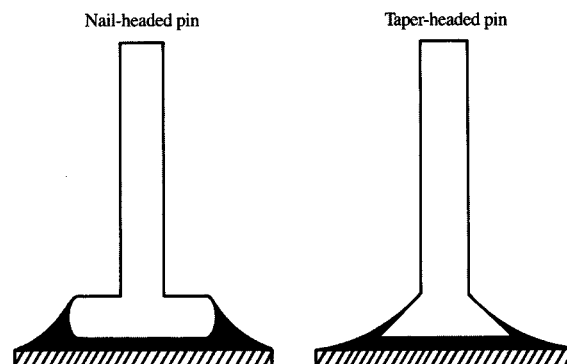
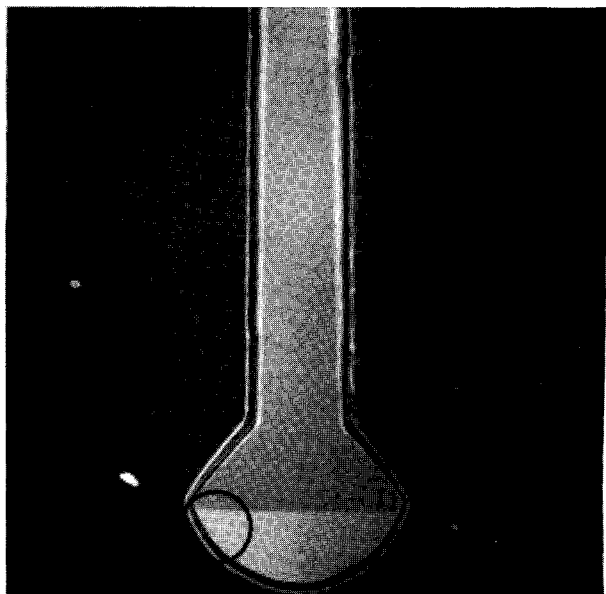


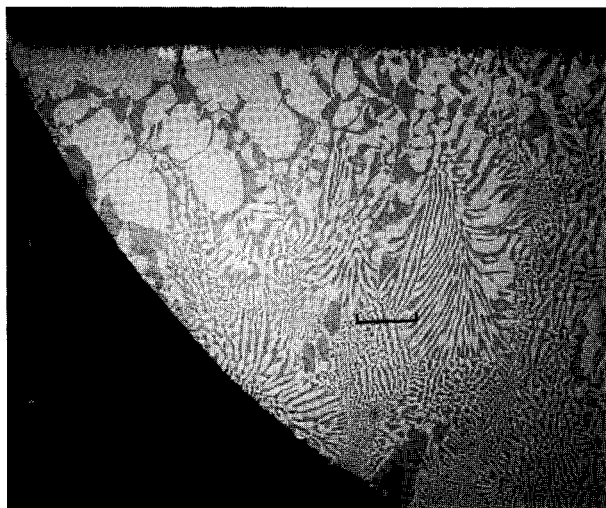
Figure 4

Schematics of nail-headed and taper-headed pins.

As indicated in Table 1, use is made of smaller C4s on the chips than previously, 3.6 times as many C4s per chip, and a tighter C4 grid. A “chip footprint” consists of 648 C4s placed in a partially depopulated 27 × 27 grid array.



(a)



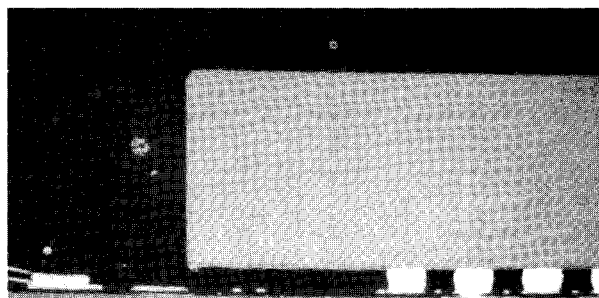
(b)

Figure 5

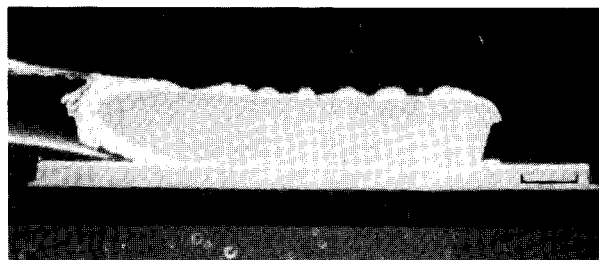
(a) Scanning electron micrograph of transverse section through taper-headed pin with a preattached preform; length of marker is 250 μm . (b) Magnified view of encircled region; length of marker is 25 μm .

Despite the increase of more than 45% in C4 DNP (Table 1), thermal cycle fatigue has been reduced because of the excellent match in TCE between the silicon chips and glass-ceramic substrate. As previously, use is made of a Pb-Sn solder and an underlying Cr-Cu-Au pad at the chip surface. This pad, designated as the ball-limiting metallurgy (BLM), also controls the diameter of the C4 solder ball that forms [19]. To increase the connection

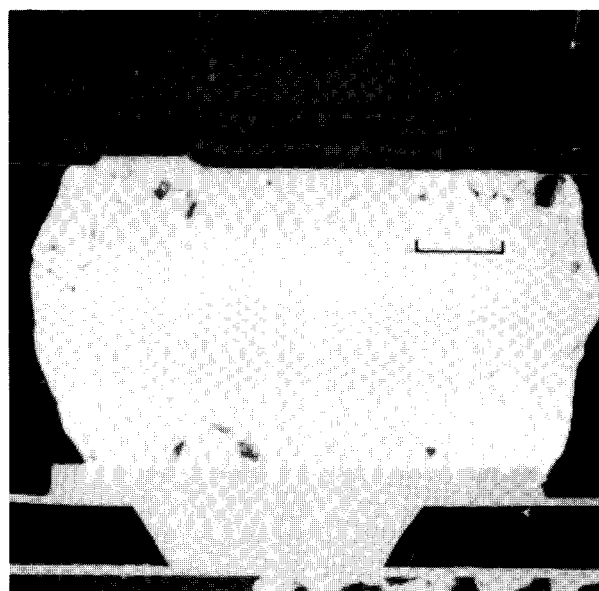
density on the chip, the diameter and pitch of the C4s were reduced from 125 to 100 μm and from 250 to 225 μm , respectively. The capacitors contain only 16 C4s, 125 μm in diameter on 450- μm centers, with a similar BLM. Pb-Sn with a high Pb content is used as the solder material for the C4s of both chips and capacitors.



(a)



(b)



(c)

Figure 6

(a) Scanning electron micrograph of cross section of a chip and EC wire bonded to a glass-ceramic/copper/polyimide substrate. (b) Magnified view of cross section of bonded EC wire; length of marker is 25 μm . (c) Magnified view of cross section of a bonded C4 solder ball; length of marker is 20 μm .

A key requirement of the substrate top-surface metallurgy (TSM) is its ability to withstand the thermally induced mechanical and metallurgical stresses of multiple attachment and replacement cycles. A vacuum-deposited composite consisting of a reaction layer such as Ni or Co, several μm thick, and a Au layer a few hundred Å thick, was found to satisfy this requirement [20]. Chips joined to such a composite have withstood a tensile force of more than 175 newtons prior to ductile fracture in the C4 solder. Cross-section analysis shows that substrates subjected to the maximum number of rework cycles permitted in manufacturing maintain an intact reaction layer. Part (a) of **Figure 6** is a scanning electron micrograph of a cross section of C4 solder balls thus joined to a thin-film TSM on a polyimide layer (on the surface of a glass-ceramic/copper substrate). Part (c) is a magnified view of a bonded C4 solder ball.

Chip attachment is accomplished by fluxing attachment sites on the substrate, aligning C4 solder balls on the chips with matching pads on the substrate, placing the chips on their sites, and passing the assembly through a furnace at a temperature high enough to obtain satisfactory solder joints [1, 21]. The substrate is then cleaned in a solvent to remove any residual flux. Critical parameters such as placement force, flux volume, and reflow temperature profile were optimized in order to maximize yield. By using optimized parameters, it is possible to form high-quality solder connections on 100% of the more than 70 000 solder connections on a single substrate in one pass through the joining furnace.

In chip replacement, as indicated by Puttlitz [21], potential substrate damage can be minimized by heating the C4s to above the solder liquidus and then removing the chip to be replaced. A careful thermal balance must be maintained in order to avoid melting the solder on adjacent chips and the pin-attachment solder on the underside of the TCM. Chips are removed by focusing an infrared light source onto their back side using careful process control [22]. Once the solder is molten, a vacuum probe is used to remove the chip from its substrate. **Figure 7** is a schematic showing the operational portion of the infrared light source that is used.

After a chip or capacitor has been removed, the substrate site is "dressed" (prepared to receive a new device). Residual solder removal is necessary to avoid solder volume buildup. Earlier approaches utilized a directed high-velocity hot gas to remove this solder residue [21], but process uniformity was found to be difficult to control because of the presence of a larger number of C4s on a chip site. Instead, a porous Cu block of roughly chip area is brought into intimate contact with the chip site, and heated by means of infrared radiation. The residual solder is then melted and wicked into the block [24]. In manufacturing use, this technique has been shown to leave

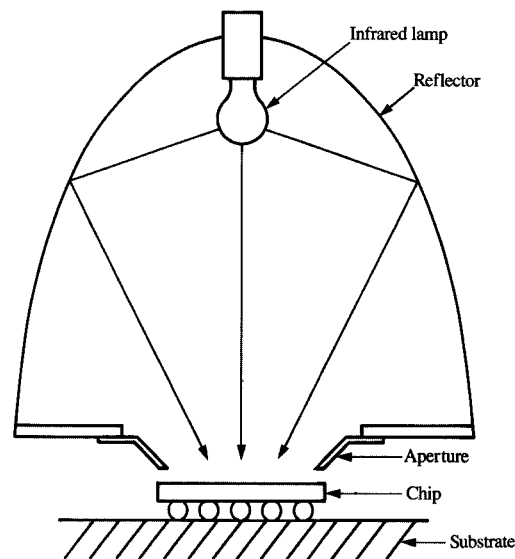


Figure 7

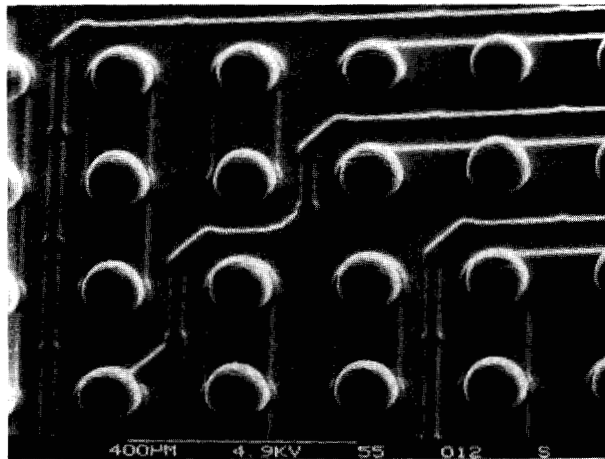
Schematic of infrared light source used for chip removal and site preparation. From [23], reproduced with permission.

residual solder less than $25\ \mu\text{m}$ in height on the substrate surface. In **Figure 8**, a site on a substrate that contained a group of C4s is shown following device removal and subsequent site dressing [23]. Chip sites subjected to multiple removal, dressing, and chip reattachment showed no degradation in metallurgical structure.

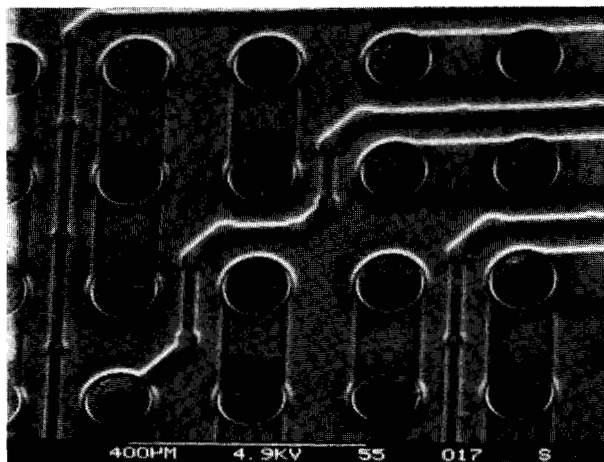
Engineering changes

The capability to introduce engineering changes by the addition and deletion of substrate conductors has continued to add flexibility to the IBM thermal conduction and multichip modules (TCM/MCM) [25, 26]. Associated wire attachment and laser deletion processes are performed directly on a substrate. As shown in Table 1, the introduction of the glass-ceramic/copper/polyimide substrate has led to a 2.4-fold increase in the number of EC pads per chip site. Furthermore, wire attachment and laser deletion processes suitable for the metallized surface of a polyimide dielectric are used. An overview of the sequence used to test and implement circuit changes in the TCMs is presented next, followed by a discussion of associated thin-film metallization, wire attachment, and laser deletion processes that are used.

Engineering change "pads" and deletion "straps" are shown in the schematic of Figure 1. C4s for use in signal



(a)



(b)

Figure 8

Scanning electron micrograph of C4 microsockets (a) immediately following device removal and (b) subsequent to site dressing. Markers are 100 μm in length. From [23], reproduced with permission.

paths are connected by means of a redistribution line to unique EC pads. These lines and pads are fabricated on a polyimide layer by thin-film processes [27]. Deletion straps connect each EC pad to a via, providing the path to an internal wiring net and to one or more C4s on the other chips of a TCM.

In the sequence in Figure 2, after substrate fabrication, an "opens/shorts" dc test is carried out and defective nets are repaired by the following use of EC wires: 1) the deletion strap between an identified EC pad and internal via is disconnected by a pulsed laser beam at all EC pads connected to the defective internal net; 2) appropriate EC pads are connected by using Au-plated Cd-Cu wires. The EC wires are insulated with a polyimide coating and are

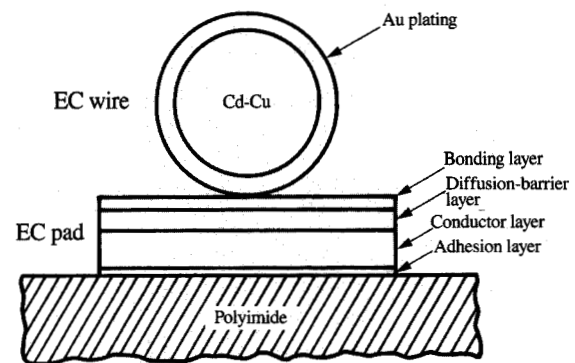


Figure 9

Schematic cross section of an EC wire and EC pad, prior to ultrasonic bonding. From [28], reproduced with permission.

bonded ultrasonically to the EC pads after the polyimide is removed from their ends by an arc. The forming, routing along wiring channels, polyimide arc-stripping, and wire bonding are performed by an automated tool.

After thus repairing internal opens and shorts, chips are joined to the substrate and the module is functionally tested. Changes to be made in internal nets are accomplished by replacing down-level chips and adding new EC wire connections as described above. This cycle of functional testing followed by creation of new internal nets is usually repeated during the course of system development. As designs become finalized, wiring changes previously implemented by EC wire attachment and strap deletion are incorporated into the substrate by generation of a new optimized set of masks for its conductive layers.

• EC wire bonding

A schematic cross section of an EC wire and EC pad on a polyimide substrate prior to ultrasonic bonding is shown in **Figure 9**. The EC pad contains several layers, including a Au bonding layer, a Ni or Co diffusion barrier layer [20], and a Cu conducting layer for fanout lines; the last also serves as a "cushion" for absorbing stresses produced during wire attachment and removal. For a given wire-pad combination, a bonding process "window" can be developed by comparing wire-pulling results (strength and fracture mode) against key process variables. Different aspects of optimization of the metallurgy and process variables have been described elsewhere [28, 29]. A scanning electron micrograph of an EC wire bonded to a glass-ceramic/copper/polyimide substrate is shown in part (b) of Figure 6.

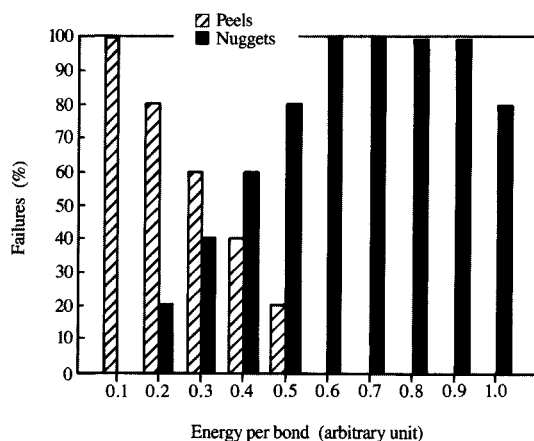


Figure 10

Illustrative process "window" for EC wire bonding, using 38- μ m-diameter wires. From [28], reproduced with permission.

Figure 10 shows an illustrative distribution of fracture modes plotted against relative bond energy. At low energies, wire removal by tensile pulling results in peeling. With increasing bond energy, the mode shifts to a mixture of peeling and nugget formation. (A nugget is a segment of the bonded wire left on the pad when the wire breaks at its base.) At sufficiently high energy settings, destructive fractures such as "tear-outs" of the EC pad metallization from its underlying polyimide occur. For a reliable and manufacturable wire attachment process, the process window should span a wide range of energy settings in which wire pulling results mostly in the formation of nuggets. It has been shown that if the Cr-Cu-Ni-Au metallization is used, the thicker the Au layer, the wider the bonding window; a thickness of a few thousand Å results in a sufficiently wide bonding window with regard to the pin and multiple-chip attachment processes described in previous sections.

• Laser deletion of EC line segments

Laser deletion is used to create an "open" in a line segment connected to an EC pad. In addition, the laser deletion process must not result in excessive damage to the underlying polyimide or other substrate components. Removal of an EC line segment with a focused, pulsed laser beam with minimal thermally related damage to nearby polyimide regions can be achieved by selecting a pulse width in the range of tens of nanoseconds. Lasers examined for this purpose included pulsed Nd-Yag and excimer lasers having pulse widths of 10–30 ns. Damage to nearby polyimide because of heat conduction during the

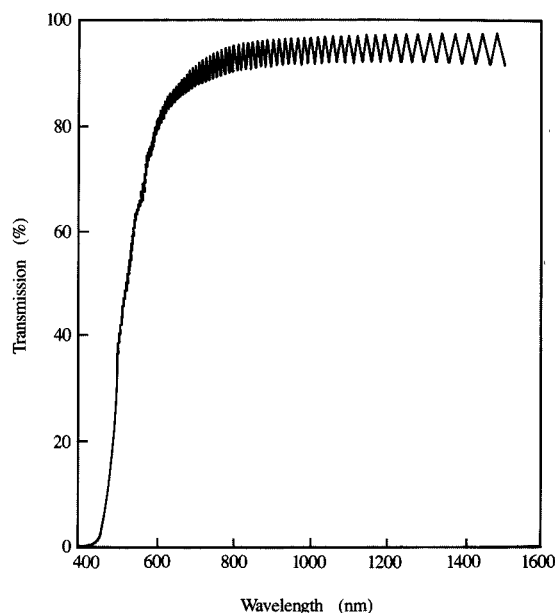


Figure 11

Transmission spectrum of a typical fully cured polyimide film. From [28], reproduced with permission.

application of microsecond-long laser pulses has been described elsewhere [28].

A more difficult source of polyimide damage that must be minimized is that resulting from the direct absorption of the laser energy in the polyimide. Most commercially available polyimides absorb radiation in the visible and are highly absorbent in uv (100–400 nm). A transmission spectrum of a typical fully cured polyimide film is shown in Figure 11. We have found that absorption damage of polyimide film can be avoided by using a Q-switched Nd-Yag laser operating at a wavelength of 1060 nm. A scanning electron micrograph of deletions of EC line segments produced in this manner on a test sample is shown in Figure 12. The energy per pulse, however, must be controlled within a narrow range to avoid catastrophic damage to the polyimide film in the deletion areas because of absorption in a metal feature below the polyimide film. Rapid heating and evaporation of the underlying metal film can cause a localized polyimide "blowout."

Deletion with an ultraviolet excimer laser always results in localized etching of the polyimide film beneath the EC line segments by a process known as ablative photodecomposition [30, 31]. The extent of polyimide etching can be controlled by the energy per pulse and the number

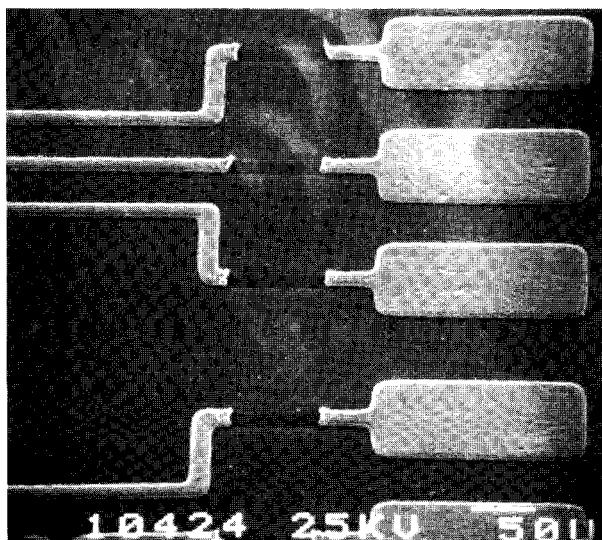


Figure 12

Scanning electron micrograph showing metal line deletions above an underlying polyimide film, achieved by means of a Q-switched Nd-Yag laser.

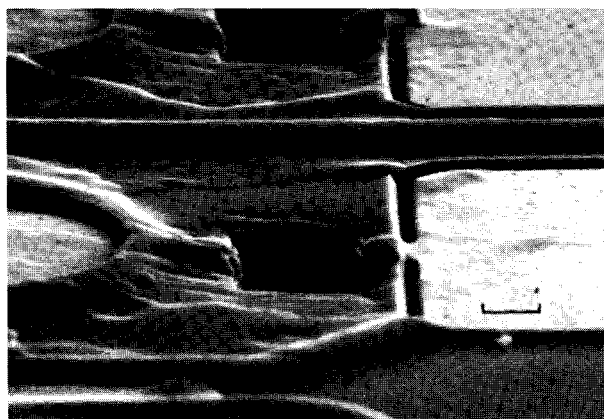


Figure 13

Scanning electron micrographs showing metal line deletions above an underlying polyimide film, achieved by means of an excimer laser; length of marker is 25 μm .

of pulses used. After experimentation with both types of lasers, it has been shown that it is easier to control the localized etching caused by an excimer laser than the occasional catastrophic blowouts of polyimide films experienced during Nd-Yag laser line deletions. Such use of an excimer laser has been successfully implemented in manufacturing; typical EC deletions produced by such a process are shown in **Figure 13**.

• “Buried” EC wiring (BECW)

For the relatively long EC wires used in previous TCMs, impedance and noise requirements could be met through the imposition of dimensional ground rules. With the increase in active surface area of the substrate and the increase in electrical performance requirements, relatively long EC wires can no longer satisfy current requirements regarding impedance EC wiring and near-end coupled noise [32]. Although the use of coaxial wires and twisted-pair wires can satisfy these requirements, their use is impractical because of the small physical dimensions available. A new wiring scheme designated as “buried” EC wiring (BECW) utilizes both the wire bonding and laser deletion processes discussed above in order to satisfy the impedance and noise requirements [2, 33].

Key elements of the BECW scheme can be seen in **Figure 14**. A dedicated x and y wiring layer pair is incorporated in the glass-ceramic/copper portion of the substrate, as shown. BECW pads with vias to these “buried” x or y wires are placed in a stitch pattern around each chip site, adjacent to EC pads. Interconnection is achieved by using short (a few mm) discrete surface wires or jumpers between EC and BECW pads to appropriately link selected x and y wires. An example of the use of discrete EC wires to connect EC and BECW pads on a substrate is shown in **Figure 15**.

Summary

Advances incorporated into the TCMs of the IBM Enterprise System/9000 water-cooled processors include those in pin attachment, chip attachment and replacement, and EC wire attachment and line deletion covered in this paper, specifically,

- The use of means to reduce the stresses associated with pin attachment. To accommodate glass-ceramic substrate strength limitations, such a reduction is achieved in part through a significant reduction in solder fillet volume; the latter is made possible by use of a tapered-head pin.
- The achievement of large-area-site solder “dressing” through the use of high-porosity copper blocks as solid wicks.
- The use of an EC-pad-to-EC-wire surface-bonding method coupled with the use of a “buried” EC wiring scheme.
- The use of a pulsed excimer laser to achieve EC line segment deletion.

Acknowledgments

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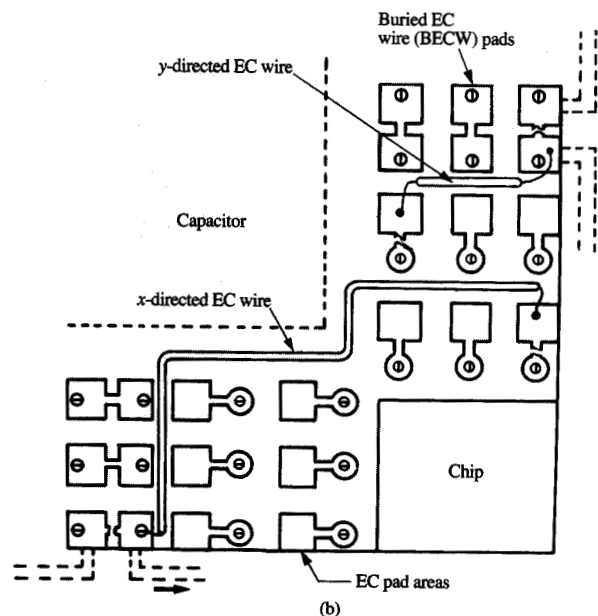
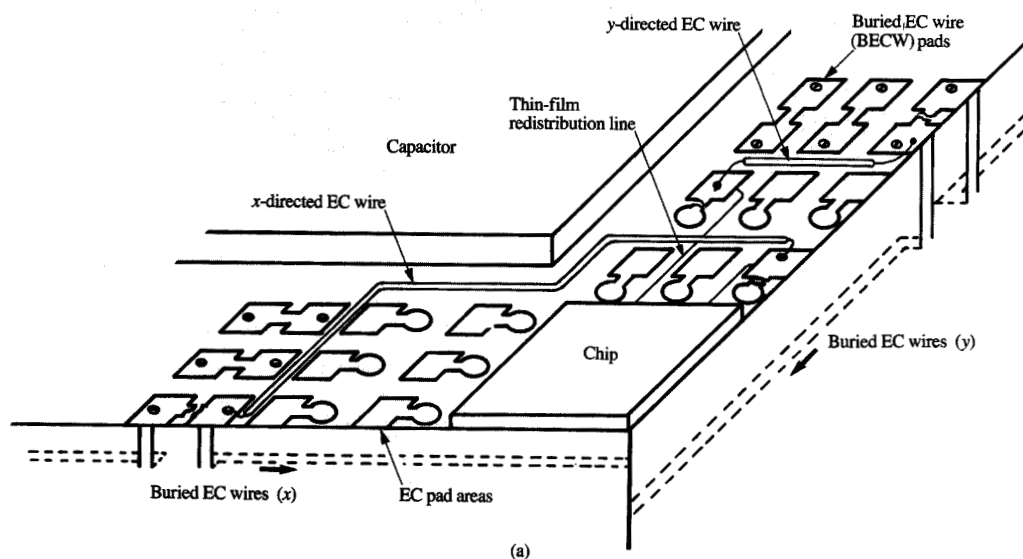


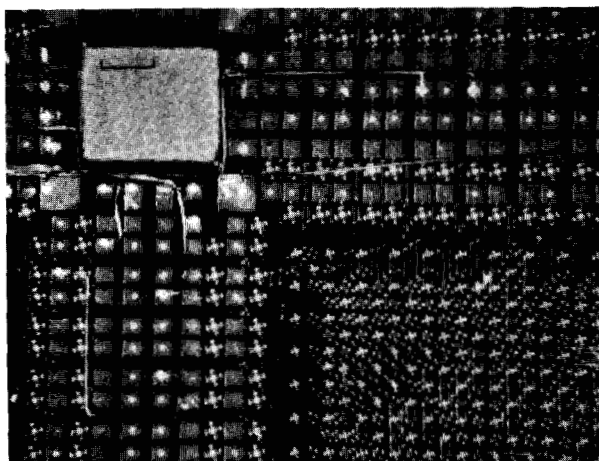
Figure 14

(a) Schematic illustrating buried EC wiring (BECW) scheme. Buried x and y EC wires are integrated in the glass-ceramic portion of substrate to create nets. (b) Top view.

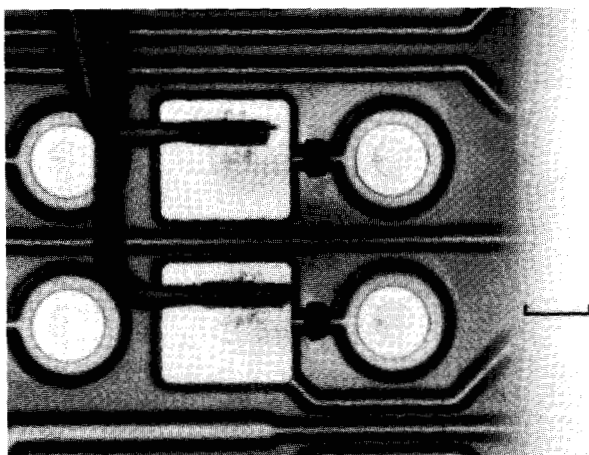
Waldman in connection with pin attachment metallization; K. Lidestri and K. Puttlitz in connection with device attachment and replacement; D. C. Hu, M. Interrante, and K. Seshan in connection with EC wire attachment and

deletion; and F. Ordonez in connection with physical analysis.

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(a)



(b)

Figure 15

(a) Photograph of a substrate, illustrating the use of EC wires in the vicinity of an attached capacitor. (b) Magnified view showing wires bonded to metallized surface pads; length of marker is 100 μm .

References

1. L. F. Miller, "Controlled Collapse Reflow Chip Joining," *IBM J. Res. Develop.* **13**, No. 3, 239 (1969).
2. D. Chance, A. Platt, C. W. Ho, and S. K. Ray, "Chip Carrier with Embedded Engineering Change Lines with Severable Periodically Spaced Bridging Connectors on the Chip Supporting Service," U.S. Patent 4,489,364, 1984.
3. R. R. Tummala, H. R. Potts, and Shakil Ahmed, "Packaging for IBM's Latest Mainframe Computers (S/390/ES9000)," *Proceedings of the 41st Electronic Components and Technology Conference*, IEEE, 1991, p. 682.
4. Y. Shimada, A. Dohya, K. Kata, and J. Inasaka, "High Speed Computer Packaging with Multilayer Glass-Ceramic Substrate," *Proceedings of the 1991 International Symposium on Microelectronics, ISHM*, 1991, p. 176.
5. T. Fujita, S. Ishihara, S. Ogihara, G. Toda, and Y. Watanabe, "Multilayer Mullite-Glass Ceramic Substrate for Mainframe Computers," *Proceedings of the 1991 International Symposium on Microelectronics, ISHM*, 1991, p. 187.
6. P. B. Dunbeck, R. J. Dischler, J. B. McElroy, and F. J. Swiatowiec, "HDSC and Multichip Unit Design and Manufacture," *Digit. Technol. J.* **2**, No. 4, 80 (1990).
7. R. Babuka, G. J. Saxenmeyer, Jr., and L. K. Schultz, "Development of Interconnection Technology for Large-Scale Integrated Circuits," *IBM J. Res. Develop.* **26**, No. 3, 318 (1982).
8. A. J. Blodgett and D. R. Barbour, "Thermal Conduction Module: A High-Performance Multilayer Ceramic Package," *IBM J. Res. Develop.* **26**, No. 1, 30 (1982).
9. L. S. Goldmann, "Mechanical Optimization of Brazed Pins," *Proc. Internat. Soc. Hybrid Microelectron. Conf.* **4**, No. 2, 420 (1981).
10. J. H. Kelly, C. K. Lim, and W. T. Chen, "Optimization of Interconnections Between Packaging Levels," *IBM J. Res. Develop.* **28**, No. 6, 719 (1984).
11. T. C. Reilly and D. Y. Shih, "Package-to-Board Interconnections," *Microelectronics Packaging Handbook*, R. R. Tummala and E. J. Rymaszewski, Eds., Van Nostrand Reinhold, New York, 1989, pp. 782-802.
12. A. G. Evans and R. L. Jones, "Evaluation of a Fundamental Approach for the Statistical Analysis of Fracture," *J. Amer. Ceram. Soc.* **61**, No. 3, 156 (1978).
13. K. Sahara, Y. Emoto, and K. Otsuka, "Improvement of Metallization of Alumina Substrates," *Proceedings of the 32nd Electronic Components Conference*, IEEE, 1985, p. 32.
14. B. N. Agarwala, P. H. Palmateer, and D.-Y. Shih, "Use of Tapered Head Pin Design to Improve the Stress Distribution in the Braze Joint," U.S. Patent 4,970,570, 1990.
15. D. Y. Shih, P. Palmateer, Y. Fu, J. Kim, S. Kapur, A. Arnold, B. Ghosal, P. Brofman, D. Waldman, P. Hayunga, S. Crikevich, J. Corso, and G. Advocate, "Designs of Low Stress I/O Pin Attach Systems," *Proceedings of the 1991 International Symposium on Microelectronics, ISHM*, 1991, p. 74.
16. A. F. Arnold, J. A. Croso, S. Kapur, W. F. Lange, and D.-Y. Shih, "Multilayer Thin Film Metallurgy for Pin Brazing," U.S. Patent 4,835,593, 1989.
17. W. R. Miller, P. H. Palmateer, and M. Potter, "Disk Reform for Braze Joining Pins to Substrates," *IBM Tech. Disclosure Bull.* **25**, 6430 (1982).
18. H. H. Manko, *Solders and Soldering*, 2nd ed., McGraw-Hill Book Co., Inc., New York, 1979.
19. P. A. Totta, "Flip-Chip Solder Terminals," *Proceedings of the 21st Electrical Components Conference*, IEEE, May 1971, p. 275.
20. B. N. Agarwala, K. F. Beckham, A. H. Cooper-Joselow, C. Narayan, S. Purushothaman, and S. K. Ray, "Multilayered Metallurgical Structure for an Electronic Component," U.S. Patent 4,985,310, 1991.
21. K. J. Puttlitz, "Flip Chip Replacement Within the Constraints Imposed by Multilayer Ceramic (MLC) Modules," *J. Electrical Mater.* **13**, No. 1, 29 (1984).
22. R. M. Meyen, K. J. Puttlitz, K. Schink, and H. Wenskus, "Individual Chip Joining Machine," U.S. Patent 4,160,893, 1979.
23. S. K. Ray, K. Beckham, and R. Master, "Flip Chip Interconnection Technology for Advanced Thermal Conduction Modules," *Proceedings of the 41st Electronic Components and Technology Conference*, IEEE, 1991, pp. 772-778.
24. B. Le Pape, "Use of a Tinned Copper Slug for Module Reworking," *IBM Tech. Disclosure Bull.* **24**, 3481 (1981).
25. B. T. Clark, "Design of the IBM Thermal Conduction Module," *Proceedings of the 31st Electronic Components Conference*, IEEE, 1981, pp. 356-363.
26. B. T. Clark and Y. M. Hill, "IBM Multichip Multilayer Ceramic Modules for LSI Chips," *IEEE Trans.*

Components, Hybrids, & Manuf. Technol. CHMT-3, 89-93 (1980).

27. T. F. Redmond, C. Prasad, and G. Walker, "Polyimide Copper Thin Film Redistribution on Glass Ceramic/Copper Multilevel Substrates," *Proceedings of the 41st Electronic Components and Technology Conference*, IEEE, 1991, p. 689.
28. S. K. Ray, K. Seshan, and M. Interrante, "Engineering Change Technology for Thin Film Metallurgy on Polyimide Films," *Proceedings of the 40th Electronic Components and Technology Conference*, IEEE, 1990, p. 395.
29. K. Seshan and S. K. Ray, "Effects of Surface Roughness on Wire Bondability," *Proceedings of the International Electronics Manufacturing Symposium*, IEEE, 1986, pp. 109-113.
30. R. Srinivasan, "Ablation of Polymers and Biological Tissue by UV Lasers," *Science* **234**, 559 (1986).
31. B. Braren and R. Srinivasan, "Optical and Photochemical Factors Which Influence Etching of Polymers by Ablative Photodecomposition," *J. Vac. Sci. Technol. B* **3**, 913 (1985).
32. E. E. Davidson, P. W. Hardin, G. A. Katopis, M. G. Nealon, and L. L. Wu, "Physical and Electrical Design Features of the IBM Enterprise System/9000 Circuit Module," *IBM J. Res. Develop.* **36**, No. 5, 877 (1992, this issue).
33. D. Chance, S. K. Ray, and C. W. Ho, "Engineering Change on Multichip Modules," *Research Report RC-9036*, IBM Thomas J. Watson Research Center, Yorktown Heights, NY, 1981.

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