Directory and Trace memory chip with active discharge cell

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The Directory and Trace memory chip is a 7.1Kb static random-access memory with 28-bit field simultaneous compare function and independent read and write 28-bit field addressing. The array is organized as four 64 by 28 subarrays. It incorporates a unique Schottky barrier diode (SBD)-coupled cell with active discharge. As memory cells are reduced in size with each new generation, soft errors become a major concern. One method of providing high soft-error immunity is to operate the memory cell transistors in the saturation region. However, in order to write data into such memory cells, the saturation capacitance in the memory cell transistors must be discharged. In prior art, such a capacitive transistor-saturation discharge was accompanied by increased power consumption and/or delay. Typically, the new data signals themselves are used to overcome this saturation capacitance. In this design a unique SBD-coupled active discharge cell discharges the conducting transistor saturation capacitance before writing new data into the cell. Thus, it enhances the write performance and preserves the high soft-error immunity of the cell.

Introduction

The Directory and Trace memory chip was developed for use in the water-cooled Enterprise System/9000™ (ES/9000™) processor family. It was designed with enough features so that it could be used in various applications within the system design. The primary applications are as an address translation array and a data cache directory chip. Other applications include an instruction cache directory and an I/O processor cache directory. It is also used throughout the machine as a trace and instrumentation array because of its relatively wide write bandwidth.

Some of the key enhancements, from a system design perspective, that the chip provides over prior designs are the following: The array is double in density compared to its predecessor. This was necessary in order to meet the system package requirements. The compare logic function and performance were also significantly improved to allow the chip to be used more efficiently throughout the system.

The Directory and Trace memory chip is designed to operate at an 8-ns cycle time. Thus, the entire write operation must take place within 8 ns. The cell bipolar transistors are operating in saturation to provide high soft-error immunity. The saturation capacitance of these devices must be discharged before the cell can be written. In prior art, the new data signals were used to overcome this capacitance, at a cost of increased power consumption

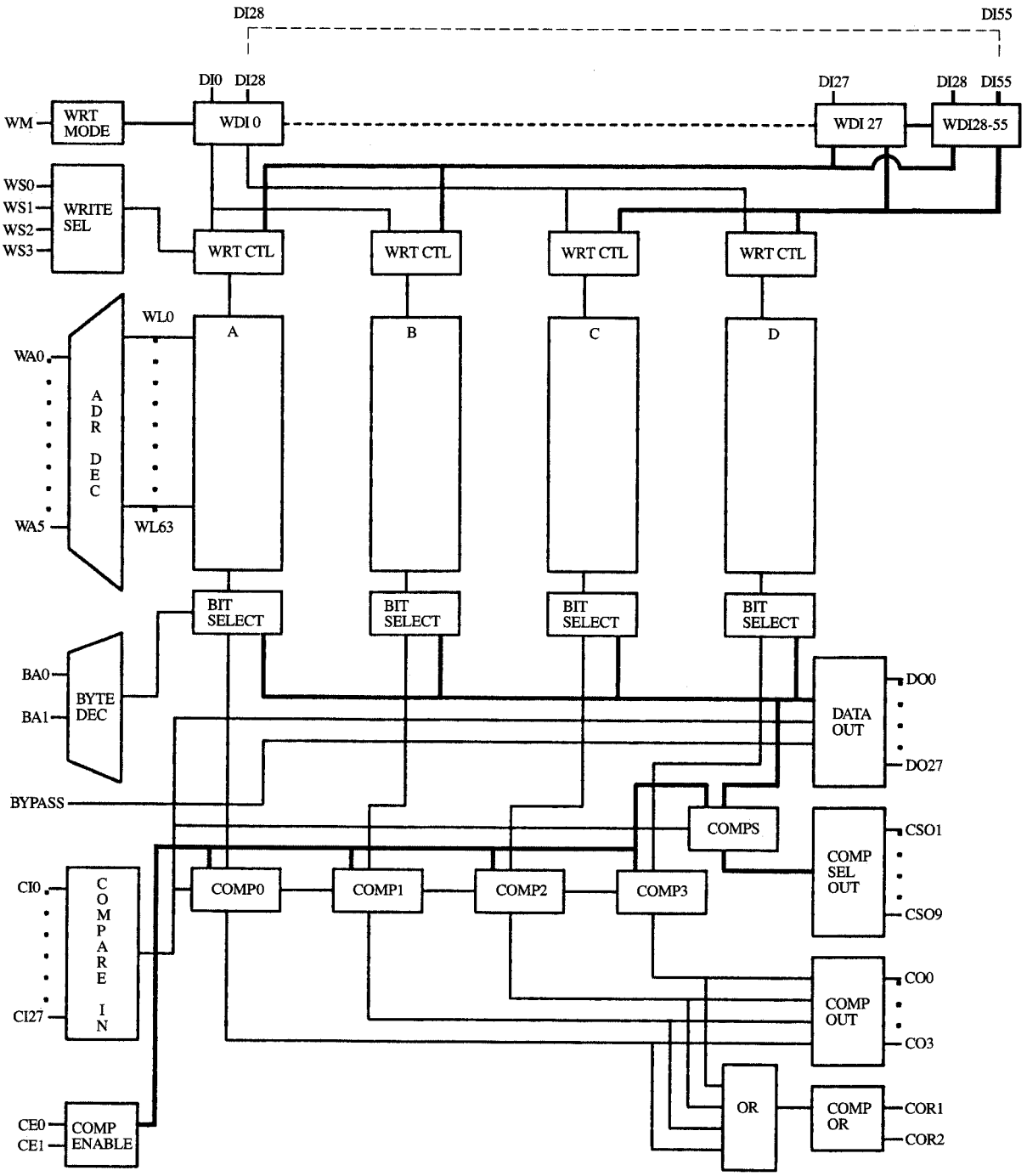

Figure 1

Directory and Trace memory organization.

and/or delay. To improve upon this, an SBD-coupled active discharge cell [1] was designed. The active discharge path reduces the delay as well as the writing time of the cell [2, 3].

Chip description

The chip is partitioned into four subarrays, as shown in **Figure 1**. Each subarray is 64 deep by 28 wide. The chip is a one-port array, with the same word address bus used for writing and reading. The same subarray cannot be written and read on the same cycle. Pertinent characteristics are given in **Table 1**.

Four write control lines, WS0, WS1, WS2, and WS3, determine which subarray(s) is to be written. Up to two of the four subarrays can be written at once. The write data bus into the chip is either 28 or 56 bits wide (a mode bit, WM, determines the width). For writing, the chip appears as one array whose dimensions are either 256 deep by 28 wide or 128 deep by 56 wide.

There is one 28-bit-wide read data bus that leaves the chip. A 2-bit read address bus, BA0 and BA1, determines which of the four subarrays is read. For reading, the chip appears as one array whose dimensions are 256 deep by 28 wide.

One 28-bit-wide compare input bus enters the chip. This bus is compared against the outputs of the four subarrays in four parallel 28-bit compare operations. The width of the compare can be altered by multiples of 7, using two mode inputs, CE0 and CE1. An (I/O) bypass line can be used to put the compare input bus onto the read data bus.

The four compares are driven off-chip in three different ways:

1. The four compares are each driven off-chip individually. These are called the "individual compares."
2. The four compares are OR-ed together into one line, with two copies of this line driven off-chip. These are called the "compare-ORs."
3. One of the four compares is selected by the same two read address inputs that pick the read data bus. Nine copies of this line are driven off-chip. These are called the "compare-AOs" (and-ORs).

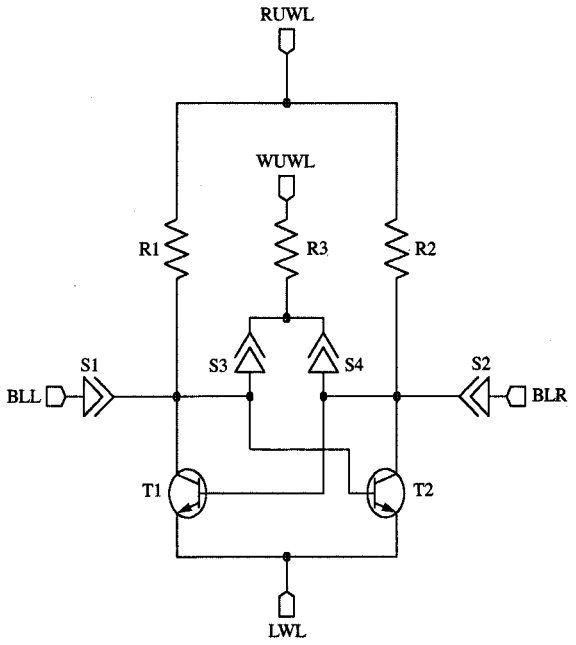

Figure 2
Directory and Trace memory cell.

Table 1 Chip parameters.

Cell size (μm)	34.8 × 36.5
Number of cells per chip	7168
Chip size (mm)	6.434 × 6.434
Power dissipation per chip (W)	10

Cell operation

- *Standby mode*

When a static memory cell is in standby mode, it must have sufficient stability to maintain data integrity. For the Directory and Trace memory cell (**Figure 2**), cell stability is achieved by ensuring that the cell outboard Schottky barrier diodes (S1 and S2) are reverse-biased over the entire standby design range, thus isolating the cell from the bit lines (BLL and BLR).

The cell standby current must be chosen to meet the system SER, or soft-error rate (a soft error is a random, nonrecurring error in a single bit of random-access memory with no permanent cell damage). To enhance soft-error immunity, the cell requires a minimum standby current of 36.9 μA at a temperature of 55°C. **Figure 3** shows the critical charge of the memory cell as a function of the standby current at 55°C. The equation for this curve is given in the Appendix. However, to further enhance the soft-error immunity of the cell, a higher bias current is chosen. This guarantees that the design meets the SER requirements.

The Directory and Trace memory chip is required to operate over a temperature range of 35–75°C, taking into account power supply fluctuations and manufacturing process tolerances. The critical charge equation and Table 2 in the Appendix allow a given Q_{crit} be calculated at a specific operating temperature and cell standby current. The actual nominal standby current for the array cells is chosen to be 54 μA. This value ensures that the chip meets the SER requirement for the system as mentioned above.

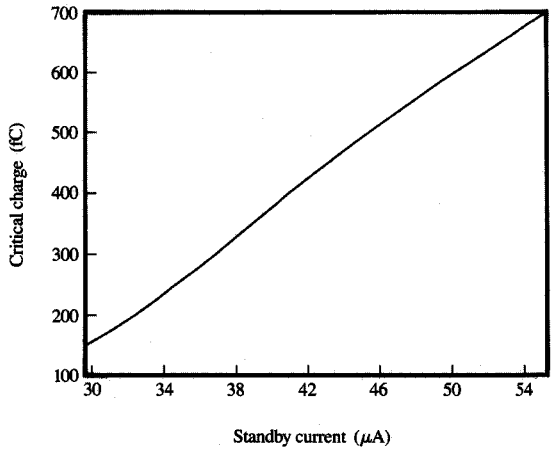

Figure 3

Memory cell critical charge variation with standby current.

In standby mode, both read upper word line (RUWL) and write upper word line (WUWL) are biased at 1.4 V, and the lower word line (LWL) is biased at 0 V. The transistor T1 is on, conducting 54 μA of current, and the transistor T2 is off (nonconducting). The resistors R1 and R2 provide 40 and 14 μA respectively for the standby current of the cell. Schottky barrier diodes (SBDs) S1–S4 are all reverse-biased. This ensures that the standby cell is isolated from the bit lines as well as from the WUWL.

- *Read mode*

The Directory and Trace memory chip array is organized as four bytes of 64 words by 28 bits. The addressed word spans all four bytes. In other words, 112 cells are selected during any read cycle.

The first design challenge faced was to minimize the voltage drops along each word line; driving 112 cells with a single word line would result in significant voltage drops from one end to the other, and large differences in voltage drop across the memory cells could result in variations to read and write performance. This performance variation is the result of cells stealing current or being starved of current on the basis of the potential drop across each cell. Thus, each word (112 bits of data) in the array was designed with one common word decode line which drives one word line group (LWL, RUWL, and WUWL) from each of the four subarrays. Since the word decode line carries only transistor base current, the voltage drop along this line is minimal. Each word line group now drives just 28 cells. To further minimize voltage drops in each word line group, the word line drive connections are made in the center of each group so that the span of each word line is only 14 cells.

To read a cell, current is drawn from the LWL of each of the word line groups corresponding to the word determined by the word addresses. This current causes the potentials of the LWL and RUWL to fall to −0.69 V and 1.06 V, respectively. WUWL remains biased at 1.4 V as in standby mode. When the collector node of the cell transistor that is conducting, T1, falls low enough to forward-bias the corresponding outboard SBD, S1, it conducts 240 μA, and an 18-mV differential voltage is developed on the bit lines. This signal is sensed by the bit sense amplifier and fed through a read amplifier to the data output driver. Only one byte of data, as selected by the byte addresses, is fed from the read amplifiers to the data output drivers.

The select current chosen must be large enough to develop a bit line differential voltage to overcome any leakage currents from the cells to the bit lines. For this chip, 335 μA per cell is the select current at 55°C. This current provides immunity to the bit line leakage mentioned above and also satisfies the system performance specifications over the power supply, process, and temperature design range.

- *Write mode*

A write cycle begins in the same manner as the read cycle. The cells are selected by drawing current from the appropriate lower word lines. In addition, discharge current is drawn from the write upper word line. Current then flows in one of the two SBD active discharge devices, S3 or S4, discharging the saturation capacitance of the cell. As before, each word line group services 28 cells (14 on each side, with the drive in the center). To prevent current stealing by one or more cells due to SBD forward-voltage tracking variations, a 750-Ω discharge resistor is added to each cell (R3 in Figure 2). The write data bit is presented to the cell by raising the potential of one of the bit lines connected to the cell. This turns on the cell transistor whose base is connected to this bit line through the SBDs S1 and S2.

In order for the new data bit to be written to the cell, the discharge current must be removed before the data is taken away. Otherwise, the new data would be discharged in the same manner as the previous data. To control this timing between discharge and data presentation, an on-chip write clock is provided. The pulse width of this write clock is designed to track with the write operation over the entire design range.

Figure 4 shows a computer simulation of the write operation for the Schottky discharge cell. The clock is activated at time 0. At 1.5 ns, current is drawn from WUWL, which begins the active discharge of the cells. At

1.8 ns, the write data are presented to the cells by means of the differential voltage between BLR and BLL. Initially, LWL follows BLR, since the cell transistors have not yet been fully discharged. When LWL begins to fall, the discharge of the cells has been completed. The writing of the cells is accomplished within a nanosecond. At 4.5 ns, the discharge current is removed from the cells, and they begin charging back to the normal selected state. The voltage differential between BLR and BLL determines which cell transistor is on, and thus, what data is stored in the cell. Finally, the data is removed from the bit lines and writing is complete. If the active discharge were not to occur, the write time of the cell would be of the order of microseconds.

In directory mode, the data byte is 28 bits wide. In trace mode, the data byte is 56 bits wide. During a write cycle, the number of cells that can be written is limited to 56 to prevent large power surges which can cause delay penalties or may disturb the data stored in the array.

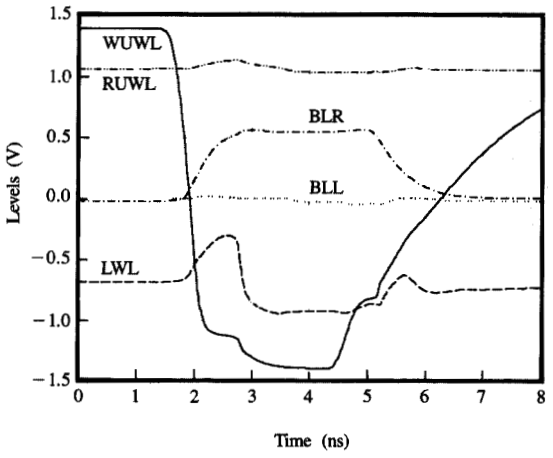

Figure 4

Simulation of write operation. For identification of the voltage nodes, see Figure 2.

Chip applications

There are five functions for which the chip is used in the system:

1. Trace and instrumentation.
2. Directory lookaside table (DLAT).
3. Segment table origin (STO) stack.
4. Logical directory.
5. Absolute directory.

These are described below.

Trace and instrumentation arrays are used for test floor debugging and performance measurement. For these applications, the write bandwidth is the most critical parameter of the array chip. The extra data-in bus allows the chip to be organized as a 56 wide by 128 deep array in write mode. This enables 128 cycles of trace information on 56 separate inputs to be stored on a single chip. For reading, several arrays are chained together, with the read data out from one array feeding the compare in of the next array. The bypass inputs of the arrays are then manipulated to select which array is read. Since the chaining has several chip crossings, the reads are multicycle paths. The chaining saves chip I/Os on the logic chip. This is accomplished by feeding the data-out bus directly to the compare inputs of the next chip in the chain. This array is also used in the central processor (CP) to store information required for address translation.

The directory lookaside table (DLAT), sometimes referred to as the translation lookaside buffer (TLB), is used for two purposes:

- It minimizes address mappings, where a logical address is mapped to an absolute address. A virtual address is mapped to a real address by translation. A real address is mapped to an absolute address. The segment table origin ID (STOID) is part of the virtual address.
- The DLAT is also used for saving the store protect key for a given address. The logical address portion of the DLAT (four chips) is similar to the logical directory, so they are discussed together below. The absolute address portion of the DLAT (two chips) is similar to the absolute directory, so they are also discussed together.

The segment table origin (STO) stack maps full STOs (20 bits) to STOIDs (seven bits). The idea is to abbreviate the STOs so that they take up less room in the DLAT and logical directory. The STO stack is similar to the absolute address portion of the DLAT and the absolute directory, so all three of these are discussed together.

The array also serves as a directory for the data caches. The enhancements that were made to the compare logic allow for an efficient implementation of this array across various applications [4, 5].

The logical directory and logical address portion of the DLAT use the chip as one 256 deep by 28 wide array. The compare-AOs are used to compare a given logical address and STOID with the array data. (These array data are selected by the six word addresses, WA0–WA5, and the two read address inputs, BA0 and BA1.) There are four logical directory chips, since the data cache is four-way set-associative. Therefore, there are 1024 logical directory entries. The logical directory is addressed with eight logical address bits. It uses the full 28-bit array field, 16

logical address bits, seven STOID bits, three parity bits, and a 2-bit mode field. When a directory access is made during normal system operation, the contents of the directory are compared with the corresponding bits of the requestor's address to determine whether there is a cache "hit" or "miss." There are four DLAT logical address chips. The DLAT is two-way set-associative, and is addressed with eight logical address bits which are different from the logical directory address bits. The DLAT chips contain 12 logical address bits, seven STOID bits, three parity bits, and the store protect key. There are 512 DLAT entries, where each entry is split across two chips. The read data buses for the DLAT logical address and logical directory are used only for parity checking and array testing. The logical directory employs nine copies of the compare-AO out. This improves the performance for this critical path, since one driver fans out to only one receiver. These chips, which receive cache data and the compare-AOs, are used to pick data from one of the four sets, or compartments A–D. The compare-ORs are used to check the compare-AOs, thereby improving the fault detection coverage of the design. If a compare-AO is on and the corresponding compare-OR is off, an error is detected. If a fetch request gets a hit in the DLAT and a hit in the logical directory, data is returned to the requesting execution element in the following cycle.

The absolute address portion of the DLAT and the absolute directory are used when the fetch gets a DLAT hit and a logical directory miss. One of two absolute addresses being read out of the DLAT is selected by the DLAT logical address hit lines described above. On the next cycle, this absolute address is used to search the absolute directory.

The absolute directory is organized differently from the logical directory. For reads, all four subarrays are accessed in parallel. The 22 bits of the 28-bit array field are used as the absolute address (just like the DLAT absolute address entry). Each of the four subarrays on a given absolute directory chip represents a set or compartment A–D. Each of the eight absolute directory chips can be addressed by three logical address bits. There are 1024 absolute directory entries (32 addresses × 4 sets × 8 classes). The eight compare-ORs (one from each chip) tell which class is selected. The individual compares (4 per chip × 8 chips = 32) tell which class and which set A–D is selected. The compare-ORs are important here, because the logic chip that needs to know only the class has few spare I/Os, and this way we use only eight I/Os instead of 32. The read data buses for the absolute directory are used for parity checking and array testing.

In normal operation, the compares for the DLAT absolute address chips are not used. However, they are used for special operation codes (OPS), such as IPTE (invalidate page table entry) and SSK (set storage key). These OPS compare a given absolute address bit with the absolute addresses in the DLAT. The individual compares are used. This way, the DLAT search takes only 64 cycles (vs. 256 cycles if the four parallel compares are not used), which significantly improves the performance of these OPS.

The STO stack chip also uses the four individual compare lines. A full STO is compared with four stack entries in parallel. If a hit occurs, the 5-bit array word address, merged with the 2-bit encode of the four individual hit lines, gives the corresponding STOID. This corresponds to 7-bit STOIDs for 128 STO stack entries. Each 28-bit-wide array entry contains the full STO. The STO stack uses 26 of the 28-bit-array-field bits. The STO itself is a 19-bit address with three parity bits. Also included are four miscellaneous control bits. The read data bus for the STO stack is used only for parity checking.

Conclusions

The Directory and Trace memory chip addresses the problem of providing high soft-error immunity while decreasing the write times in a memory cell array. The conducting transistors in the memory cell are operated in deep saturation to achieve a high soft-error immunity. By incorporating separate upper read and write lines, significant voltage drops along the upper word lines are reduced. The memory cell write time variations along the word lines due to differences in voltage drop across the memory cells are reduced. The SBD-coupled active discharge cell discharges the saturation capacitance of the conducting transistor in the forward current direction through the SBD active discharge devices prior to writing new data into each cell. This improves the write time and the write time tolerance, and further improves the power dissipation of the memory cell. The result is a memory cell array chip which satisfies all of the ES/9000 requirements for soft-error rate and cycle times.

The enhancements to both performance and functionality reflected by this design in comparison with the 3090™ series were a direct result of discussions held between the chip and system designers early in the design cycle. The end result was a design with enough flexibility to allow for its efficient usage in several system applications.

Acknowledgments

The authors are grateful to F. Y. Chang for providing the critical charge equation, which is derived from the simulation of critical charge as a function of standby current.

Appendix: Critical charge equation

From simulations of the circuit of Figure 2 we can fit to the data an expression for the critical charge in femtocoulombs [6],

$$Q_{CRIT} = Q_N(T)e^{(I_{STBY} - MQ_{CRIT})K},$$

Table 2 Q_{CRIT} versus I_{STBY} and a constant M with units of time^{-1}.

Q_{CRIT} (fC)	I_{STBY} (μA)	M (1000/ns)
150	29.7	0.0000235
200	32.5	0.0000235
250	34.7	0.0000235
300	36.9	0.0014060
350	39.0	0.0028950
400	41.0	0.0042660
500	45.5	0.0080460
600	50.2	0.0115600
700	55.3	0.0150430

where

$$Q_N(T > 55°C) = Q_N(1 + 0.020553\Delta T),$$

$$Q_N(T < 55°C) = \frac{Q_N}{1 + 0.020553\Delta T},$$

$Q_N = 7.214$ is the normalized Q_{CRIT} constant at 55°C,

$K = \dfrac{0.102191}{\mu A}$, a constant,

I_{STBY} is the cell standby current in μA,

M is a fitted parameter shown in **Table 2**,

ΔT is the magnitude of the change in temperature from 55°C in °C.

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