A four-level VLSI bipolar metallization design with chemical–mechanical planarization

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A high-performance four-level semiconductor device wiring fabrication process has been developed for bipolar devices in Enterprise System/9000™ (ES/9000™) processors. The reliable interconnection of large numbers of devices on a single integrated circuit chip has been enhanced by planarizing insulators and metals using chemical–mechanical polishing processes, by a novel contact stud structure, and by a Ti-clad Al–Cu metallurgy. This paper describes the structure of the four-level wiring and elements of the process, including the silicon contacts, techniques for depositing metal and oxide to cover features with high aspect ratios, high-temperature fine-line lift-off stencils, and high-density, area array solder terminals.

Introduction

Fast integrated circuits (IC) and densely packed IC chips can be produced by advances in lithography, thin-film processing, transistor structures, and circuit designs. Increases in circuit densities on a chip improve computer reliability and performance by reducing the number of IC chips in a computer and the effect of chip-to-chip signal delays. To realize these benefits, processes are required to electrically interconnect the maximum number of transistors on a chip. The major challenges are 1) to provide sufficient wiring channels to fully utilize increased chip densities, 2) to keep interconnection signal delays from becoming a more significant fraction of the total switching time, and 3) to increase interconnection complexity without adversely affecting manufacturing chip yield. An increase in the integrated circuit complexity usually increases the number of external contacts required for power and input/output signals.

The central processing units and components of the IBM Enterprise System/9000™ (ES/9000™) family that require high-speed circuits contain advanced emitter-coupled logic (ECL) chips, whereas the system cache memory contains bipolar static random access memory (SRAM) IC chips. The high-performance bipolar circuits include an 80 000-transistor "sea-of-gates" array and a 64-kilobit SRAM with

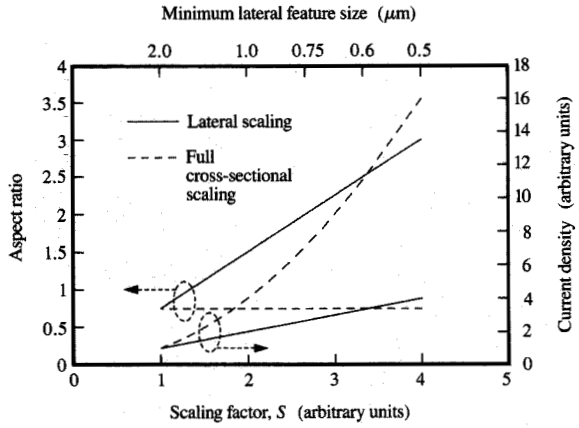


Figure 1

Aspect ratio and current density of minimum-dimension lines as feature dimensions vary with scaling factor S. Current density trends assume constant current. Trends are shown for lateral scaling and for full cross-sectional scaling.

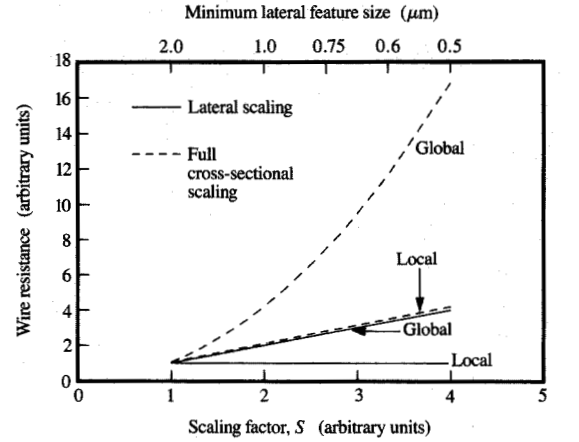


Figure 2

Resistance trends of minimum-dimension local and global wires as feature dimensions vary with the scaling factor S. The resistance of local and global wires is shown for lateral scaling and for full cross-sectional scaling.

a 2.5-ns access time [1]. Interconnecting devices is most complex for the sea-of-gates logic chips, which require wiring to connect approximately 85 000 transistors, 40 000 resistors, 10 000 junction capacitors, and 1000 Schottky diodes.

The design of interconnection structures for chips with a high density of reliable, high-performance circuits is affected by many competing demands, and trade-offs are inevitable. Scaling rules specify how integrated circuit component dimensions are reduced to the minimal dimensions achievable by lithography. A scaling factor, S, is equal to the factor by which the minimal lithographic dimension is decreased. "Ideal" scaling laws for field-effect transistor (FET) circuits [2, 3] usually require full cross-sectional scaling in which all dimensions in the transistor structure are reduced by a factor S. In FET circuits, full-dimensional scaling is generally applied, by which the width and height of interconnect lines and the thickness of insulator layers are decreased by the same scaling factor S [4, 5]. This simplifies changes in deposition, etching, and lithography processing because the aspect ratio (ratio of height to width) of the lines and spaces between lines remains constant.

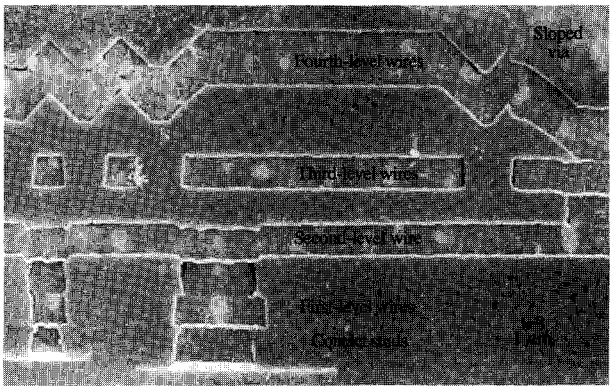
The optimal bipolar transistor is derived from different laws [6], since voltages and current levels typically scale much less than the lateral dimensions. One option is to laterally scale wiring dimensions by reducing linewidths and spaces by a factor S, while heights of the lines and insulator between layers of lines remain constant. To utilize the full speed of bipolar transistors, they must be operated near a minimum point in a delay-versus-power curve [6]. This places demands on the current-carrying capabilities of the interconnections, particularly when several emitters are connected to produce a "wired-OR" function. **Figure 1** shows the trade-off between current density and aspect ratio for full cross-sectional scaling and for lateral scaling assuming that the height of the laterally scaled lines remains constant at 1.5 μm. For an equal reduction in height and width, the cross-sectional area decreases quadratically as a function of S. If the current carried by the wires is not decreased, the current density increases quadratically, and circuit reliability is reduced because of electromigration in the wires. The cross-sectional area decreases only linearly with lateral scaling. For a constant current, current density is linearly increased, as shown by the lower solid line in Figure 1, and the risk of failure due to electromigration rises less rapidly than for full cross-sectional scaling. However, the aspect ratio increases as design scaling changes from full cross-sectional to lateral scaling, as shown in Figure 1.

Circuit performance is affected by the scaling rules selected [5]. **Figure 2** compares the trends in wiring resistance for full cross-sectional scaling and for lateral scaling with AlCu wiring. Two types of interconnections [4] are considered: local wires, which connect components within subcircuits, and global wires, which connect separate subcircuits and can extend as long as the chip length. The component complexity of subcircuits is unaffected by increases in chip complexity, so subcircuit dimensions decrease by the same factor S by which the

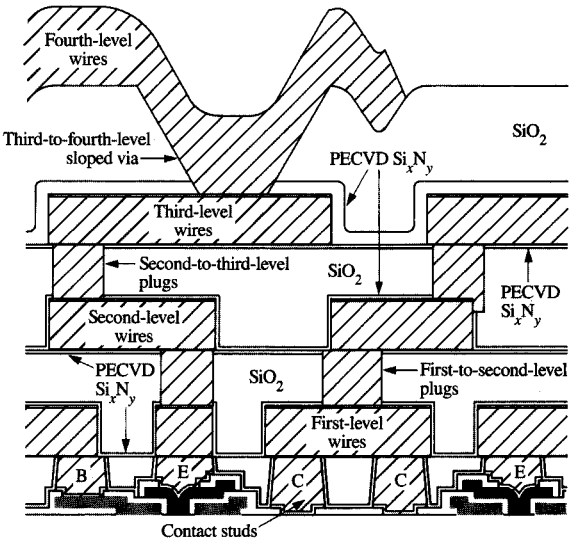
transistor dimensions decrease. Since local wires run within subcircuits, the local wire length decreases by the factor S. A decreasing local wire length compensates for a decreasing wire cross section. This results in a constant total local wiring resistance for lateral scaling and an increase that is linear in S for full cross-sectional scaling. These trends are plotted as the lower dashed and solid curves in Figure 2. Since bipolar chip sizes have increased as the transistor dimensions have decreased, global wire lengths remain constant or are increased. As shown in the upper dashed and solid curves of Figure 2, global line resistances increase linearly in S with lateral scaling and quadratically with full cross-sectional scaling. Large wiring resistance increases are a disadvantage, since bipolar circuit design is sensitive to current- and resistance-related (IR) voltage drops. A major source of capacitance in bipolar circuits is the wiring, and the switching speed of a transistor is affected by wire resistance and capacitance through an RC time constant [4]. Since full cross-sectional scaling decreases the insulator thickness between wiring layers and the silicon substrate, interlevel wiring and wire-to-substrate capacitances are increased. Full cross-sectional scaling leads to a rapidly increasing RC circuit delay [5], whereas this component of circuit delay increases more slowly with lateral scaling.

To minimize increases in current density, wire resistance, and interlevel capacitance, the lateral dimensions of the lines and spaces were reduced, wiring density was increased, and the vertical dimensions were left unchanged at 1.5 μm. New planarization and deposition techniques were used to process circuit features with an increase in aspect ratio. A new wiring metallurgy was developed consisting of an Al–2%Cu alloy sandwiched between thin layers of titanium to form highly reliable wiring layers with a sheet resistance of 21 m$\Omega/\square$. A reaction between titanium and aluminum yields thin layers of an intermetallic alloy which increases resistance to thermal-stress-induced void formation and to electromigration in lines and interconnection structures, and significantly improves wiring lifetimes compared to 3090™ circuits [8, 9].

This paper describes the four levels of metal interconnection with 1.6-μm minimum dimension lines on 3.0-μm pitch that were developed for bipolar ICs in Enterprise System/9000 processors. The bottom level is used primarily for local wiring with some global interconnections, while the second and third levels provide alternating wiring channels in the x and y directions to efficiently distribute power and route signals among all areas of the chip. The fourth level provides basic power distribution and signal routing to an "area array" of approximately 650 solder bumps which are used to "flip-chip" mount ICs to a thermal conduction ceramic package [10–13].



(a)



(b)

Figure 3

Cross section of the four-level interconnection structure. (a) SEM cross-sectional image. The bright areas in the metal features are copper-rich grains. The cross-section preparation left particles which appear as bright specks across the image. (b) Structural drawing. Conductive features are indicated by solid fill or cross-hatching. The metal interconnection structure is indicated by the cross-hatching, the emitter polysilicon by the solid fill, and the extrinsic base by the gray shading.

Interconnection design

A cross-sectional scanning electron microscope (SEM) image of the interconnection structure is shown in **Figure 3(a)**. **Figure 3(b)**, which is drawn approximately to scale, identifies the components of the interconnection structure. The first- through third-level lines are composed of 1.5-μm-thick Al–2%Cu and titanium intermetallic "sandwiches" and are patterned by lift-off processing [14]. The fourth-level metal is sputtered Al–3%Cu and has wider lines, less

stringent planarity requirements, and thicker metallurgy (2.3 μm) than the underlying levels. The fourth-level wires do not require Ti intermetallic stripes because current densities are too low for electromigration to occur. The contact, first-, and second-level insulator layers are fully planarized. To simplify processing, the third-level insulator layer is not fully planarized. The third-level insulator consists of a 3-μm-thick dual dielectric structure in which a thin plasma-enhanced chemical-vapor-deposited silicon nitride (PECVD Si_xN_y) layer is located beneath a sputtered silicon dioxide (SiO_2) layer.

The transistor emitter, base, and collector [labeled E, B, and C respectively in Figure 3(b)] are connected to the first-level wiring by "contact studs." The first-to-second and second-to-third-level wiring interconnections, or "plugs," are composed of metal deposited in etched vertical vias. The contact stud and the first-to-second and second-to-third-level plugs are fully planar, nearly vertical interlevel connections that can be stacked to maximize the wiring density [15–17]. The plugs may be partially misaligned with underlying and overlying wiring layers. This partial misalignment increases the tolerance to lithographical overlay variations and provides a significant gain in wiring density. When partial misalignment cannot be tolerated, compensation for the inherent registration variations of the lithographical alignment system is obtained by increasing the wiring linewidths or adding borders at the plug locations [17, 18]. The third-to-fourth-level wiring connections are made by etching sloped vias and depositing fourth-level metal into the vias. The sloped vias are larger than the vertical plugs used in the underlying levels, but wiring density is unaffected because of the wider dimensions of the fourth-level metal.

Interconnection processing

- *Stud and plug processing*

Two vertical connection processes were developed to meet different structural requirements for contact and interlevel connections. The contact stud level connects to the sensitive device contacts. The contact stud process is the first interconnection process developed at IBM that uses chemical–mechanical (designated as chem–mech) polishing; it was used for circuits in the 3090 system. This process was developed by combining earlier stud processing with chem–mech polishing planarization techniques [19]. It is called "cloisonné" because of its similarity to cloisonné jewelry-making techniques. The basic process sequence consists of forming free-standing studs, depositing an insulator, and planarizing the insulating layer by chem–mech polishing until the studs are exposed.

Interlevel plugs are connected to nearly planar metal lines, which makes them well suited to etched via and plug formation processes. The interlevel plug process [19, 20], which is called "damascene" for its similarities to the damascene technique used to decorate Damascus swords, consists of etching vertical vias in a planar insulator and then filling the vias with metal. Excess metal is removed and the metal is polished, using a selective chem–mech polishing process, until it is co-planar with the insulator surface.

Contact stud

The nominal contact stud height is 1.6 μm, but a 1.2-μm vertical height difference between the collector and emitter contacts produces a minimum separation of 0.5 μm between the first-level wiring and the emitter. The processing sequence used for forming contact studs with lift-off stencils is shown in **Figure 4**. The lift-off stencil consists of a baked planarizing polymer layer, an imaging photoresist layer, and a thin "release layer" deposited between the planarizing and imaging layers. The stencil planarizes much of the transistor structure topography and produces a smooth imaging layer for the photolithography process. The imaging photoresist layer is exposed, developed, and treated in a silylation bath [21]. Silicon from the silylation process masks the photoresist as an oxygen gas plasma RIE etches through the stencil layers [14].

The contact stud metallurgy is deposited through a patterned lift-off stencil, as illustrated in Figure 4(a). The contact metals consist of a layer of titanium beneath a 250-nm layer of chromium/chromium oxide cermet (Cr/CrO_x). The cermet acts as a barrier to aluminum transport into the transistor junctions [18]. All device contacts are made to platinum silicide except for the polysilicon emitter, because the silicide can penetrate into the emitter–base junction. An Al–Cu film is deposited onto the stencil, as shown in Figure 4(a), and excess metal is mechanically lifted off. By placing a release layer above the stencil, the stencil layer, which protects the studs, is not removed during lift-off. The stencil is then removed in a wet stripping process. Dual-dielectric Si_xN_y/SiO_2 layers are deposited onto the free-standing studs [Figure 4(b)] and the structure is planarized by chem–mech polishing, as shown in Figure 4(c).

The contact stud process decreases the first-level-to-substrate wiring capacitance [4] and, consequently, the wiring propagation delay time, which is proportional to an *RC* time constant. Previous circuit wiring [15] used channels of planar recessed oxidation [23] to isolate first-level wiring from silicon. Because long wires were routed above the channels and only short wires crossed over transistors, the number of wiring channels was reduced, and a compromise between transistor and first-level wiring densities was required. With contact studs, the first-level wiring is routed directly over the transistors, which nearly

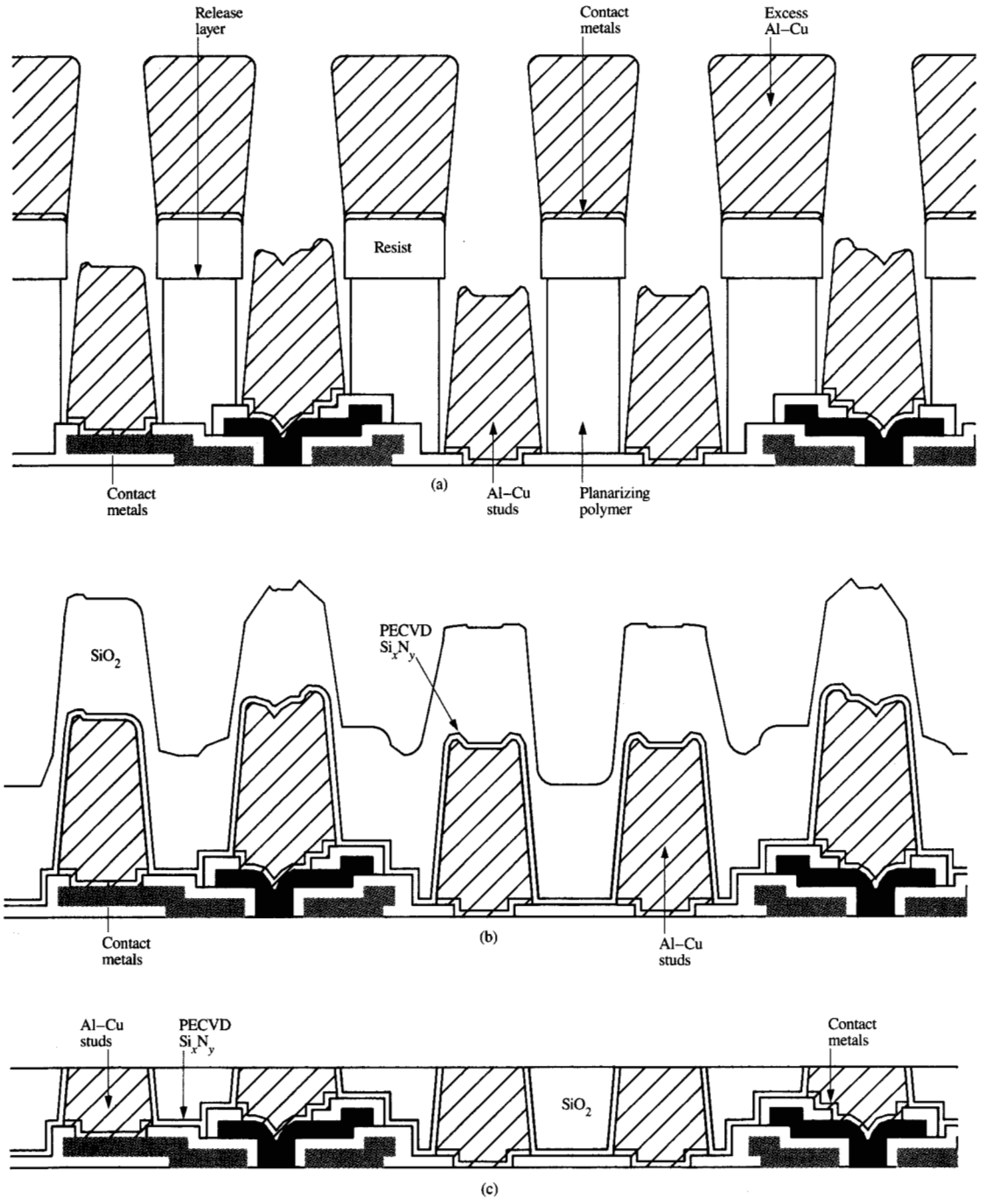


Figure 4

Schematic representation of contact stud formation. (a) Lift-off stencil formation, and contact and stud metal evaporation. (b) Metal and stencil lift-off, underlay dissolution, and insulator deposition. (c) Stud planarization.

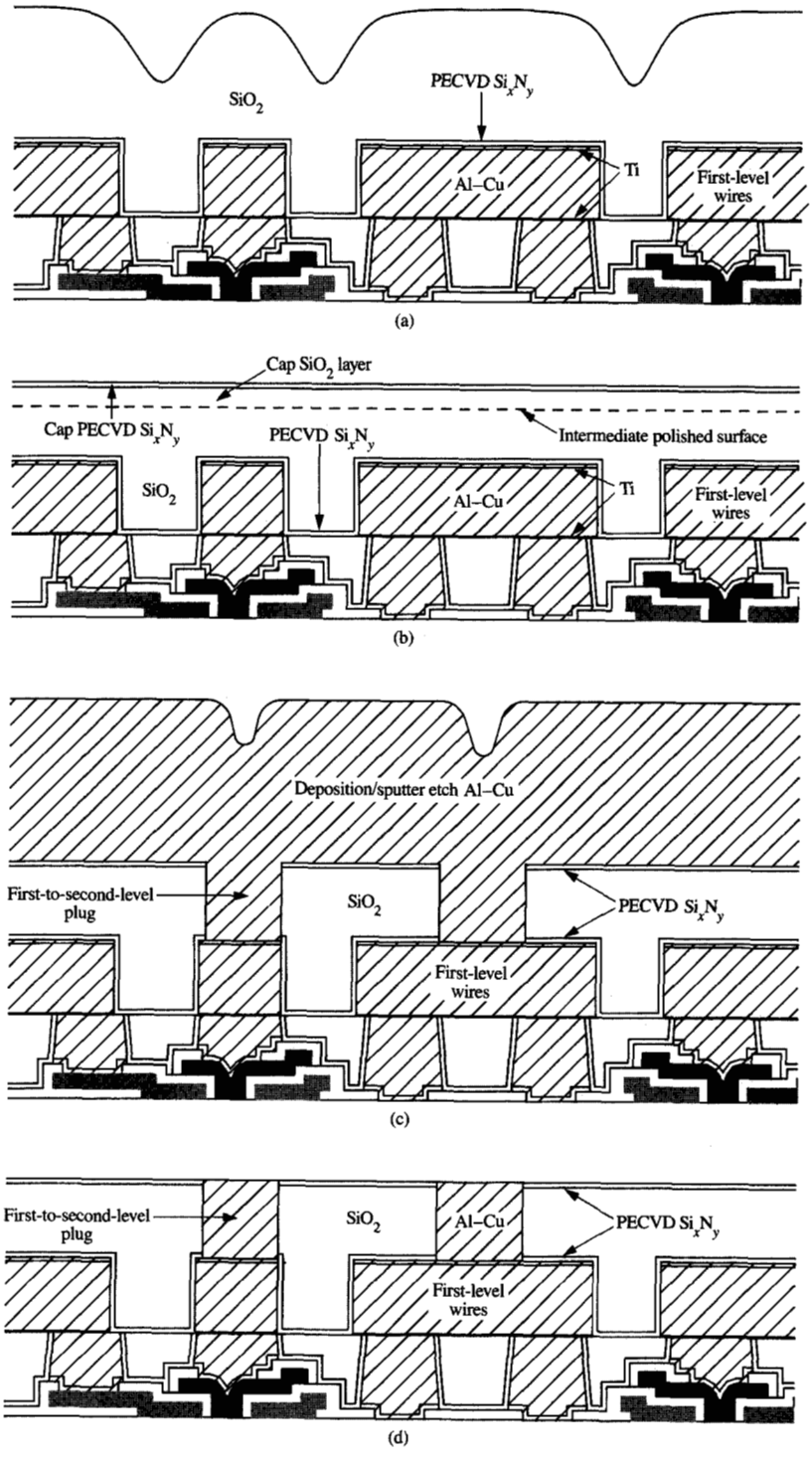


Figure 5

Schematic representation of interlevel plug formation. (a) Insulator deposition above metal wires. (b) SiO_2 planarization, and thin insulator cap; the dashed line represents the planarization surface. (c) Via etch to the underlying wires and metal deposition. (d) Plug planarization.

doubles the number of wiring channels and maintains low wiring capacitance levels. Improved planarity and elimination of the steep steps that first-level wiring traversed in previous processes improves metal integrity.

Interlevel damascene plug

The processing steps for forming interlevel studs are illustrated in **Figure 5**. A dual dielectric layer, which consists of a 100-nm Si_xN_y layer and an SiO_2 layer, is shown in Figure 5(a) deposited over the patterned wires. The SiO_2 is planarized by chem–mech polishing, which removes about 400 nm. A thin SiO_2 and Si_xN_y "cap" layer is then deposited. The planarized dual dielectric insulator is shown in Figure 5(b). The distance from the top of the first-level metal to the top of the insulator is designed to be 1.65 μm. Vertical vias are etched through the insulator to the underlying metal as described below. Although the nominal aspect ratio (ratio of depth to width) of the interlevel via is 1.03:1, the deposited Al–Cu metallurgy must be capable of filling deeper vias, since process variations result in vias with aspect ratios to 1.5:1.

Of the several planarizing metal deposition techniques available, which include high-temperature sputtering [24], partially ionized beam deposition [25, 26], deposition and sputter etch-back techniques [27], CVD [28], and laser melt reflow [29], a repetitive deposition/sputter etch process was selected to fill the vias with metal. The initial deposition step is a line-of-sight metal evaporation which ensures filling at the bottom of the via. Deposition is continued until more than half of the via is filled. Metal depositing on the insulator surface accumulates and projects laterally, thereby blocking subsequent metal deposition into the via. The blockage, which slopes inward in a conical shape with a gap at the via periphery, progressively worsens during metal deposition and must be reopened by a sputter etch step. Sputter etching opens the gap and redistributes metal from the via top and interior into the gap. The metal deposition/etch cycles are repeated and followed by a final metal evaporation cycle. The total metal thickness deposited is at least 2.5 times the via depth to ensure a void-free plug. The interlevel plug is shown in Figure 5(c) following Al/Cu deposition. Excess metal is removed by selectively chem–mech polishing to produce a planar Al–Cu plug, as shown in Figure 5(d).

An SEM micrograph of an interlevel plug that connects the first and second wiring levels is shown in **Figure 6**. The first-level metal structure was exposed by etching the insulator with a combination of reactive ion etching and wet etching in buffered hydrofluoric acid. The interlevel plug walls are vertical, and the second wiring level planarity is maintained as it passes over the plug. Yields are proprietary, and may be discussed at a later time; however, the general mechanisms by which this plug process affects yield and reliability can be discussed here. Wires that traverse discontinuous steps can develop seams and discontinuities in the wiring metal which affect yield and increase susceptibility to electromigration failures [7]. The interlevel plug process produces planar wires and interlevel connections without steps at interlevel vias, as shown in Figure 6. Yields critically depend on the structure and processing and the effects of contaminants and particles. Foreign materials adjacent to wire traces are encased in insulating layers which are planarized by polishing. By isolating the contaminants from the overlying wiring layer with a planar insulator, contributions to interlevel shorts are reduced, and yields are significantly improved in comparison to earlier processes. The metal polish process can leave metal particles trapped in depressed insulator defect regions, leading to intralevel and, occasionally, interlevel shorts.

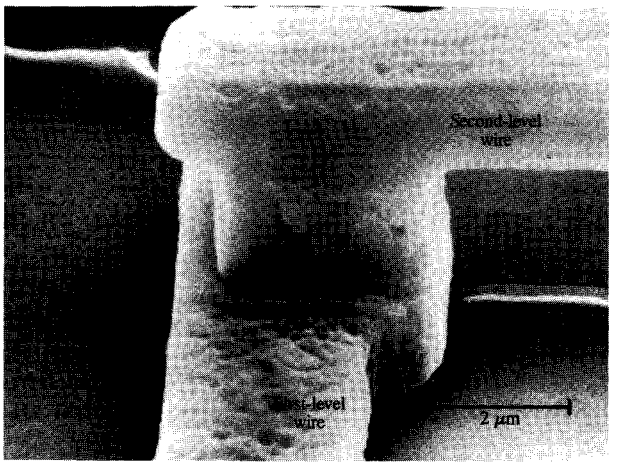


Figure 6

SEM micrograph of exposed first- and second-level wires with interlevel plug. The wiring levels and interlevel plug were formed, then the insulator was etched away to expose the metal features.

The cross-sectional area of the plugs formed by the via lithography and vertical etch yields a well-defined metal-to-metal contact area. *In situ* sputter cleaning of metal-to-metal interfaces and the absence of discontinuities and seams produces level-to-level plug resistances with small standard deviations. A typical distribution of plug resistance with a standard deviation of 3% is plotted in **Figure 7**. Vertical interlevel plugs optimize via-to-via spacings, and the pitch and density of the overlying wires are optimized by the vertical interlevel plugs while a 1.65-μm level-to-level spacing is maintained. The level-to-level spacing minimizes interlevel capacitive coupling and decreases the wiring capacitance that would otherwise contribute to reducing circuit switching speeds [4].

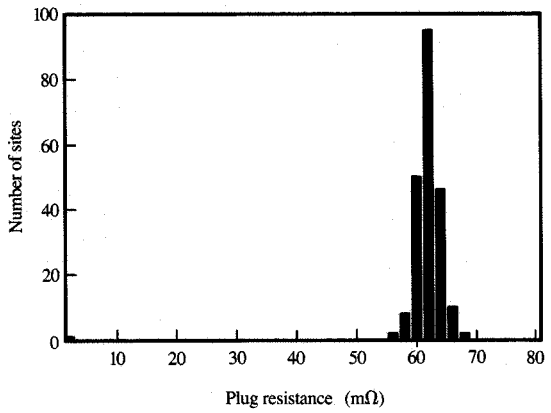


Figure 7

Typical distribution of plug resistance values for 32 000-plug chains. Measurements were made at 12 sites per wafer on 18 wafers. Data plotted = corrected resistance per plug.

- *Oxide RIE*

The insulator RIE process is a deep oxide etch which produces vias with high aspect ratios (ratio of via depth to diameter). The vias are nominally 1.5 μm deep, and the via sidewalls, designed to be within 5 degrees of vertical, are typically 1 to 2 degrees from vertical and do not have a negative sidewall slope or faceting at the rim. The photoresist mask is a silylated bilayer similar to the lift-off stencil. The photoresist is exposed, developed, and silylated. The photoresist pattern is transferred to the underlayer by a low-pressure oxygen RIE which results in a low process bias with minimal undercut. The thick photoresist stack masks the via etch in the subsequent oxide RIE step. Several successful deep oxide etch processes have been developed for the via etch with CF_4/O_2, $CF_4/CHF_3/Ar$, and $CHF_3/CF_4/He$ plasmas.

Oxide etching is complicated by a phenomenon first observed during development of this insulator etch and dubbed "RIE lag" [30]. RIE lag, which is presumably caused by incident ion scattering in the plasma sheath [31, 32], exhibits an aspect ratio (height/diameter) dependence on the etch rate for vias that are small in at least one of the lateral dimensions (e.g., narrow rectangular or small square vias). RIE lag causes a 5% to 10% decrease in etch rate for 1.6-μm vias relative to larger vias. Small vias must be etched to completion to remove etch residues without affecting profile variations in the larger vias. RIE lag decreases as operating pressures are lowered and photoresist thicknesses are decreased, but these changes produce rapid photoresist erosion and eventual loss, and via faceting.

- *Insulator processes*

Insulator deposition must be controlled to prevent voids from forming in the high-aspect-ratio gaps into which the insulators are deposited. At the contact level, the high-aspect-ratio gaps are present during insulator deposition between the 2.7-μm-high contact studs with minimum interstud spacing of 1.4 μm. For the first to third metal wiring levels, the metal height of 1.5 μm with a minimum design spacing of 1.4 μm produces a nominal aspect ratio of 1.07:1. Because statistical process variations can produce aspect ratios of 1.4:1, the sputtering process has been designed to fill gaps with aspect ratios of at least 1.5:1.

The dual dielectric is composed of a thin layer of Si_xN_y deposited in a standard PECVD system and of sputtered SiO_2 which is deposited in a rf-powered parallel-plate sputtering system. Sputtered oxide fills gaps with aspect ratios of at least 2.0:1 under conditions of heavy substrate bias [33]. The substrate bias causes resputtering of the oxide layer during deposition and leads to partial planarization and enhanced filling of the gaps. However, excessive resputtering causes faceting of the aluminum, and the eroded aluminum is redeposited into the sputtered SiO_2. Excessive resputtering of the contact-level insulator damages exposed portions of the underlying devices. Adequate filling of the gaps is attained without metal faceting or device damage by initially depositing a low-sputter-yield material such as Si_xN_y, by using multistep depositions, and by optimizing the sputtering power (deposition rate), substrate bias (resputtering rate), and rf frequency [33]. The sputtering process window must be controlled to avoid forming low-density insulator, contaminating oxide on the sidewalls, and creating large insulator voids. The PECVD silicon nitride is a low-sputter-yield material that protects the metal and/or underlying devices and, as the second layer of the dual dielectric, increases reliability by compensating for silicon dioxide layer defects [15, 34].

- *Chem–mech planarization processes*

Chem–mech polishing has been used for various device processing steps [35–37], but this is its first manufacturing application to planarize interconnections [38]. The front surface of a substrate is polished with a plastic pad saturated with a slurry containing abrasives and chemical additives. The surface of the material being polished is presumably converted chemically to a softer compound, which is then mechanically removed by the pad and slurry abrasive [39]. The removal rate depends on the pad material, abrasive, chemical additives in the slurry, material being removed, temperature, relative pad velocity, and pressure. Chem–mech polishing is used to planarize the interlevel insulator prior to formation of the interlevel via, to planarize the contact stud and insulator, and to planarize the interlevel plug metal.

Techniques described for planarizing insulators include deposition and etch-back [40], polymer planarization and etch-back [15], and spin-on glasses [41, 42]. The effectiveness of a planarization technique is measured by a characteristic planarization length, which is the largest feature size that is effectively planarized. In chem–mech polishing, the pressure dependence of the polishing rate produces planarized surface features, since high points on a surface develop more pressure and polish more rapidly. The planarization length is primarily determined by the elastic properties of the polishing pad. The planarization length for each pad material is approximately the distance from a topographical step to a point at which the contact pressure of the polishing pad returns to its nominal value [38]. This length varies between 50 μm and a few hundred μm, which makes polishing the most effective planarization technique in use. **Figure 8** is an SEM image of a section of interconnection wiring which illustrates the effectiveness of the insulator planarization.

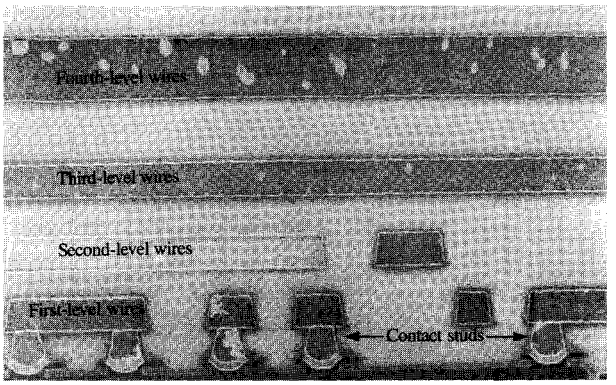


Figure 8

Cross-sectional SEM image of an area of the interconnection structure without interlevel studs. The degree of SiO_2 planarization can be seen in the top surfaces of the insulator layers above the first- and second-level wires. The bright areas in the metal features are copper-rich grains.

Contact stud and interlevel insulator planarization are similar except that metal and SiO_2 are polished together for the studs. The polishing rates for the two materials must be similar, and the slurry must not etch or corrode the Al–Cu studs. Critical process parameters include the stud metal height relative to the nominal insulator thickness and the elasticity of the polishing pad. If the stud metal is significantly higher than the nominal insulator thickness, the stud and covering insulator form a large protrusion which will be planarized early in the polishing cycle, thus making the process more controllable. The degree of pad stiffness affects the planarization behavior; a compromise is made because stiffer pads planarize more rapidly, while more elastic pads planarize uniformly a wider variation of stud widths and densities. Planarized contact studs are illustrated in Figures 3(a) and 8.

The plug metal planarization makes greater use of the chemical aspect of the chem–mech polishing mechanism. With adequate selectivity, the metal polishing process stops as the insulator layer is reached, and the pad bridges across the via metal. As the contact pressure of the pad on the plug metal decreases, the mechanical component ceases and metal removal stops. This leaves the plug surface nearly flush with the insulator surface. Several slurries have been used with different chemical additives. Typical slurries contain either colloidal silica or alumina abrasive, an oxidizer or natural dissolved oxygen, and other additives to adjust slurry pH or to improve material selectivity. The oxidizer changes the oxidation state of the metal and produces metal ions. To prevent wet etching or metal corrosion, the metal compounds that form must not be too soluble or the oxidation potential too aggressive. Ideally the surface product formed should be continuous and compact enough to limit the depth of the reaction and protect the metal against corrosion and should be soft enough to be readily removed. Aluminum and aluminum alloys are protected by aluminum oxide, a hard, dense film that is readily formed in neutral pH ranges. Aluminum oxide slows the polish rate and agglomerates as it is removed into large particles which can scratch and damage the surface. For aluminum polishing, the slurry must be formulated to either prevent aluminum oxide formation or control the size of the aluminum oxide agglomerates. Galvanic action of other metals in contact with the polished metal and the slurry affect metal etching and corrosion [43], while pH conditions that cause pit and crevice corrosion [44] must be avoided. Because Al–Cu is one of the most corrosion-sensitive aluminum alloys, corrosion prevention is particularly important.

- *Wiring processes*

The first- through third-level wiring processes are identical and have the same design rules: 1.5-μm-high lines with a minimum width of 1.6 μm on a minimum pitch of 3.0 μm. Chem–mech planarization prevents the topography from increasing with each wiring layer. A number of enhancements in the lift-off process were made to achieve these dimensions.

The lift-off stencil used to form these levels is similar to that for the contact stud stencil. The metallurgy consists of titanium intermetallic alloy layers which sandwich the main Al–2%Cu layer with the top titanium layer capped by a thin layer of Al–Cu. This structure is an improvement over the previous hafnium intermetallic alloy in a center-stripe geometry [8]. The intermetallic striped structures have outstanding electromigration resistance [8]. This is partially

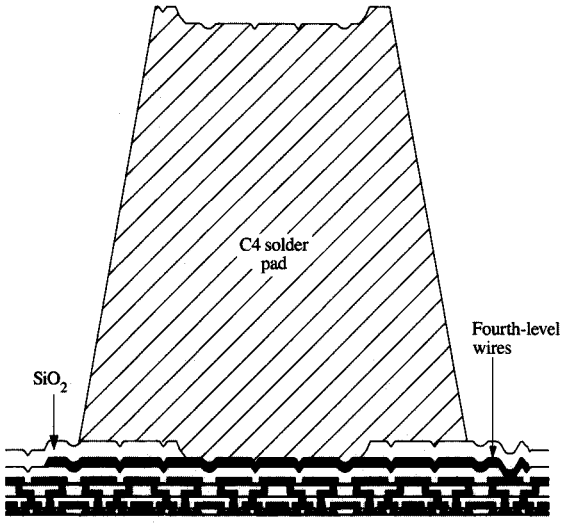


Figure 9

Schematic representation of C4 solder pad formation. A 4.3-μm SiO_2 layer is deposited above the fourth-level wires, and a sloped via is etched through at the contact points. The solder pad material is evaporated through a metal mask positioned above the wafer.

because the stripe provides a second conduction path. In accelerated lifetime tests, wiring-level test structures with intermetallic hafnium stripes form voids which grow and then dynamically reheal.* The voids appear to nucleate at the metal/insulator surface, but are typically confined by the hafnium center stripe to the upper half of the line.

The Ti–AlCu–Ti sandwich structure is used to minimize electromigration-induced void formation. Both titanium layers react with the Al–Cu to form high-melting-point $TiAl_3$ intermetallic layers. These layers reduce void formation by inhibiting nucleation at these surfaces. Thin Ti layers limit increases in line resistance and reduce electron-transport flux divergence at plugs. The electromigration lifetimes for Hf center-stripe and Ti sandwich structure lines are similar, but a reduced number of voids indicates that the Ti sandwich lines are more reliable. Although the lifetimes of wiring-level test structures are unchanged from those composed of the previous Hf-based metallurgy, electromigration tests on interconnection line-plug chains show an enhancement of two to three times. Resistance to thermal-stress-induced voids has also increased.

*E. Levine and J. Rathore, unpublished work, IBM East Fishkill facility, Hopewell Junction, NY 12533.

- *Area array solder interconnections*

The Enterprise System/9000 ICs use an extension of the controlled collapse chip connection (C4) process [18, 45] to connect the chip to the chip packaging. The solder pad materials remain unchanged, but the pad density has been significantly increased to approximately 650 solder connect terminals arranged in a 27 by 27 array. **Figure 9** shows the solder pad structure drawn approximately to scale. The solder pads are 100 μm in diameter and have a 230-μm center-to-center spacing. The solder pads are formed by first covering the fourth-level wires with 4.3 μm sputtered oxide. Resist for 50-μm-wide vias is exposed and developed and the vias are wet-etched through the oxide. The barrier metals and solder pads are evaporated through a metal contact mask. The thermal stability of the contact mask was improved to meet the tighter dimensional tolerances required for 125-mm wafers and to achieve the higher density of solder pads. Using the solder pad array, the ICs are flip-chip mounted by a solder-reflow process to a multichip package of alumina [12] or glass-ceramic [10]. The glass-ceramic packages are extremely dense, capable of mounting 121 ICs in an 11 by 11 array in a 125-mm-square package. When combined with the thermal conduction module (TCM) [46] and mounted on the system circuit boards, they provide a dense, highly thermally efficient packaging system.

Summary

The process of forming interconnections between transistors is no longer a simple series of wiring steps at the conclusion of a chip manufacturing process. Transistor switching speeds have increased to a point where signal delays caused by the interconnection structure are significant factors in the overall operating frequency, and an inability to interconnect all of the available transistors limits transistor density. The added complexity of interconnecting high densities of bipolar devices can negatively affect the overall manufacturing yield. By improving existing processing techniques and by introducing new techniques, it has been possible to produce a high-performance, dense, reliable, and highly planar interconnection structure that meets current needs without compromising materials, current-carrying capabilities, resistance, or signal delay.

A four-level metal wiring design and fabrication process was described. The introduction of chemical–mechanical polishing and the improvements in lift-off masking techniques, metal and insulator deposition, wiring metallurgy, and controlled collapse chip connection (C4) processing have produced interconnections with increased wiring density, improved planarity and reliability, input/output, and power connection density. Additional decreases in lateral patterning dimensions and increases in numbers of wiring levels will produce interconnections

between higher densities of bipolar devices and lead to further improvements in future system performance.

Acknowledgments

The structures and processes described here represent the individual efforts of hundreds of engineers, scientists, and technicians in both the East Fishkill facility and the Watson Research Center. We therefore acknowledge the efforts of the entire IBM team which made possible the successful production of this leading-edge chip wiring technology. We would like to thank A. Stainkamp and J. Gajda for SEM images.

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Received September 15, 1991; accepted for publication November 29, 1991

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