Improved performance of IBM Enterprise System/9000 bipolar logic chips

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The performance required for logic gate arrays by the IBM Enterprise System/9000™ (ES/9000™) family of water-cooled processors was obtained by redesigning chips that previously consisted of emitter-coupled logic (ECL) circuits. Multiple bipolar logic circuit families were implemented for the first time on a single IBM chip by using a modular cell approach. In 60% of the ECL circuits, ac coupling in ECL gates reduced the maximum operating power per ECL circuit on ES/9000 chips by 50% and decreased the signal delay per loaded gate by 30%, to 150 ps. About 10–20% of the remaining ECL circuits were replaced by differential current switches (DCS) which dissipated less power and improved the overall chip performance. Circuits to communicate between ECL and DCS circuit families and to improve DCS circuit reliability were included on the ES/9000 chips without affecting logic function density.

Introduction

Recent advances in bipolar logic semiconductor processing have increased circuit densities on a chip by an order of magnitude [1, 2]. However, packaging improvements have only doubled the quantity of heat that can be removed from a chip [3]. Consequently, a 50% reduction in the average operating power per logic circuit is required. Bipolar chips in IBM 3090™ processors are composed of ECL circuits which operate at high (15 mW/single phase) power and dissipate significant quantities of heat. In ES/9000 chips, a decrease in power per circuit increases the delays due to the load associated with the capacitance of interconnecting wires. The interconnections introduce a measure of circuit loading which doubles the sensitivity of a circuit's performance to fan-out and wire lengths. Vertical geometry device design improvements reduce delays with intrinsic, but not extrinsic, loads. Advanced metallurgies do not compensate for the high wiring capacitance that arises from the longer wire lengths due to a doubling of the ES/9000 chip areas. The performance of gate arrays required by the ES/9000 family of mainframe

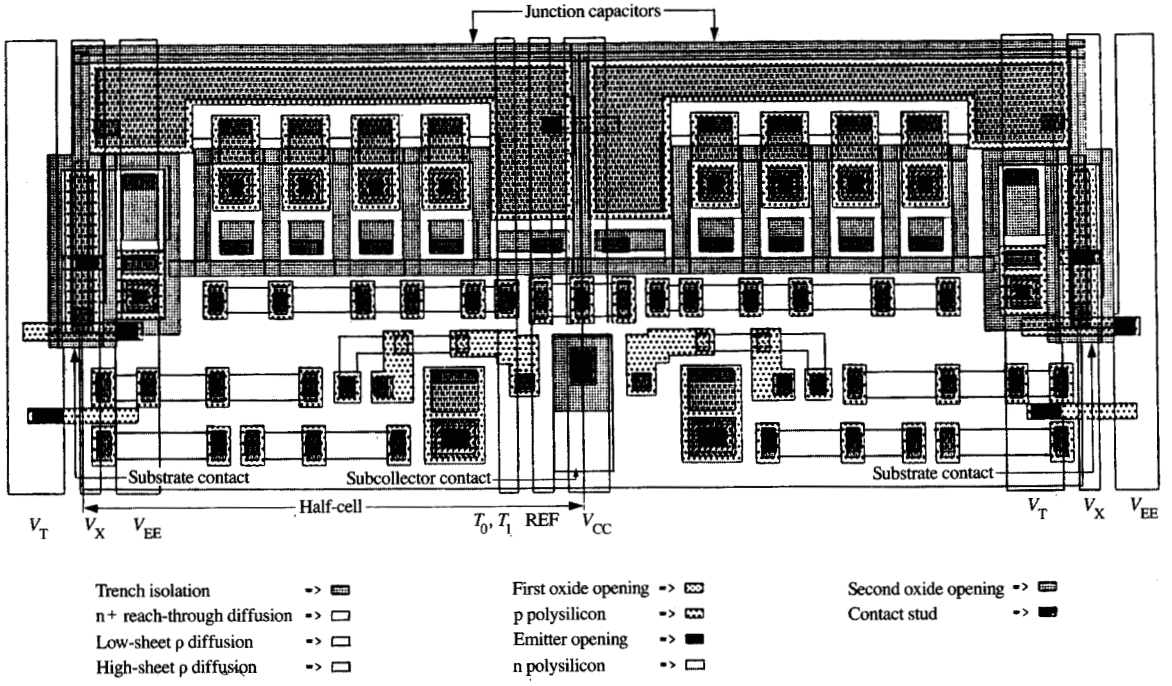

Figure 1

Layout of two half-cells. Inputs: REF, T_0, T_1, V_X. Power supplies: V_{CC}, V_{EE}, V_T.

computers was obtained after redesign of the chips and circuits.

Several ES/9000 chip and circuit design modifications were developed to regain performance with increased capacitive loads. ECL circuit delays due to wiring capacitance were reduced by ac coupling in ECL gates. A modular cell design on chips was used to accommodate multiple logic circuit families on a single chip. The power required to operate many logic functions with ECL circuits was lowered by replacing these circuits with multifunction DCS cascode circuits [4, 5]. The metal wiring capacitance delays in DCS circuits are smaller than in ECL circuits, which facilitates implementation of certain key logic functions with less power. Test circuits were included which improve DCS reliability [6]. Communications between the different logic families were accomplished with conversion circuits. The ac coupling in ECL circuits, the modular cell approach, and circuit topography allow mixtures of ECL and DCS circuits to be implemented on the same gate array, and enabled bipolar logic chips to meet ES/9000 system requirements with negligible effect on circuit density.

Gate array cell design

The primary building block in the modular cell design approach is the half-cell, which contains the devices required to implement a nonthreshold logic (NTL) two-input NOR gate [7, 8]. A four-input, two-output ECL OR and NOR gate requires two adjacent half-cells, and a DCS two-way multiplexer or latch can be built using four adjacent half-cells. Bipolar logic chips in ES/9000 processors are composed of 11 000 half-cells.

A cell layout consisting of two half-cells is shown in **Figure 1**. To optimize the design for multiple circuit families, multiple resistors connected in series in the cell provide a range of available resistances per resistive section. An isolated p/n junction depletion capacitor which is used for ac coupling in ECL circuits is shown at the top of Figure 1. The capacitor (called a "speedup" capacitor) is composed of a layer of p-type polysilicon deposited over a p-diffusion in an n-type epitaxial layer junction. The polysilicon increases the capacitance to 0.2 pF and provides a low-resistance contact to the bipolar junction. The entire capacitor resides beneath the first-level metal global wiring channels and does not increase the cell size.

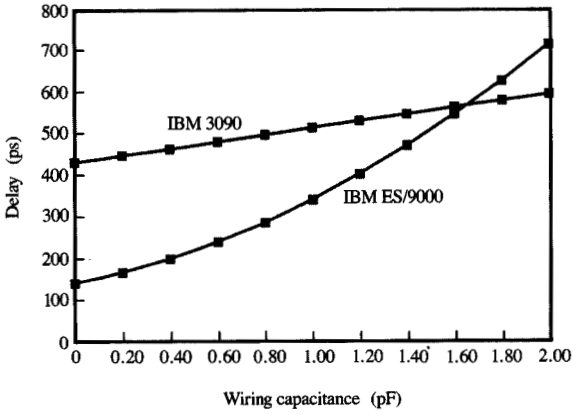

Figure 2

Dependence of ECL circuit delays on wiring capacitance. The high-power ECL circuits on ES/9000 and 3090 chips operate at 6 mW and 15 mW/single phase, respectively.

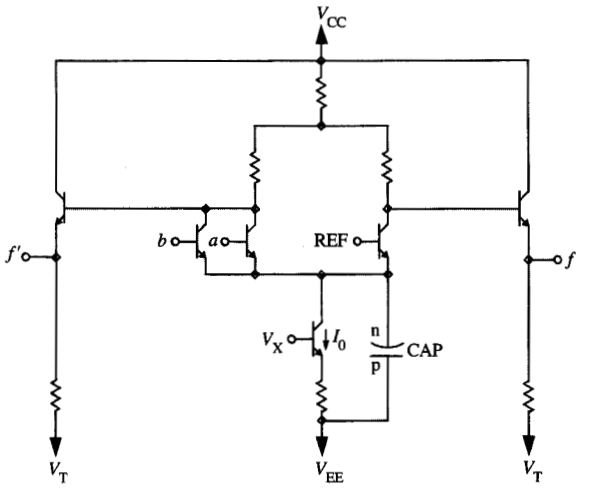

Figure 3

Dual-phase ECL gate designed with speedup capacitor (CAP) optional. Inputs: *a*, *b*, REF, V_X (current source reference voltage). Outputs: *f*, *f'*. Power supplies: V_{CC}, V_{EE}, V_T. I_0 current source.

ECL circuit enhancements

The performance of high-power ECL gates vs. wiring capacitance is compared for ES/9000 and 3090 systems in **Figure 2**. Delays in ES/9000 circuits increase with capacitance at nearly twice the rate of 3090 ECL circuits. This difference in circuit performance is due to a doubling of an emitter-follower pull-down resistance in ES/9000 ECL circuits [5] which is required to reduce power dissipation.

Circuit sensitivity to wiring capacitance is reduced by ac coupling in ECL gates [9]. Coupling is accomplished by placing a capacitor between a common-emitter node of an ECL gate and the power supply voltage, V_{EE}, as shown in **Figure 3**. The delay in ECL circuits due to large capacitive loads is dominated by a resistance-limited falling output signal. This signal must reach the circuit dc threshold voltage before switching occurs at the next circuit's input. The capacitor increases the *RC* time constant of the common-emitter node and prevents the emitter voltage from tracking the input voltage. Consequently, the input transistor turns off above the dc threshold voltage. This rise in dynamic threshold voltage dramatically reduces the effects of large wiring capacitance loads on gate input. A rising transition is less sensitive to loading and is relatively unaffected by the capacitor. **Figure 4** illustrates the signal delay improvement gained for a high-power ECL gate with a 0.3-pF load on its input and output.

The capacitor for ac coupling in ECL gates is selected as a compromise between performance gains and a

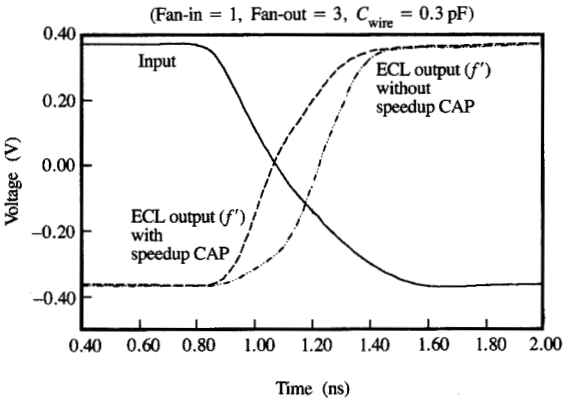

Figure 4

Effect of speedup capacitor on delay in a high-power ECL circuit.

reduction in ac noise tolerance. The capacitor produces a dip in the ac noise tolerance curve for narrow-pulse-width noise spikes. The capacitance is selected to keep the pulse width at which the dip occurs smaller than the pulse width of any chip-generated noise. As shown in **Figure 5**, a capacitance of 0.2 pF provides most of the performance gain capability of the capacitor without sacrificing noise

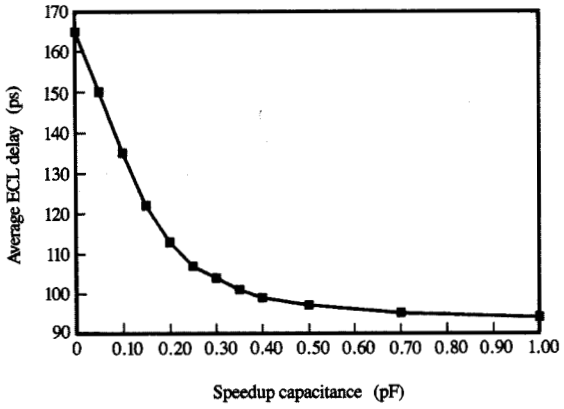

Figure 5

Dependence of average delay in very high-power ECL circuits on speedup capacitance.

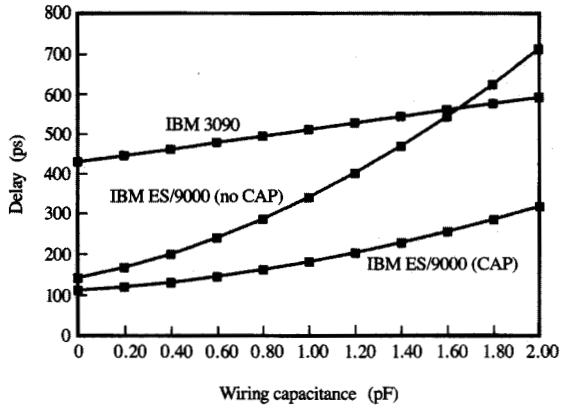

Figure 6

Dependence of high-power ECL circuit with speedup capacitance on wiring capacitance delays.

tolerance. In **Figure 6**, the sensitivity of an ECL gate to wiring capacitance is again shown, with a speedup capacitor added to the ES/9000 ECL circuit of Figure 2. Not only is the circuit delay decreased, but the sensitivity of the NOR gate to wiring capacitance is restored to that achieved by 3090 ECL circuits.

The speedup capacitor degrades the performance of an OR output from an ECL gate. When an OR output of the ECL gate is not used, as at output *f* in Figure 3, the capacitor is connected to the common-emitter node of a current switch. Since gates which use only a NOR output represent about 60% of the random logic (excluding latches) in the ES/9000 mainframe, introducing the capacitor to ECL circuits in these logic functions significantly improves overall chip performance.

For the OR output of ECL gates, the performance loss due to long wire lengths is regained by including very high-power (8 mW/single phase) ECL circuits in the circuit library. These circuits, which use pull-down resistances equal to those in high-power 3090 ECL gates, decrease the circuit delay sensitivity to wiring capacitance at the cost of increased power and reduced wired-OR output capability. These circuits were used when addition of a speedup capacitor was not applicable.

DCS logic circuits

The DCS circuits on ES/9000 bipolar logic chips are high-performance, two-level cascode, differential current switches with emitter-followers which are compatible with ES/9000 system power supply voltages ($V_{CC} - V_{EE} = 3.6$ V) [5]. This compatibility allows the circuit to retain a bipolar current source and emitter-followers. Only DCS circuits achieve delays less than 500 ps with a capacitive load as high as 0.3 pF while dissipating 1.2 mW. DCS circuits require about twice the area of an ECL circuit. However, high-performance DCS circuits perform multiple logic functions and therefore require less area than ECL circuits which perform similar functions [5]. The overall effect on chip area from replacing ECL with DCS circuits is negligible in water-cooled ES/9000 processors.

DCS has several advantages over ECL. The differential outputs in DCS circuits are dominated by fast-rising emitter-follower signals which are relatively insensitive to output loading. The sensitivity of the circuit to wiring capacitance is reduced by 25% in comparison to an ECL gate with the same emitter-follower current. DCS circuits are nearly impervious to the power-supply noise that disturbs ECL circuits as a result of the significant common-mode noise rejection provided by the differential inputs and outputs. Consequently, DCS can be designed with a voltage difference of only 200 mV between a logic "1" and a logic "0," compared to 750 mV for ECL. The biggest advantages DCS, or any cascode circuit, offers are a reduction in power dissipation and an increase in performance for functions such as shift register latches and XOR circuits [10]. In **Table 1**, the power dissipation and performance of high-power ECL and DCS gates are compared for several representative functions. A primary DCS application in ES/9000 Type 9021 water-cooled systems has been in latch operations. ECL latches are replaced with modified DCS latches which operate with ECL input and output signals. Air-cooled ES/9000 systems with DCS

circuits perform logic functions with reduced power. Chips with ultra-low-power (1.2 mW) DCS circuits have been fabricated which operate at a total power of <7 W.

A disadvantage of DCS circuits is their sensitivity to certain processing defects. A defect which generates a large resistance in a current source resistor of the circuit is easily detected in an ECL gate but requires extensive ac testing to be detected in a DCS gate. To improve the ability to detect faults [11] unique to differential circuits, the test circuit shown in **Figure 7** was added to the DCS gates [5, 12]. This circuit detects defects using simple dc "stuck-fault" testing. Components are available in four half-cells to add this circuit to DCS gates without affecting circuit density.

To illustrate the effects of a typical defect, assume that the collector contact of a current-source transistor has not opened. Without current flowing in the branches of the upper switches, both outputs will be in a logic "1" state. This defect is detected in an ECL gate, since a logic "0" state cannot be produced. In a DCS circuit, both gate outputs in a logic "1" state appear as a threshold signal to the next DCS gate. Small differences in device characteristics, such as resistances, could produce a large enough differential (5 mV) to appear as a valid output signal.

A second defect type occurs when outputs of two DCS circuits are shorted together. If one output is at a logic "1" state and the other is at a logic "0" state, the resulting voltage is a "wired-OR" which produces an "up" level 20–40 mV lower than a nominal "up" level. This is due to a connection between the two output resistors which doubles the emitter-follower transistor current.

The added test circuit detects these defect types. The test circuit in Figure 7 uses input control signals T_0 and T_1 to steer current between the OR and NOR collectors of the current switch. Feedback lowers one of the output voltages with respect to the other to produce a stuck fault.

Signal conversion

Signal conversion between ECL and DCS circuits utilizes converter circuits with the full logic capability of each family. By adjusting from ECL to DCS collector resistances, an ECL-to-DCS converter provides full ECL logic capability. A test-bias circuit is added, and the dual-phase ECL outputs are relabeled as differential outputs. For signal conversions from DCS to ECL, DCS collector resistors in a DCS circuit are replaced with ECL resistances. A six-transistor test network is replaced with a single test transistor. This replacement is acceptable, since the only defect that does not cause a detectable stuck fault results from shorted input transistors. The DCS outputs are relabeled as dual-phase outputs to complete the circuit.

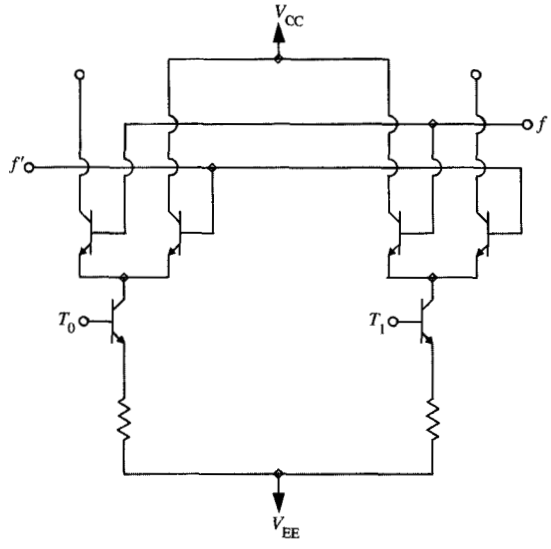

Figure 7

Test circuitry to enhance DCS gate reliability. Test signal inputs: T_0, T_1. DCS outputs: f, f'. Voltage supplies: V_{CC}, V_{EE}.

Table 1 Power and performance of 6-mW ECL and DCS circuits for typical logic functions.

Function	*ECL*		*DCS*	
	Power (mW)	*Performance* (ps)	*Power* (mW)	*Performance* (ps)
Shift register latch	40.5	384	12.2	397
8-W XOR	65.4	651	44.8	426
16-W multiplexer	66.6	369	31.3	310
16-W OR	9.4	190	34.8	280

Summary

Circuit design innovations have significantly advanced the performance and reliability of bipolar semiconductor chips. Multiple logic circuit families allow the logic to be designed with an optimum balance of power and performance. Low-power DCS circuits and ac-coupled ECL circuits reduce sensitivities to wiring capacitance loads to levels that allow the ES/9000 chips to meet their aggressive cycle time objectives. The circuitry necessary for easy conversion between circuit families has been developed. A new on-chip testing scheme reduces the effects of manufacturing defects and results in DCS circuits of high reliability.

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