Advancing the state of the art in high-performance logic and array technology

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High-speed silicon bipolar technology continues to meet the demands of integrated circuits for mainframe computers. IBM has developed an advanced bipolar logic and high-speed array technology for its Enterprise System/9000™ systems. This technology, code-named ATX-4, is composed of trench-isolated, double-polysilicon self-aligned bipolar devices, and has four fully planarized wiring levels with interlevel connecting studs. Chip fabrication has been implemented in 1-μm ground rules and is in full-scale manufacturing. ATX-4 represents a significant advance in providing higher-speed and lower-power logic at increased levels of integration compared with that of the ATX-1 technology used in previous generations. An overview of the design and integration of ATX-4 is discussed.

Introduction

The evolution of mainframe computing systems has led to significant changes in high-speed bipolar logic and array integrated circuit technology. Fundamental logic gate speed and the ability to minimize on-chip and off-chip delays is essential for providing the lowest system cycle time. Modern bipolar technology remains the best solution to this product requirement because of its fundamental advantages in intrinsic device switching speed and capacitance-driving capability. To achieve the lowest possible delay, the transistors and wiring must be designed to minimize parasitic resistances and capacitance. To reach these objectives, state-of-the-art bipolar devices consist of a polysilicon base contact which is self-aligned with the polysilicon emitter, a thin intrinsic base with an optimized collector doping profile, and deep-trench isolation [1–3]. Interconnections between devices must be designed for low parasitic capacitance and higher current and power densities. To accomplish this, electromigration-resistant wire levels are interconnected by vertical studs [4] incorporated into a fully planarized structure. The four independent wiring levels in ATX-4 chips minimize the path length between logic gates and significantly reduce the wiring capacitance.

This paper describes the design of the advanced high-performance bipolar logic and array chips used in the

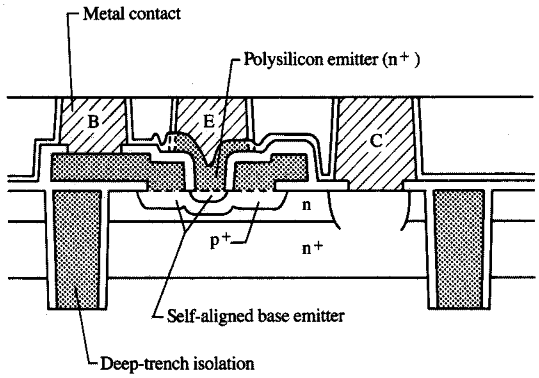

Figure 1

Schematic of an ATX-4 transistor. B = base, E = emitter, C = collector.

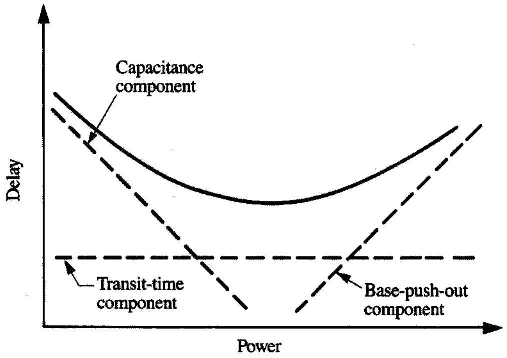

Figure 2

Log-log plot of a typical ECL circuit delay as a function of operating power.

IBM Enterprise System/9000™ (ES/9000™) mainframe computers. ATX-4 contains all of the advanced bipolar transistor and interconnecting elements mentioned above, which are implemented by utilizing 1-μm lithography. ATX-4 technology is currently used to manufacture logic, directory, and cache array chips; it represents a significant advance in speed and density over the previous ATX-1 technology.

Transistor structure and design

An ATX-4 transistor (shown schematically in **Figure 1**) can be characterized by three salient features: 1) a polysilicon base (B) contact self-aligned with the emitter opening, 2) deep-trench isolation, and 3) a polysilicon emitter (E) together with a very thin implanted intrinsic base and an optimized collector (C) doping profile. IBM has pioneered the development of these features since the 1970s [5–9]. Features 1 and 2 were used in bipolar technology for System/370™ 3090™ systems [10] introduced in 1989. Feature 3 is used for the first time in ATX-4.

Figure 2 illustrates the dependence of a typical emitter-coupled logic (ECL) circuit's delay on its operating power. The delay is dominated by three components [11]. The capacitance component is determined by lithography feature size tolerance and device structure. The base-push-out component, or Kirk effect [12], is a strong function of the device current density and the collector doping profile. These device features of the ATX-4 transistor have been designed to drastically reduce device delay.

- *Self-aligned device structure, deep-trench isolation, and capacitance delay component*

The self-alignment of the emitter opening with the polysilicon base contact greatly (by about a factor of 3 for 1-μm designs) reduces the base–collector junction area and its associated capacitances compared with conventional non-self-aligned devices. Deep-trench isolation permits transistors to be closely packed and minimizes the collector–substrate junction capacitance. The self-aligned device structure and trench isolation are central to achieving a small device size and the small capacitance delay component of the ATX-4 transistor.

The self-aligned device structure also provides a natural decoupling of the extrinsic-base and intrinsic-base processing steps. The polysilicon extrinsic base and the sidewall insulation, which separate the extrinsic base from the emitter in a self-aligned manner, are formed first. The intrinsic base is then formed by low-energy boron implantation followed by a minimal drive-in thermal cycle; it can be made very thin, with basewidths ≤150 nm.

As implemented in ATX-4 transistors, the bottom of the deep trench is open (see Figure 1) and is filled with heavily doped, p-type polysilicon. The p+ polysilicon serves as a front-side contact to the p-type substrate. The front-side substrate contact is required because chips are mounted face-down on the package module.

- *Polysilicon emitter and transit-time delay component*

The transit-time delay component is primarily determined by the intrinsic-base profile. In order to take advantage of the very thin intrinsic base formed by low-energy implantation, an arsenic-doped polysilicon emitter, with an emitter junction depth of 50 nm, is used in ATX-4 transistors. Since the minority hole diffusion length in the heavily doped emitter region is about 0.1–0.2 μm, the 50-nm single-crystal emitter region is transparent to the base current. It has been shown that for such shallow emitters, a polysilicon contact is essential to maintain current gain at levels necessary for circuit operation. This result is not achievable with a normal metal contact [13]. Thus, a polysilicon emitter allows shallow vertical profiles to be achieved without emitter–collector punchthrough or insufficient current gain.

- *Collector design and base-push-out delay component*

Base push-out occurs when the collector current density is larger than can be supported by the collector doping concentration. This causes the effective electrical base width to be much larger than the physical base width (the base is pushed out) and hence degrades the device and circuit speeds because of an increase in base transit time and stored charge. In bipolar scaling [14], the collector current density increases rapidly as device size shrinks. This in turn causes the base-push-out delay component to increase rapidly. Base push-out can be minimized by reducing the collector epitaxial layer thickness and/or increasing the collector doping concentration [15]. In ATX-4 transistors, the base-push-out component is minimized by optimizing the collector profile design through a locally implanted phosphorus region under the emitter area. As a result, the intrinsic switching speed of the transistor is doubled.

With these three transistor features, ATX-4 represents a state-of-the-art silicon bipolar transistor technology which is extendable to submicron dimensions in subsequent generations with improved lithography. The ATX-4 transistor provides a foundation for high-performance submicron silicon bipolar technology in future mainframe systems.

Lithography

All ATX-4 chips are fabricated using 1-μm ground rules. This is a significant advance over 1.5-μm ground rules used in ATX-1 chips. High-speed logic and array designs have a greater dependence on pattern overlay alignment to obtain maximum density and speed at a given critical dimension than on feature size. Thus, the 3σ minimum overlay tolerance for ATX-4 chips has been specified at 0.3 μm, which is significantly tighter than the 0.4–0.5 μm specified for most other 1-μm VLSI applications.

The ATX-4 chip is patterned with 5× step-and-repeat lithography tools which expose the photoresist using both the 436-nm g-line and the 405-nm h-line of the mercury emission spectrum. The tools are capable of submicron geometries and take advantage of site-by-site alignment or wafer mapping techniques to improve individual chip overlay tolerances. The planarization techniques featured in ATX-4 coupled with tight overlay specifications require particular attention to the stepper alignment capabilities, because the planarization processes remove topography on which alignment signals are conventionally generated. To evaluate stepper capabilities and realistically predict alignment performance on real product, a series of test wafer and resist structure types was defined to optimize the tools, alignment mark structures, and process conditions [16].

In addition to an optimum alignment strategy, the ATX-4 overlay requirements led to the development of a technique for measuring the latent image created in the photoresist by exposure with either g- or h-line steppers prior to image development. Using signal processing and enhancement algorithms, a tool was designed and implemented in the manufacturing line which provides real-time measurement of overlay on product hardware and allows improved tool set-up and control practices [17]. This capability has improved product overlay alignment and throughput by 20% and has a primary role in achieving ATX-4 lithography specifications.

The ES/9000 system utilizes several hundred logic and array chip part numbers. This large set of logic part numbers, which is supported through IBM Engineering Design Systems, is manufactured using direct-write E-beam lithography for the metal interconnection levels. The EL3 E-beam tool is capable of field sizes greater than 7 mm, minimum critical dimensions of 0.8 μm, and 3σ overlay tolerances of less than 0.2 μm [18]. Software was developed to allow an E-beam lithography exposure to be matched to previously exposed levels using stepper lithography and to correct for wafer and within-field distortions created by prior processing.

In summary, the lithographic strategy and design rule for the ATX-4 chips in which a state-of-the-art overlay and image size tolerance was obtained has been crucial to achieving minimum device delays and maximum wirability and circuit density.

Chip interconnections

Four-level wiring capability is a major factor in the overall performance and reliability of the ES/9000 systems. The ten meters of integrated wiring on a single 7-mm × 7-mm logic chip with 648 I/O C-4 (controlled collapse chip connection) pads should be viewed as an important extension of the total system packaging. With the large improvement in the intrinsic performance of the ATX-4 transistor, circuit delays which are due to chip wiring capacitance and resistance become more important. This is illustrated in **Figure 3**. For the ATX-4 logic chips, about one fourth of the on-chip delay is attributable to chip wiring. **Figure 4** shows the ATX-4 transistor together with four levels of interconnecting wires. The use of four levels of wiring is key to achieving this low wiring delay. The extra wiring level has shortened the average wire length of

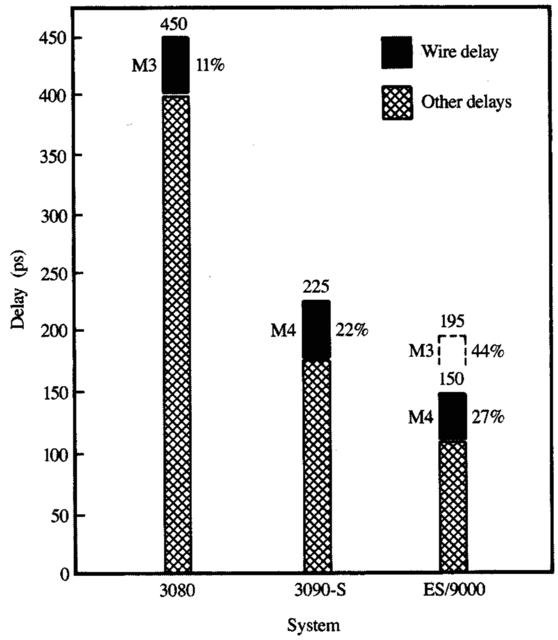

Figure 3

Relative contributions of wiring and silicon device to the on-chip propagation delay in three generations of IBM computers.

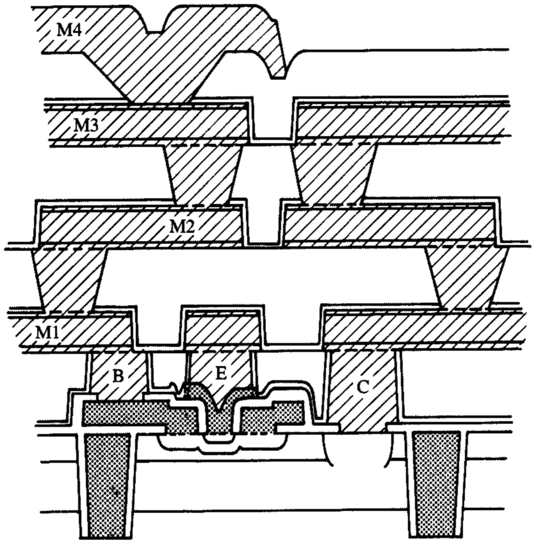

Figure 4

ATX-4 transistor with four-level interconnect wiring. B = base, E = emitter, C = collector.

conventional three-level-wired chips by one half. The complexity of fabricating four levels of chip wiring has also grown to the point that it now exceeds that of the silicon device and resistor. A major part of this increased complexity is due to an added emphasis on reliability and manufacturability in the four-level wiring design.

The current four-level system evolved from improvements made in the three-level metallization of IBM 3080 and 3090 systems [19] which have been retained in ATX-4 chips. These improvements are electromigration-enhanced Al–Cu and dual dielectric insulation.

Electromigration-enhanced Al–Cu

A 70× improvement in electromigration lifetime of aluminum wiring realized from adding about 4% Cu [20] was found to be less effective as lines narrowed to 1 μm [21]. It was subsequently discovered that transition metal layers such as Hf, Ti, or Cr, which react with Al to form aluminide intermetallic compounds, improve the lifetime of narrow AlCu lines by as much as two orders of magnitude [21]. This innovation was first used in 3090 system three-level chips as a second-level AlCu–Hf–AlCu film and was included in later four-level devices. The latest four-level structures use an inverted Ti–AlCu–Ti sandwich structure. This structure is equivalent in electromigration resistance to a Hf sandwich but appears to be more immune to void formation under conditions which create thermal-stress-induced voids. This allows current density design limits to be raised as high as 500 000 A/cm^2 without increasing electromigration wear-out failure rates.

Dual dielectric insulation

Early 3080 system product showed that a principal weakness in three-level wiring was that interlevel oxide shorts developed with time. This phenomenon was attributed to pinhole defects and embedded conductive particles in the SiO_2 film which caused the dielectric to deteriorate under stress. This problem was minimized by overlaying the rf-sputtered SiO_2 film of the interlayer dielectric with a 250-nm layer of plasma-enhanced chemically vapor-deposited (PECVD) SiN to form a much more reliable dielectric layer [22].

Four-level metal interconnections were developed to obtain greater integrated circuit productivity per wafer, improve wirability, and reduce wire length. Analysis of three-level logic chips showed that only about 30% of the surface of a chip was active logic cell area; the rest was simply a "wiring platform." If the logic cells could be brought together into close proximity, or "brickwalled," and vertical wires (studs) could be used to bring intercell wiring to the second and third levels, the chip circuit density could be significantly increased [23].

The development of successful four-level-metal fabrication progressed with advances in processing in three evolutionary stages. Each stage incorporated vertical, interlevel metal studs with small cross-sectional areas instead of conventional tapered vias. Each wiring level was planarized to allow the same pitch wiring at each of the first three levels instead of the normal practice of relaxing wiring pitch at each subsequent level because of increased topography. The processing changes which evolved at each stage were 1) etch-back planarization with photoresist; 2) chem–mech polishing planarization; 3) damascene studs.

Etch-back planarization with photoresist Studs were initially formed by lift-off, which has been the predominant IBM thin-film-line fabrication technique since the mid-1970s. The planarization of dielectric layers was achieved by first leveling the topography created by sputtering SiO_2 over studded lines with multiple layers of photoresist. The combination of the planarized photoresist and buried SiO_2 was then etched back with appropriate RIE gases which remove both materials at approximately equal rates. The photoresist, a sacrificial layer, was totally removed. The remaining SiO_2 and Al studs were planarized. A PECVD SiN film was deposited to form a dual dielectric layer, and shallow vias were etched through this layer to the deepest studs.

Using this methodology, the first IBM four-level-metal chips were successfully fabricated and shipped to numerous internal customers for the AS/400®, DASD, and other applications. The chips had as many as 12 000 bipolar circuits on a 7-mm × 7-mm chip, and as many as 762 C-4 solder connections [22].

Chem–mech polishing planarization A low-cost chem–mech polishing technique [24] was then developed which provided greater planarity. It combined chemical and abrasive polishing to level the dielectric layer and expose the studs [25]. Contact-level studs were concurrently introduced to planarize the silicon masterslice topography. This permitted the finest wiring pitches to be used for "book" or intracell first-level wiring. This methodology was used for fabricating the four-level-metal logic chips for the 3090 system during the late 1980s.

Damascene studs The third step in the evolution of the current four-level-metal process was to invert the stud fabrication technique. It involved etching stud holes in a deposited dielectric film, polishing the film to the proper interlevel thickness, and then filling the holes with metal [22]. Excess metal was polished away to make the top of the metal stud flush with the insulator. We have referred to this method as the "damascene stud" method because of its strong similarity to the damascene jewelry-patterning technique. The previously described system, or studs-up polishing method, is the analog to a "cloisonné" jewelry-patterning technique.

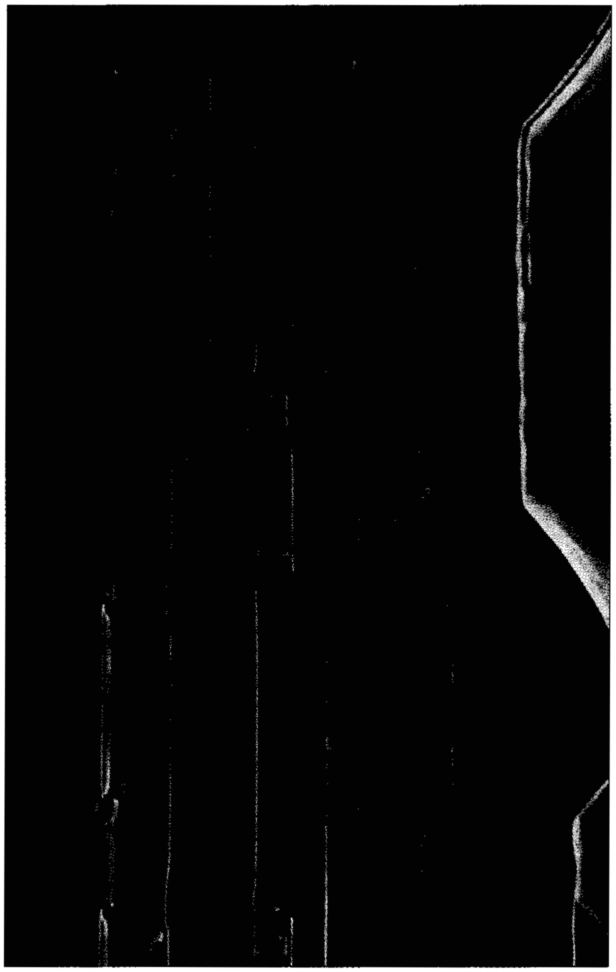

Figure 5

Metallographic cross section of four-level wiring on an ATX-4 chip, illustrating damascene studs and chem–mech planarization.

The principal advantages of damascene stud fabrication are that the shallow via topography etched in SiN is avoided, the manufacturing hazards of bending or breaking the fine lift-off studs are absent, and the full cross-sectional area at the exposed tip of the studs is retained, minimizing resistance and increasing yield and reliability. To implement this stud-fabrication technique, RIE processes were required to make stud holes that were different in area and depth. Then, a deposition process was needed to fill these holes with metal. A repetitive deposition/rf etching or "dep-etch" hole-fill sequence was developed that satisfied these requirements [26]. A metallographic cross section of ATX-4 chip wiring is shown in **Figure 5**. This damascene stud processing is used for manufacturing ATX-4 logic and array chips used in ES/9000 systems.

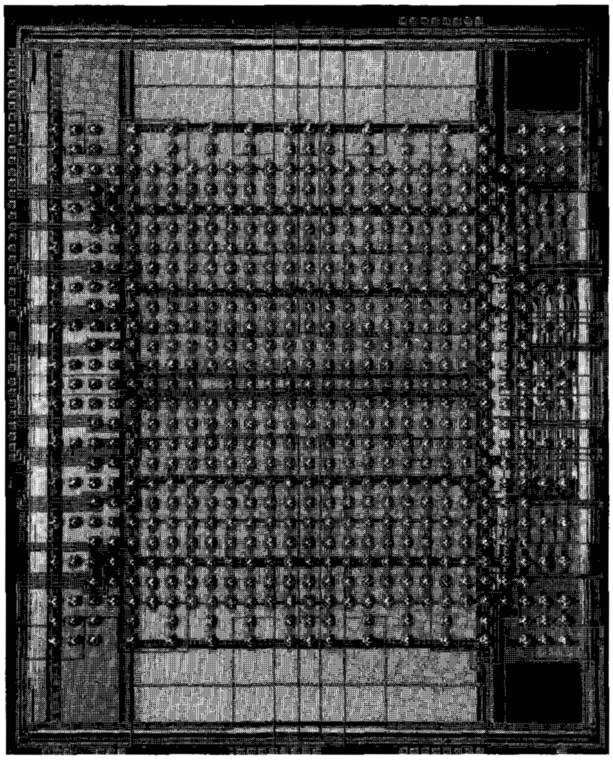

Figure 6

Photograph of a 64KB SRAM array chip with more than 600 C-4 pads.

With continuing improvement and modification, this processing should be extendable into the submicron era of the 90s.

I/O terminal connection system

Connecting a chip to the package is accomplished with a C-4 solder bump array [27]. According to Rent's rule, additional I/O terminations are required for more random logic circuits [28]. The number of C-4 solder bump arrays has increased from 11 × 11 in the 3080 system, to 17 × 17 in the 3090 system, and to 27 × 27 in ES/9000 systems. As many as 648 pads are used in the ATX-4 chip set. Solder bumps 4 mils in diameter are located on 9-mil centers. The mating substrate may be multilayer alumina in the low-end machines of System/390® or the newly introduced multilayer glass-ceramic material at the high end. The glass-ceramic material [29] was purposely designed to match the thermal expansivity of silicon. Therefore, many of the previous constraints on chip size which were driven by the thermal cycle fatigue capability of the solder bumps no longer exist, and chip sizes for the future become essentially unbounded on this substrate material. **Figure 6** shows a 64Kb SRAM array chip with C-4 pads.

Concluding remarks

The ATX-4 technology integrates advances in both transistor and interconnection design and processing and provides a high-reliability, high-performance bipolar engine for the ES/9000 systems. The ATX-4-based product set includes bipolar logic chips with circuit densities nearly five times those of ATX-1. Logic speed has been enhanced to 150 picoseconds in loaded circuits. Both differential current switch (DCS) and ECL circuits are available on the same ATX-4 logic chip, which allows considerable speed/power flexibility in optimizing circuit functionality. High-speed memory arrays were developed in the ATX-4 technology with densities up to 64 000 bits and a nominal access time of 2.5 ns. Direct attachment of chips to air- and water-cooled modules is accomplished by extending IBM C-4 interconnection solder technology, which has more than 600 solder connections available on each chip.

It is expected that the ATX-4 technology, with incremental improvements, will provide a sound basis for meeting the needs of high-end computing systems throughout the next decade.

References

1. D. D. Tang, P. M. Solomon, T. H. Ning, R. D. Isaac, and R. E. Burger, "1.25 μm Deep-Groove-Isolated Self-Aligned Bipolar Circuits," *IEEE J. Solid-State Circuits* **SC-17**, 925–931 (1982).
2. K. Ueno, H. Goto, E. Sugiyama, and H. Tsunoi, "A Sub-40 ps ECL Circuit at a Switching Current of 1.28 mA," *IEDM Tech. Digest*, pp. 371–374 (1987).
3. M. Sugiyama, H. Takemura, C. Ogawa, T. Tashiro, T. Morikawa, and M. Nakamae, "A 40GHz *fr* Si Bipolar Transistor LSI Technology," *IEDM Tech. Digest*, pp. 221–224 (1989).
4. T. A. Bartush, "A Four-Level Wiring Process for Semiconductor Chips," *Proceedings of the Fourth IEEE Multilevel Interconnection Conference*, 1987, p. 41.
5. T. H. Ning and H. N. Yu, "Utilizing Polysilicon Diffusion Sources and Special Masking Techniques," U.S. Patent 4,157,269, June 5, 1979.
6. N. G. Anantha, H. S. Bhatia, and J. L. Walsh, "High Performance Bipolar Device and Method for Making Same," U.S. Patent 4,160,991, July 10, 1979.
7. J. A. Bondur and H. B. Pogge, "Method for Forming Isolated Regions of Silicon Utilizing Reactive Ion Etching," U.S. Patent 4,104,086, August 1, 1978.
8. T. H. Ning, R. D. Isaac, P. M. Solomon, D. D. Tang, and H. N. Yu, "Self-Aligned NPN Bipolar Transistors," *IEDM Tech. Digest*, pp. 823–824 (1980).
9. D. D. Tang, K. P. MacWilliams, and P. M. Solomon, "Effects of Collector Epitaxial Layer on the Switching Speed of High-Performance Bipolar Transistors," *IEEE Electron Device Lett.* **EDL-4**, 17 (1983).
10. Y. H. Chan, J. L. Brown, R. H. Nijhuis, C. R. Rivadeneira, and J. R. Struk, "A 3ns 32K Bipolar RAM," *Proceedings of the 1986 IEEE International Solid-State Circuits Conference*, pp. 210–211.
11. D. D. Tang and P. M. Solomon, "Bipolar Transistor Design for Optimized Power-Delay Logic Circuits," *IEEE J. Solid-State Circuits* **SC-14**, 679–684 (1979).

12. C. T. Kirk, "A Theory of Transistor Cutoff Frequency Fall-Off at High Current Density," *IRE Trans. Electron Devices* **ED-9**, 164 (1962).
13. T. H. Ning and R. D. Isaac, "Effect of Emitter Contact on Current Gain of Silicon Bipolar Devices," *IEEE Trans. Electron Devices* **ED-27**, 2051–2055 (1980).
14. P. M. Solomon and D. D. Tang, "Bipolar Circuit Scaling," *Proceedings of the 1979 IEEE Solid-State Circuits Conference*, pp. 86–87.
15. H. Goto, Y. Nagase, T. Takadam, A. Tahara, and Y. Momma, "Analysis of Highly-Doped Collector Transistors by Using Two-Dimensional Process/Device Simulation and Its Application in ECL Circuits," *IEEE Trans. Electron Devices* **38**, 1840–1844 (1991).
16. J. D. Buckley, "An Advanced H-Line Stepper," *Solid State Technol.* **30**, 7 (1987).
17. W. D. Hopewell, J. C. Shaw, T. G. Van Kessel, and R. R. Jackson, "Latent-Image Based In-Situ Closed-Loop Control of Lithography Tools," U.S. Patent filed March 2, 1990.
18. H. C. Pfeiffer, T. R. Groves, and T. H. Newman, "High-Throughput, High-Resolution Electron Beam Lithography," *IBM J. Res. Develop.* **32**, 494–501 (1988).
19. L. J. Fried, J. Havas, J. S. Lechaton, J. S. Logan, G. Paal, and P. A. Totta, "A VLSI Bipolar Metallization Design with Three-Level Wiring and Area Array Solder Connections," *IBM J. Res. Develop.* **26**, 362–371 (1982).
20. I. Ames, F. M. d'Heurle, and R. E. Horstmann, "Reduction of Electromigration in Aluminum Films by Copper Doping," *IBM J. Res. Develop.* **14**, 461 (1970).
21. P. S. Ho, J. K. Howard, and J. F. White, "Intermetallic Compounds of Al and Transition Metals: Effect of Electromigration in 1–2μm-Wide Lines," *J. Appl. Phys.* **49**, 4083 (1978).
22. G. S. Gati, A. P. Lee, G. C. Schwartz, and C. L. Standley, "Composite Insulator Structure," U.S. Patent 4,601,939, July 22, 1986.
23. S. Brenner, T. A. Bartush, D. J. Swietek, D. C. Banker, F. J. Crispi, D. J. Delotto, D. L. Merrill, J. P. Norsworthy, M.-N. Shen, and C. D. Waggoner, *Proceedings of the 1983 IEEE International Solid-State Circuits Conference*, p. 152.
24. K. Beyer, W. Guthrie, S. Makarewicz, E. Mendel, W. Patrick, K. Perry, W. Pliskin, J. Riseman, P. Schaible, and C. Standley, "Chem-Mech Polishing Method for Producing Coplanar Metal/Insulator Films on a Substrate," U.S. Patent 4,944,836, July 31, 1990.
25. W. L. Guthrie, W. J. Patrick, E. Levine, H. C. Jones, E. A. Mehter, T. F. Houghton, G. T. Chiu, and M. A. Fury, "A Four-Level VLSI Bipolar Metallization Design with Chemical-Mechanical Planarization," *IBM J. Res. Develop.* **36**, 845–857 (1992, this issue).
26. H. P. Bader and M. A. Lardon, "A New Metallization Technique for Very Large Scale Integrated Structures: Experiments and Computer Simulation," *J. Vac. Sci. Technol. B* **4**, 833 (1986).
27. L. S. Goldmann and P. A. Totta, "Area Array Solder Interconnections for VLSI," *Solid State Technol.* **26**, 91 (1983).
28. *Microelectronics Packaging Handbook*, R. R. Tummala and E. J. Rymaszewski, Eds., Van Nostrand Reinhold, New York, 1989.
29. R. R. Tummala, A. H. Kumar, and P. W. McMillan, "Glass Ceramic Structures and Sintered Multilayer Substrates Thereof with Circuit Patterns of Gold, Silver or Copper," U.S. Patent 4,301,324, 1981.

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