Preface

IBM recently introduced a family of large-scale processors known as Enterprise System/9000 (ES/9000). This issue of the *IBM Journal of Research and Development* describes many of the technical advances made in semiconductor and packaging technologies used in these processors. The preceding issue of the *Journal* focused on System/390 architecture and on ES/9000 processor and power/thermal system designs, while the ES/9000 air-cooled processors were described in an earlier issue (*IBM Journal of Research and Development* **35,** No. 3, 1991).

Bipolar circuit densities on ES/9000 processor chips increased nearly fivefold, and logic speed per loaded gate improved by 30% to 150 ps when compared with chips from IBM 3090 processors. These advances were achieved with trench-isolated, bipolar transistors in which polysilicon base contacts were self-aligned with polysilicon emitters. Interconnections between devices were made with four fully planarized metal wiring levels and metal studs between the levels. The chips were fabricated using 1-μm ground rules. The overlay alignment tolerance of a lithographic pattern on a chip, which affects the design of high-speed logic and arrays, was specified at 0.3 μm, which is much tighter than the 0.4–0.5-μm tolerance that is generally used in the industry for 1-μm VLSI applications. The reliability of interconnecting large numbers of devices on a single integrated circuit chip was improved by planarizing insulators and metals using chemical–mechanical polishing processes, by a novel contact stud structure, and by a Ti-clad Al–Cu metallurgy. The maximum operating power per emitter-coupled logic (ECL) circuit was lowered by ac coupling in ECL gates and by replacing some ECL circuits with differential current switches (DCSs), which dissipate less power and increase the overall chip performance. Multiple bipolar logic circuit families were implemented for the first time on a single IBM chip by using a modular cell approach. Circuits that communicated between ECL and DCS circuit families and circuits that improved DCS reliability were included on the ES/9000 chips without affecting logic function density. Other specialized circuits introduced into these processors include fast static memory cells using bipolar transistors which provide 8-ns write times while increasing immunity from soft errors. The ES/9000 processors were the first IBM systems to transmit clock oscillator signals to logic and array chips which then generated signals within each chip to control the execution of sequential functions. By using customized clock designs with advanced circuits that increased the clock pulse width accuracy, clock frequencies greater than 100 MHz were achieved in the high end of the ES/9000 processor family.

The packaging technology in IBM processors was significantly enhanced in electrical performance, interconnection density, and cooling capability in comparison to earlier systems. In the advanced thermal conduction module (TCM) of the ES/9000 Models 820 and 900, the multilayer alumina/molybdenum substrate was replaced by a substrate based on the crystallization of a unique glass that formed a glass-ceramic with a dielectric constant of 5.0 compared to 9.4 for alumina; and molybdenum conductors were replaced with copper. The copper conductors exhibited a threefold improvement in electrical conductivity over earlier designs. The thermal expansion of the new multilayer substrate, less than 30×10^{-7}/°C, closely matched that of the silicon chips that were solder-bonded to it, thereby enhancing the fatigue life of the associated 648 chip-to-substrate connections. A novel sintering process, developed for the glass-ceramic/copper substrate, provided excellent dimensional control and facilitated the closest placement of metal vias in the industry. The substrate consisted of a sintered composite of 63 glass-ceramic layers, each metallized with copper, and contained an overlying polyimide-copper thin-film layer. It measured 127.5 mm square, supported up to 121 logic and memory array chips, and provided a wiring density of 844 cm/cm^2, the highest that any multilayer packaging substrate has achieved to date in the industry. The number of solder terminal pads on 3090 processor chips was doubled on an ES/9000 chip surface to provide a controlled collapse chip connection (C4) to a substrate. Inverted chips were mounted on a substrate by the flip-chip process which, when combined with the 1.0-μm product design rule, provided the maximum circuit density achieved to date. The switching noise was reduced significantly by the use of decoupling capacitors flip-chip bonded to the substrate.

In the ES/9000 processors, six TCMs were mounted on a 22-layer glass–epoxy circuit board which measured 60 cm × 70 cm. Each TCM supported more than five times the circuits used by TCMs in previous IBM 3090 processors. The new TCMs contained an aggregate of 16 632 pin connections between their modules and their circuit board. Additionally, 3600 terminals were provided on the board for cable connections to other boards. The board also distributed power to each module and supported more than one kilometer of internal wiring. Substrate cooling in thermal conduction modules (TCMs), discussed in the previous issue of the *Journal,* was

enhanced to accommodate the highest power density (17.0 W/cm^2) in the industry achieved to date at a substrate level. The heat-transfer capacity of the water-cooled pistons in the TCMs was increased by tapering the piston faces to improve contact at chip surfaces, permitting power densities in excess of 60 W/cm^2 at the chip level. The pistons, which were aluminum in the 3090 systems, are now made of copper, which has twice the conductivity.

The combination of new technology elements with advanced design rules produced the highest-yielding and most reliable introduction of new technology in IBM history. The papers in this issue describe many of the important device and packaging advances incorporated in the ES/9000 family of processors.

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