

Stress-induced dislocations in silicon integrated circuits

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Many of the processes used in the fabrication of silicon integrated circuits lead to the development of stress in the silicon substrate. Given enough stress, the substrate will yield by generating dislocations. We examine the formation of stress-induced dislocations in integrated circuit structures. Examples are presented from bipolar and MOS-based integrated circuit structures that were created during developmental studies. The underlying causes of oxidation-induced stress and the effect on such stress of varying oxidation conditions are discussed. The knowledge thus gained is used to explain dislocation generation during the formation of a shallow-trench isolation structure. The importance of ion-implantation processes in nucleating dislocations is illustrated using structures formed by a deep-trench isolation process and a process used to form a trench capacitor in a DRAM cell. The effect of device layout geometry on dislocation generation is also examined. We show how TEM observations can be used to provide more information than

solely identifying those process conditions under which dislocations are generated. By combining TEM observations with stress analysis, we show how the sources of stress responsible for dislocation movement can be identified.

1. Introduction

Given enough stress, a silicon substrate will yield by generating dislocations. Although it would certainly be preferable for this not to occur during the fabrication of silicon integrated circuits (ICs), its occurrence appears to be an unavoidable by-product of the processes used to fabricate such circuits; dislocations often appear at some point during the development of a fabrication sequence. Once present in the silicon substrate, dislocations can lead to charge leakage and electrical shorting between elements—effects that can seriously degrade or prevent device operation [1, 2].

There are many sources of stress that arise during IC fabrication processes. Some important examples are the imbedding of materials with thermal expansion coefficients different from that of silicon, deposition of films with intrinsic stress, and oxidation of nonplanar surfaces. A

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recent paper by Hu [3] gives an excellent overview of these and other stress-related problems. In the present paper, we present examples of stress-induced dislocations that occur during the fabrication of advanced bipolar and MOS-based integrated circuits. This is a timely subject because of the growing importance of stress-induced defects in evolving IC processes.

For each succeeding generation of integrated circuits, two major trends are evident: The packing density of circuits on a chip increases, and device dimensions are reduced. Increasing packing density permits a greater level of integration per chip; reducing critical device dimensions leads to improved device performance for both MOS and bipolar structures. Unfortunately, the two trends lead to processes in which stress levels increase.

Higher packing densities are achieved by developing devices that occupy smaller areas of the silicon substrate and by packing the devices closer together. However, such scaling is subject to the constraint that devices must be electrically isolated from one another by isolation regions. In general, the reduction of the area required for isolation has been found to result in larger substrate stresses. In addition, as the area occupied by an active device continues to shrink, more of the device in each isolated cell is in proximity to the edges of its isolation regions, and some of the largest stresses develop at these locations. Scaling of device dimensions may lead indirectly to increased substrate stress. To maintain critical device dimensions (e.g., the channel length of a MOSFET or the base width of a bipolar transistor), control of dopant diffusion is essential. A large degree of such control is accomplished by minimizing the temperatures of thermal processing. But for oxidation processes, lowering the temperature of oxidation leads to higher stress levels in the substrate [4-6]. The fundamental reason for this is that an oxide growing on a nonplanar silicon surface must constantly deform, and oxides become more resistant to strain as temperatures are lowered. As an oxide thus becomes more rigid, a greater amount of the stress that develops during oxidation is accommodated by the development of strain in the substrate. Given the pervasive use of oxidation steps in IC fabrication, oxidation-induced stress is likely to become an increasingly important concern in the continuing drive toward lower-temperature processing.

Since stress is responsible for the unwanted appearance of dislocations, a question that naturally arises is how much stress a silicon wafer can tolerate before dislocations are generated. There is no simple answer to this question. A variety of studies indicate that stress levels of the order of 10^7 dynes/cm² or higher should be considered significant. In practice, however, the strengths of silicon wafers vary depending on a number of factors—in particular, the oxygen content and thermal history of the

wafer [7-9]. Also, the generation of stress-induced dislocations is a two-step process. Dislocations must first be nucleated and must then grow or move into regions where they affect devices. The stress necessary to nucleate dislocations depends greatly on the particular process of nucleation. Nuclei may be found in the as-grown wafer [7-9] or may be introduced into the wafer during processing. Two common process steps that assist the nucleation of dislocations are oxidation and ion implantation. Oxidation generates silicon self-interstitials, which can coalesce preferentially in strained silicon [1]. Vanhellemont et al. [10, 11] have discussed in detail the homogeneous nucleation of dislocations by condensation of self-interstitials. Ion implantation disrupts the crystalline structure of the silicon lattice and creates an excess of point defects. Although the details of the nucleation process following ion implantation are not thoroughly understood, it is well established that implantation damage can lead to the nucleation of dislocations. The effect of implantation on dislocation generation in stressed material can be quite dramatic; we demonstrate this with examples from bipolar and DRAM technologies (Sections 4 and 5). Once nucleated, dislocations can move great distances under an applied shear stress, by the process of glide. (The level of stress necessary to move dislocations depends, as in the case of nucleation, on oxygen content and thermal history [12].) Thus, dislocations initially created in a locally stressed area can propagate to other parts of a device cell (Sections 3 through 5).

The examples presented in this paper are taken from structures used in developing IC processes. During the developmental stage, process conditions are often varied to extreme cases, yielding important information regarding relevant process windows and information regarding process extendability: for example, extendability by placing devices closer together (vs. changing the layout design or isolation scheme) or by lowering processing temperatures and thereby minimizing dopant diffusion. We have chosen examples gathered from process experiments performed as part of a few different chip development efforts at several IBM laboratories. The examples illustrate the underlying causes of stress, how they cause dislocation generation, and how solutions to defect generation can be found.

In Section 2 we examine the underlying causes for the development of stress in oxide layers on silicon substrates and relate its development to oxidation parameters (temperature, pressure, ambience). In Section 3 we present an example illustrating the increased susceptibility of a process to defect generation as oxidation temperatures are lowered. The example explores dislocation generation resulting from a shallow-trench isolation process compatible with the requirements of a 16Mb DRAM technology. In addition to the temperature of oxidation, the importance of cell layout geometry is shown to be a

key factor in determining the onset of defect generation. The very important process of defect nucleation by ion implantation is discussed in Section 4, where we examine the effects of implantation on a deep-trench isolation process used in a bipolar technology. Damage created by ion implantation can develop into dislocations that glide large distances in stressed material. Substrates that otherwise show no signs of defects can become heavily dislocated after ion implantation. The geometry of cell layout again plays a key role in affecting this behavior. Finally, in Section 5 we present a detailed stress analysis for dislocation generation and propagation in a 4Mb DRAM process.

2. Oxidation-induced stress

Oxidation can introduce stress into silicon substrates in two different ways. The first is associated with the volume expansion of SiO_2 from silicon. A given volume of silicon will produce about 2.2 times as large a volume of SiO_2 . If the oxide is not free to expand, it pushes on whatever material is constraining its growth. This occurs frequently during IC fabrication, for example, during oxidation along the sidewalls of polysilicon-filled trench structures or at the edges of regions masked with Si_3N_4 . A second cause of stress is the strain that oxide layers experience when oxidation is performed on nonplanar structures. As a nonplanar silicon surface is oxidized, the oxide layer is constantly forced to stretch or contract as it grows out of the silicon surface.

How much stress is translated from an oxide layer into the substrate is determined by how easily the oxide deforms as it grows. In the following discussion, we consider the deformation of an oxide layer growing on a nonplanar substrate. The parameters that determine the ability of an oxide layer to deform in response to stress are examined, with particular attention focused on the effect of oxidation conditions on oxide stress.

• Development of stress in SiO_2

Upon oxidation, the growth of oxide at the Si/SiO_2 interface pushes the oxide above it away from the Si surface. On a convex-shaped surface, this causes the oxide to experience a tangential tensile stress; on a concave-shaped surface, compressive stress results. We are primarily interested in how stress develops in the silicon substrate during an oxidation step. This requires foremost an understanding of how an SiO_2 film deforms in response to the stresses that arise during its growth. Our knowledge of such stress-induced deformation processes is not yet satisfactory, and the subject remains an active area of research. However, in the past few years there has been a growing consensus that the best starting point for understanding nonplanar oxide growth is to view SiO_2 as a

nonlinear viscoelastic material [13, 14]. In recent papers, Rafferty, Borucki, and Dutton [13] and Hu [15] have provided an excellent illustration of the viscoelastic properties of SiO_2 . They considered the simple case of oxidizing a cylinder of silicon. The geometry of this problem lends itself to relatively simple analyses of stress induced in a growing oxide, yet the oxidizing cylinder example brings out most of the essential features of oxidation-induced stress on nonplanar surfaces. Hu has modeled oxide stress on a cylinder under a variety of process conditions. Rafferty et al. have modeled oxide stress under a more limited set of conditions than Hu, but with a more realistic viscoelastic model for SiO_2 . In the following treatment we use the oxide model of Rafferty et al. and reexamine the model predictions of Hu for a variety of process conditions. We also use the oxidizing cylinder as a vehicle to demonstrate how different model assumptions used in process modeling programs manifest themselves in predicting oxidation-induced stress.

Consider a cross section of a silicon cylinder having a thin surface oxide layer, the outer surface of the oxide located at a radial distance r_o . When the cylinder is oxidized, the newly formed oxide at the silicon surface will push out the original oxide layer. After a given oxidation time, the outermost layer of oxide moves from r_o to r , stretching out in the process. The stretching process requires a tangential strain of $\epsilon = (r - r_o)/r_o$. If the oxide grows at a rate $\dot{X}_{ox}$, it is a simple matter to show that $\dot{\epsilon} = (1 - \beta)\dot{X}_{ox}/r_o$, where $\beta = 0.44$ is the amount of silicon consumed for a given thickness of oxide grown. Therefore, the strain rate of the outermost oxide layer on the cylinder is given by

$$\dot{\epsilon} = \frac{(1 - \beta)}{r_o} \dot{X}_{ox}. \quad (1)$$

The question is how this strain is accomplished. If the oxide is highly resistant to deformation, large stresses develop in the oxide during the oxidation and, consequently, also in the underlying silicon. On the other hand, if the oxide can be stretched easily, little stress is developed during the oxidation. In general, stress is accommodated by a combination of elastic deformation and viscous flow. Following the treatment by Hu [15] and Rafferty et al. [13], we illustrate the viscoelastic deformation process by analogy to a spring and dashpot (i.e., damped piston) in series—a combination known as a Maxwell element (Figure 1).

Initially, the system is assumed to be in a state of zero stress. Stress is developed by applying a force that moves the end of the spring. The total strain in the system is $\epsilon = (A - A_o)/A_o$, where A_o is the original position of A . If the end of the spring moves at a speed v , the strain rate of the system is $\dot{\epsilon} = v/A_o$. The total strain is the sum of elastic

and viscous deformation processes, i.e., $\epsilon = \epsilon_{\text{elastic}} + \epsilon_{\text{viscous}}$. The elastic strain is given by

$$\epsilon_{\text{elastic}} = \frac{(A - B)}{A_0} = \frac{\sigma}{G}, \quad (2)$$

where G is the spring constant, which we identify with the elastic modulus of rigidity of the oxide. The stress-strain relation for viscous flow is expressed as

$$\dot{\epsilon}_{\text{viscous}} = \frac{\dot{B}}{A_0} = \frac{\sigma}{\eta}, \quad (3)$$

where η is the viscosity of the dashpot (i.e., the viscosity of the oxide). Equations (2) and (3) lead to the differential equation

$$\frac{\dot{\sigma}}{G} + \frac{\sigma}{\eta} = \dot{\epsilon}. \quad (4)$$

Equation (4) is a simple but useful expression for understanding many of the important factors that determine evolution of stress in oxides during growth. By using values for G and η corresponding to SiO_2 and using the expression for $\dot{\epsilon}$ in Equation (1), relative levels of stress generated with different oxidation conditions can be investigated for the oxidizing cylinder example [13, 15]. For example, one can calculate the relative stress levels in different thicknesses of an oxide film grown at a given temperature, or the relative stress levels in an oxide film of a given thickness grown at different temperatures.

In the simplest case, both the growth rate and viscosity are assumed constant. In this case, Equation (4) has the solution

$$\sigma = \eta \dot{\epsilon} (1 - e^{-Gt/\eta}). \quad (5)$$

This equation states that the oxide starts at zero stress and asymptotically approaches a value of $\eta \dot{\epsilon}$. Physically, this means that the oxide deforms elastically in the initial stages of growth; then, as the oxide continues to grow, its stress is relieved by viscous flow. In steady state, the stress in the oxide is directly proportional to the oxidation rate times the viscosity. Obviously, the less viscous the oxide, the smaller the saturation value of its stress. Oxide viscosity decreases with higher temperatures and increasing hydroxyl content (see the papers by Hu [15] and Stiffler [14] for a summary of data). Thus, performing oxidations at the highest acceptable temperature and in a wet rather than a dry oxygen ambience would seem to be preferable. However, oxidation rates increase with increasing temperature and are higher in a wet oxygen ambience than in a dry oxygen ambience. Faster oxide growth means that the strain rate is higher and viscous flow must increase to avoid stress buildup. Predictions regarding such trade-offs in processing conditions can be obtained by solving Equation (4). In that regard, Equation

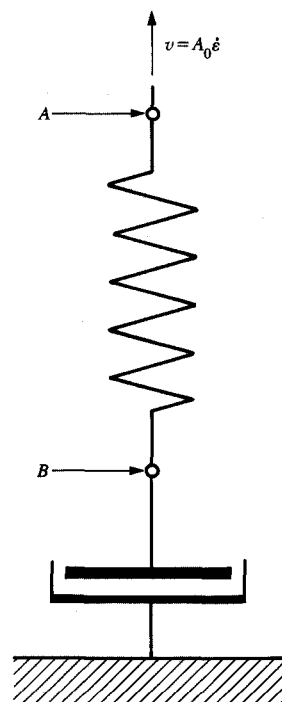
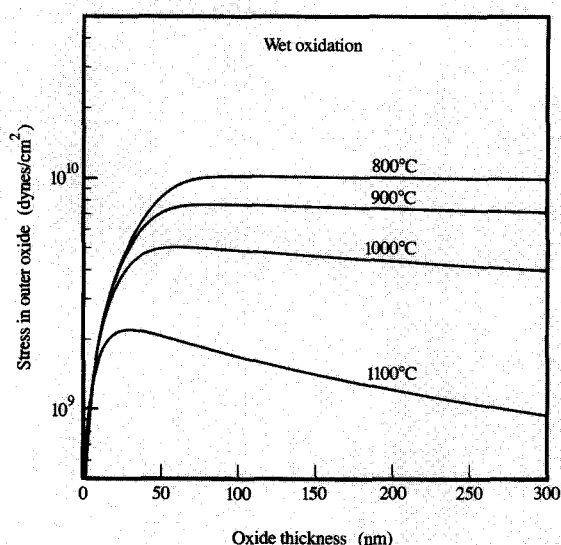


Figure 1

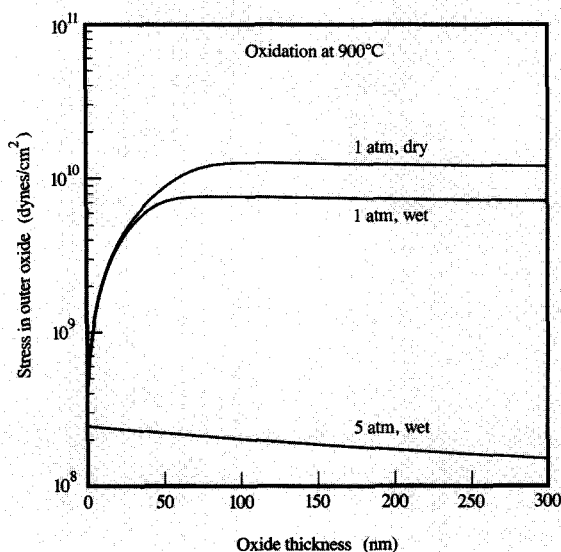
Viscoelastic model of oxide strain. Analogy is made to a spring and dashpot (i.e., damped piston) system.

(5) predicts that growing oxides at high temperatures in a wet oxygen ambience does indeed minimize stress levels, despite growth at relatively high rates. Hu [15] has shown that this same qualitative behavior occurs for the more general situation of linear-parabolic oxide growth. In addition, the analysis of Hu predicts that high-pressure steam oxidation should lead to further reductions in oxide stress from the levels of atmospheric oxidation—again, despite the increased oxidation rates at high pressure.

The above analysis applies under the assumption that oxide viscosity remains constant during growth. The viscosity of SiO_2 was considered a function of temperature and hydroxyl content only. However, it has been shown experimentally that the viscosities of glasses decrease under high stress [16–18]. Recent treatments [13, 14, 19, 20] of oxidation-induced stress have attempted to take account of this fact. Sutarjda and Oldham [19, 20], Rafferty et al. [13], and Stiffler [14] have favored the use of Eyring's model [21] to describe viscosity. In Eyring's model, the viscosity of the oxide decreases dramatically at



(a)



(b)

Figure 2

Calculated oxide stress as a function of oxide thickness at different conditions, for growth on a silicon cylinder, initially 1 μm in radius: (a) Stress in the outermost oxide layer for different oxidation temperatures. (b) Stress developed at 900°C for different ambient conditions.

high stresses. The high-stress behavior is described by the relation

$$\eta = \eta_0 \frac{(\sigma V_m / 2kT)}{\sinh(\sigma V_m / 2kT)}, \quad (6)$$

where η_0 is the zero-stress viscosity and V_m is a characteristic volume associated with the space cut out by a diffusing molecule during flow. Eyring [21] has analyzed the dependence of viscosity on stress from the viewpoint of absolute rate theory. However, the quantitative predictions of this atomistic approach do not agree well with experiment [16]. To obtain agreement with experiment, V_m has been viewed as a fitting factor. Donnadieu et al. [18] have empirically determined a value for V_m of approximately $180 \text{ \AA}^3$.

As an example of how oxide stress varies as a function of process variables, we show in Figure 2 calculations for stress in the outermost layer of oxide grown on a silicon cylinder 1 μm in radius. To produce these plots, we have solved Equation (4) using the expression for viscosity η given in Equation (6). We have used a value of $G = 3 \times 10^{11} \text{ dynes/cm}^2$ [22, 23] and viscosity values for η_0 from Stiffler [14], and have assumed oxidation rates for $\{100\}$ surfaces using the Deal-Grove formulation [24]

$$\frac{X_{\text{ox}}^2}{k_p} + \frac{X_{\text{ox}}}{k_e} = t, \quad (7)$$

where k_p and k_e are the parabolic and linear growth-rate constants. For wet oxidations, we have used values for k_p and k_e from Razouk et al. [25]; for dry oxidations, we have used values from Hess and Deal [26, 27].

In Figure 2(a) we show calculated stress values for varying thicknesses of oxide grown at different temperatures. This plot indicates that stress should decrease as the oxidation temperature is increased. This is primarily due to the decrease of viscosity with increasing temperature. Similar plots by Hu [15], using a stress-independent viscosity model, show a stronger temperature dependence on stress than that shown in Figure 2(a). A secondary effect involves the quicker transition at higher temperatures from linear growth rate ($\dot{X}_{\text{ox}} \propto t$) to parabolic growth rate ($\dot{X}_{\text{ox}} \propto t^{-1/2}$). In the viscous flow regime, stress is expected to decrease as the strain rate decreases [Equation (3)]. Therefore, as the oxidation rate decreases during parabolic growth, stress should also decrease. The effect of parabolic oxide growth is most pronounced for the 1100°C case in Figure 2(a), where more of the oxide growth takes place in the parabolic regime compared to the lower temperatures of oxidation. Similar plots by Rafferty et al. [13], using the same type of viscoelastic oxide model, do not show this behavior. For simplicity, Rafferty et al. ignored the parabolic growth regime in their treatment and assumed oxidation rates to be constant with time.

Including full linear-parabolic growth-rate behavior for the oxide, Figure 2(a) shows that for a given temperature there should be a maximum value in the amount of stress in the oxide. Once the oxide growth has moved from the elastic to viscous regimes, no further increase in stress is

expected. As long as the maximum stress level is not enough to generate dislocations in the bulk, it should be possible to grow any thickness of oxide without defect generation. The prediction that the growth of the thicker oxide does not necessarily lead to more substrate stress is not at all intuitive, and demonstrates the value of the viscoelastic analysis. Conversely, the viscoelastic analysis indicates that growing relatively thin oxides is no guarantee that high levels of stress will not be generated. Supportive experimental results for the above predictions are presented in Section 3.

In Figure 2(b) we show the calculated effects of oxidant ambience on stress. To take account of changes in pressure, we have scaled k_e and k_p linearly with pressure [24, 25]. Reductions in stress going from dry to wet oxidations and from atmospheric to high-pressure wet oxidations are caused by corresponding decreases in viscosities. The predicted stress reduction for high-pressure wet oxidation compared to atmospheric conditions is dramatic. Note also that in the 5-atm oxidation case there is no large elastic contribution to stress; i.e., there is no initial increase of stress with oxide thickness [Equation (2)] for thin oxides as there is for the 1-atm dry and wet cases. This is because the oxide viscosity at 5 atm is already low enough that oxide flows viscously during the entire time of oxidation. While Figure 2(b) implies a beneficial effect of reducing viscosity, it should be kept in mind that the large decreases in oxide stress with high-pressure wet oxidation are at present only predictions. Hu [15] has made this prediction by using available data for the dependence of oxide viscosity on hydroxyl concentration at one atmosphere, and extrapolating to the case of higher atmospheres. However, we have found that such predictions based on extrapolation are very sensitive to data fitting of the data obtained at one atmosphere. We mention in the following discussion some preliminary data indicating that high-pressure wet oxidation may not lead to significant reductions in oxide stress.

We have also calculated the effect of reducing the partial pressure of oxidant. Consider the effect of reducing the partial pressure of oxygen in a dry-oxidation process. The viscosity of the oxide is unchanged, but the oxidation rate is reduced. Therefore, stress levels should be reduced. For the case of dry oxidation at 0.1 atm, the curve for stress as a function of oxide thickness practically coincides with the 1-atm wet-oxidation curve in Figure 2(b); we have not plotted the 0.1-atm case because of this close agreement. The stress can be reduced simply by diluting oxygen with an inert carrier gas. The penalty for this is that it increases the time needed to grow the same amount of oxide, and the extra time might be in excess of the allowable thermal budget. Reducing the partial pressure of oxidant in a wet-oxidation process leads to different results. If we dilute a

wet-oxidation ambience, the growth rate of the oxide film will go down, but so will the viscosity of the oxide. For the case of 0.1-atm wet oxidation, the curve of stress as a function of oxide thickness practically coincides with the curve of 1-atm dry oxidation in Figure 2(b); reducing the pressure leads to higher stress levels. From these last two examples we can immediately see that the worst possible situation is a high-pressure dry-oxidation ambience. For dry oxidation, increasing the pressure increases the oxidation rate without reducing the oxide viscosity, resulting in a greater oxide stress with increasing pressure.

• Quantitative modeling of stress in Si

The preceding discussion summarizes the basic factors that determine the buildup of stress in SiO_2 during oxidation. We are primarily interested in modeling stress distributions in the silicon substrate for oxidation of arbitrarily shaped structures. Modeling this class of problems is considerably more involved than simply solving Equation (4). In principle, computer simulation using appropriate process models can be used to calculate stress distributions for any realistic situation. In this paper, we rely primarily on simple analytic approximations to evaluate stress; the examples of stress generation we have chosen lend themselves to such treatments and are easier to understand than results from rigorous process simulation. Here, we include a brief review of the process-simulation approach. Understanding the requirements of associated oxidation models gives further insight into the physical processes that govern oxidation and the development of stress. We also summarize the status of oxidation models and their utility in modeling oxidation-induced stress.

Process-simulation programs differ from one another primarily in the numerical methods of solution employed and the specifics of the oxidation models; algorithms for simulating oxidation are roughly the same. The flow chart in Figure 3 shows the algorithm used in our process simulation program FEDSS (Finite Element Diffusion Simulation System) [28]. During one time period, oxygen diffusion through the SiO_2 is simulated. This determines the flux of oxygen to the silicon surface, which in turn determines the local oxidation rate according to the Deal-Grove formulation of oxide growth [24]. The strain rate is calculated for each element of the oxide using a purely viscous flow model (examined further in the following discussion). Si_3N_4 is also treated as a viscous material—a model supported by the recent work of Griffin and Rafferty [29]. The stress and strain at the Si/SiO_2 interface is then treated as a boundary-value problem, and the yield in the silicon is determined using elastoplastic models. The process is then repeated for the next time period.

One drawback of most process-modeling programs is that they do not simulate oxidation in three dimensions.

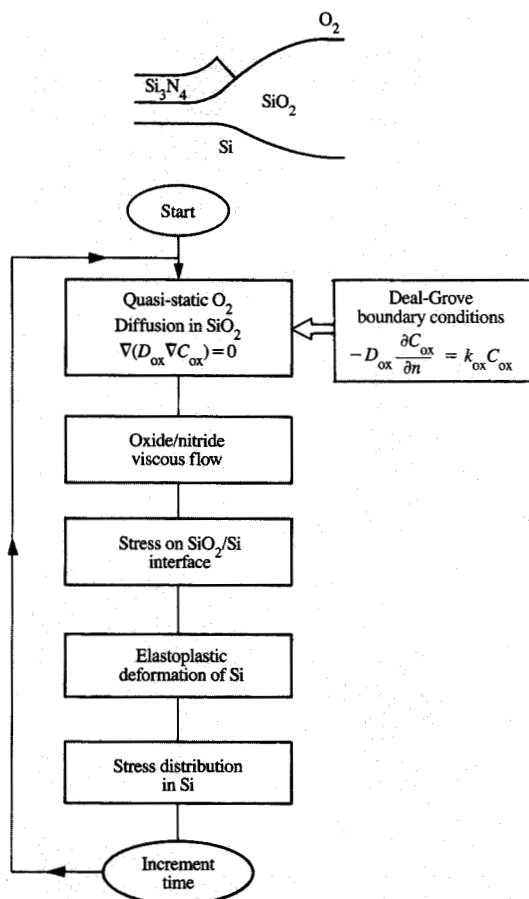


Figure 3

Flow chart for process-simulation algorithm used in FEDSS [28] program. D_{ox} and C_{ox} are the oxidant diffusivity and concentration, respectively, and k_{ox} is the surface reaction rate defined by Deal and Grove [24].

(Umimoto and Odanaka [30] have recently presented results of such simulations.) The validity of simulation results then depends on the applicability of the plane analysis approximation to a given two-dimensional cut. We explicitly point out the three-dimensional nature of stress problems several times in this paper. Development of three-dimensional versions of current process modeling programs is a difficult but not unsolvable problem. More impetus to develop appropriate programs will undoubtedly come from the growing necessity of performing three-dimensional analyses on IC structures and the smaller computational overhead afforded by increased computer power.

For two- or three-dimensional oxidation simulations, correct modeling of stress in the oxide is a critically important requirement because of its effects on oxidation process. The effects of oxide stress on oxidation rates have been observed experimentally in a number of studies. Marcus and Sheng [31] first showed oxide growth to be retarded on both convex- and concave-shaped surfaces. Even in the absence of dislocations, such oxide-thinning effects on nonplanar surfaces are known to be reliability concerns because of the high electric fields they produce at corners [32, 33]. Oxide growth on a variety of shapes (including cylinders) was studied by Kao et al. [34–36]. Sheng and Marcus [37] have shown oxidation to be retarded in areas close to the edges of oxide-isolated regions.

These observations of retarded oxidation rates are believed to arise predominantly from stress effects. The degree of retarded oxidation rates on convex and concave corners for different process conditions is consistent with this view. For example, Yamabe and Imai [33] have shown that oxidation on the corners of trenches is retarded less for growth at high temperatures than at low temperatures, less for wet-oxidation conditions than dry-oxidation conditions, and less for diluted dry-oxidation conditions than atmospheric dry-oxidation conditions. As expected, the conditions that lead to highest oxide stress result in the greatest amount of oxide thinning at corners. Recent results from Imai and Yamabe [38] show oxide-thinning effects at corners to be greatly mitigated by the addition of small amounts (hundreds of ppm) of NF_3 to dry O_2 , even though the oxidation rate is increased by the addition of NF_3 . These results strongly imply that the NF_3 is somehow effective in reducing the viscosity of the oxide. This contention is supported by the experiments of Kouvatso et al. [39], which show for planar growth under dry-oxidation conditions that stress is reduced by the addition of NF_3 . However, there is still some question about the relevance of intrinsic stress during planar oxide growth to that generated during the oxidation of nonplanar surfaces.

From current experimental results, it appears that the degree of oxide thinning during corner oxidation corresponds to the amount of stress developed in the oxide. We have recently performed corner oxidation experiments to investigate the effect of high-pressure steam oxidation on oxide stress. We find that wet oxidation at 800°C and 10 atm leads to greater retardation of oxidation rates around corners than does atmospheric wet oxidation—contrary to the predictions of Hu's model [15]. Our results suggest that whatever reduction in oxide viscosity occurs under high-pressure conditions, it is not enough to offset the increasing stress that results from oxidizing at a faster rate (at least for our specific conditions).

Stress effects have also been suggested as a source of field-oxide thinning. Mizuno et al. [40] first observed that

the oxidation rate of a field oxide is retarded in a LOCOS (LOCAl Oxidation of Silicon) process when the width of the oxidizing window is smaller than about 1 μm . They attributed this effect to a diffusion-limited supply of oxidant to the surface, which results from the two-dimensional nature of the oxidation process. This effect has recently been studied by Lutze et al. [41] using a poly-buffered LOCOS process. The authors concluded that stress effects cause retarded oxidation rates in their experiments, and also in the experiments of Mizuno et al.

To model oxidation in two or three dimensions, it is necessary to understand how stress in the oxide affects oxidation rates. Referring to the flow chart of Figure 3, one can see that oxidation will be affected if stress has an effect on oxidant diffusion or the surface reaction rate. Stress may also have an effect on the solubility of oxidant in the SiO_2 , which will in turn affect the oxidation rate. A comprehensive review on this subject has been given by Rafferty [42]. His conclusions are the following: 1) oxidant diffusion is reduced under compressive stress, and unaffected under tensile stress; 2) the surface reaction rate is retarded by compressive stress normal to the surface (as first proposed by Kao et al. [34]); 3) there are not enough data to quantify the effects of stress on oxidant solubility, and some results qualitatively explained by changes in oxidant diffusivity may reflect changes in both the oxidant solubility and diffusivity.

Until recently, process simulation programs followed the ground-breaking work of Chin et al. [43–45] and assumed a model of viscous rather than viscoelastic flow for the SiO_2 ; i.e., the oxide is treated as an incompressible fluid. In the analogy to a spring and dashpot system (Figure 1), this is equivalent to assuming that the spring is perfectly rigid [$G \rightarrow \infty$ in Equation (4)]. If the elastic component of strain cannot be neglected, such a model will obviously overestimate the stress buildup in an oxide because it does not allow for any stress relief by elastic deformation. The problem is compounded by not allowing for any reduction in viscosity at high stress levels, i.e., assuming a linear rather than nonlinear viscous model.

Assuming that the viscosity η in Equation (4) is stress-dependent introduces nonlinear behavior into the viscoelastic treatment. In contrast to a constant-viscosity model, the stress dependence does not affect the qualitative relationships between process conditions and stress levels, but it does have a profound effect on quantitative results. Some illustrative examples are given in Figure 4, which shows the separate contributions of stress-dependent viscosities and elastic components of strain. For a viscous (vs. viscoelastic) model, the elastic component of strain is ignored completely. For a linear (vs. nonlinear) model, viscosity is assumed to be independent of stress. Figure 4(a) shows a comparison of predictions for wet oxidation at 800°C. For the linear

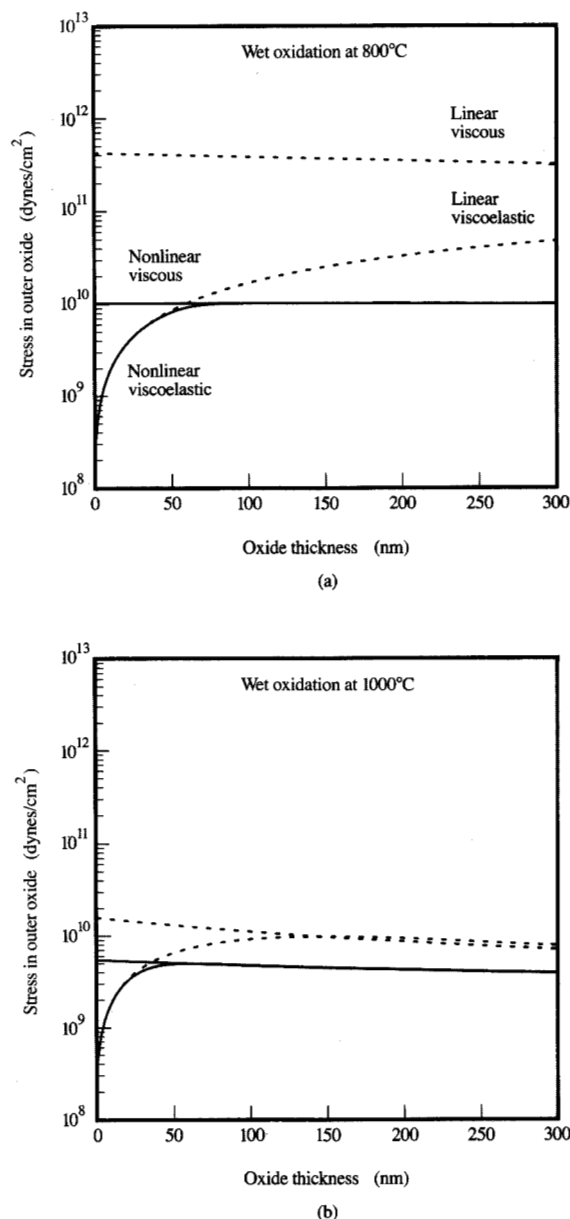


Figure 4

Comparison of predictions based on oxide deformation models. A 1- μm cylinder of silicon is assumed to be oxidized as in Figure 2. For viscoelastic models, use is made of Equation (4), while for viscous models, G is set to infinity. For nonlinear models, use is made of the stress-dependent viscosity of Equation (6) when solving Equation (4), while for linear models, a constant viscosity η_0 is assumed to apply.

viscous model, Equation (4) with G set to infinity gives $\sigma = \eta_0 \dot{\epsilon}$, where $\dot{\epsilon}$ can be expressed as a function of oxide

thickness using Equations (1) and (7),

$$\dot{\epsilon} = \frac{1 - \beta}{2r_o} \frac{k_p}{(k_p/2k_e + X_{ox})} \quad (8)$$

Including the stress dependence of viscosity from Equation (6) in the nonlinear viscous model leads to $\sigma = (2kT/V_m) \sinh^{-1} (\eta_0 \dot{\epsilon} V_m / 2kT)$. As shown in Figure 4(a), the nonlinear viscous model predicts substantially less stress (about a factor of 40) than the linear viscous model. When the elastic contribution to strain is included, the stress is first expected to grow with increasing oxide thickness and asymptotically approach the viscous solutions. The linear viscoelastic solution does not merge with the linear viscous model after 300 nm of oxide growth, while the nonlinear viscoelastic solution matches the nonlinear viscous solution after only 80 nm of oxide growth. Because the oxide becomes less viscous as stress increases, the predicted behavior for the nonlinear viscous model approaches the viscous flow regime more quickly than that of the linear viscoelastic model. Figure 4(b) shows predictions for wet oxidation at 1000°C. Qualitatively, the results are the same as for Figure 4(a), but the agreement between models is much closer at 1000°C. The agreement is better because of the lower assumed oxide viscosity. For a given oxide thickness, the less viscous the oxide, the less stress is built up. The effect of including a stress-dependent viscosity is thus minimized, and the predictions of the nonlinear and linear viscous models approach each other. As an oxide becomes less viscous, the elastic contribution becomes less important, and the predictions of the nonlinear viscoelastic and nonlinear viscous models tend to coincide except for the beginning of the oxidation process. At 1100°C, where the oxide viscosity is reduced further, the differences in the predictions are barely distinguishable. For the 5-atm 900°C oxidation shown in Figure 1(b), the oxide viscosity is low enough to lead to the same stress predictions for each of the models.

Fundamentally, the choice of oxide deformation model is unimportant if not much stress is built up in the oxide. However, in situations where stresses are large enough to affect the oxidation rate, the choice of deformation model becomes crucial. Although the assumption of an incompressible fluid is a simplification, greater inaccuracies result from the assumption of a stress-independent viscosity. Indeed, the agreement between an incompressible fluid model and a viscoelastic model is far better when a stress-dependent viscosity is used. Stress-dependent viscosity models are being added to the FEDSS program, and are already incorporated in current versions of the popular SUPREM 4 program from Stanford [42, 46], the Berkeley CREEP program [20], and the IBM NOVEL (NOnlinear ViscoELastic) [47] program.

Fortunately, the emerging need to simulate oxidation-induced stress coincides favorably with current developments in oxidation models. The original goal of developing oxidation models was to accurately predict oxide shapes grown on nonplanar structures. This work has led to the identification of stress as a major factor in determining oxide shapes. Because of this, the development of better oxidation models will also result in better stress modeling.

Compared to older oxidation models, current model predictions lead to much more optimistic projections for limiting oxidation-induced stresses at low temperatures. In the temperature range toward which IC processing is evolving, 800–900°C, the newer stress-dependent viscosity model sometimes predicts orders of magnitude less stress than a constant-viscosity model. If the constant-viscosity model were correct, there are many instances in which gross defect generation in silicon substrates or cracking of oxides should result. The absence of these phenomena in such cases is evidence that the presence of stress has reduced the viscosity, thus allowing the oxide to relieve its stress by flow rather than dislocation generation in the substrate. In Section 3 we present an example of a defect-free isolation structure produced using oxidation at temperatures as low as 850°C. Using stress-independent viscosity values for SiO₂, we would predict that it is not possible to perform the oxide isolation step at such a low temperature without generating dislocations in the silicon substrate. The presentation in Section 3 also illustrates the effect of process conditions on the generation of defects using most of the concepts discussed in this section.

3. Shallow-trench isolation

As a first example of stress-induced defects, we examine the generation of dislocations in an advanced isolation process known as shallow-trench isolation (STI) [48]. Traditionally, increased integrated circuit density has been accomplished with simple photolithographic scaling; however, advanced lithography techniques have exposed several materials-related limitations. One of these is the resistance to scaling of traditional recessed-oxide or semirecessed-oxide isolation. As a result of lateral oxidation and viscoelastic deformation in the oxide, substantial “bird’s beaking” generally accompanies these processes and results in isolation features that are substantially larger than photolithographically defined images. To minimize these effects, the pad structure has been altered in several ways [49]. However, while the amount of bias on the isolation image can be reduced using these techniques, it is not eliminated. In general, for a given isolation scheme, process changes that have reduced bird’s beaking have also led to an enhanced susceptibility to process-induced dislocation generation.

An alternative isolation technology, shallow-trench isolation, has been developed [48, 50], which attempts to introduce much less lateral bias than traditional recessed-oxidation techniques. In this process, the isolation images are defined photolithographically, and relatively shallow trenches ($\sim 0.5 \mu\text{m}$) are etched into the substrate by reactive ion etching (RIE). A thin thermal oxide is then grown to remove the RIE damage and electrically passivate the trench surfaces. Next, a thick layer of SiO_2 is deposited by chemical vapor deposition, completely filling the trenches. The structure is subsequently planarized, yielding the structure shown in **Figure 5**. Following planarization, the structures are annealed at a relatively high temperature to reduce the wet-chemical etch rates of the deposited oxide to values comparable to those of thermal oxide. Since RIE is capable of producing nearly vertical sidewalls, the image bias is nearly zero, and the isolation process is truly scalable. While the STI process is scalable, and hence advantageous from an extendibility viewpoint, trench structures have also been shown to be susceptible to process-induced dislocation generation [51–53].

After planarization the STI structure introduces only moderate levels of stress into the silicon substrate. Due to the viscoelastic behavior of the oxide trench-fill material, the structure is expected to be essentially stress-free at the postplanarization annealing temperature. As the structures are cooled, stress is generated in the substrate because of the thermal expansion mismatch between the SiO_2 and Si. Experience has shown that stresses generated solely by differential thermal contraction are not a primary concern for STI. However, during thermal oxidation steps following STI planarization, which are generally required for device fabrication, substantial stresses can be generated at elevated temperatures. This process can easily be envisioned for the cross section of **Figure 5**. While the substrate surface oxidizes, oxidation also occurs along the silicon surface defining the trench, with the oxidation rate most rapid close to the substrate surface. Since a substantial volume expansion accompanies the thermal oxidation of silicon, oxidation of the trench sidewalls is analogous to driving a wedge into the trench, overfilling it and creating stress in the adjacent silicon. The exact nature of the stress generated by this “wedge” is, in part, determined by the temperature-dependent oxidation kinetics. Because of the difference in the coefficients of thermal expansion of Si and SiO_2 , stresses present at the oxidation temperature are further increased during cooling.

The effects of oxidation on defect generation have been studied for two different STI patterns; these patterns are shown in **Figure 6** [53]. In the following discussion, the patterns of parts (a) and (b) are referred to as pattern types A and B, respectively. These isolation patterns are both suitable for a 16Mb DRAM process. (The particular cell

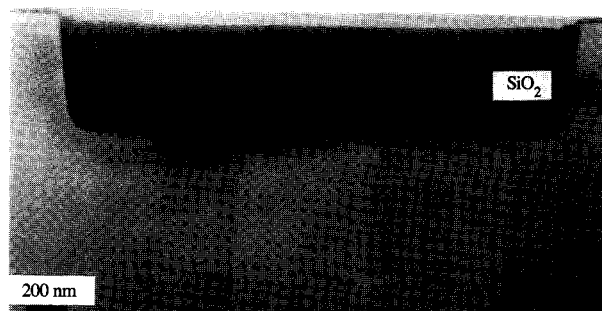


Figure 5

A transmission electron micrograph cross section of a shallow isolation trench, following planarization. From [53], reproduced with permission. (© 1990 IEEE.)

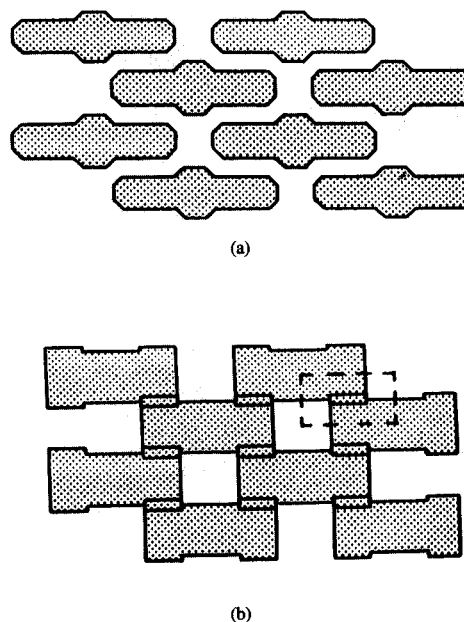


Figure 6

Two types of STI patterns. Patterns in (a) and (b) are referred to in the text as type A and type B patterns, respectively. The shallow-trench regions are unshaded, and the DRAM cell region is shown as the dashed box in (b).

design utilizes a merged isolation and (storage) node trench (MINT); details of the process can be found in [54].) Both these patterns take up the same amount of area. When practiced in $0.7\text{-}\mu\text{m}$ ground rules, the cell area is approximately $7 \mu\text{m}^2$; it is indicated as the region enclosed by the dashed box in **Figure 6(b)**. Layout patterns A and B

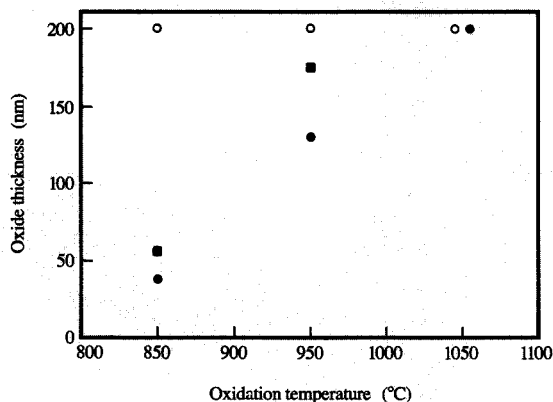


Figure 7

Effect of pattern type on defect formation for various oxidation temperatures. The open circles correspond to data from pattern B; the solid circles and squares correspond to data from pattern A. Both sets of circles indicate that no defects were observed, while the squares indicate that multiple defects were observed in all cells. From [53], reproduced with permission. (© 1990 IEEE.)

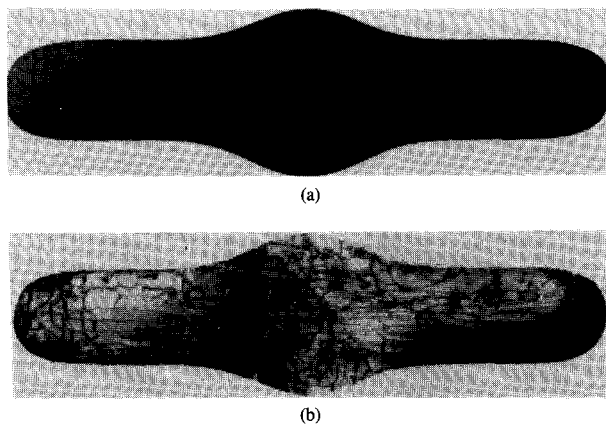


Figure 8

Bright-field, plan-view transmission electron micrograph of silicon mesa [pattern type A in Figure 6(a)]. Samples were oxidized at 850°C. (a) No dislocations were present after forming of 38 nm of oxide. (b) Increasing the oxidation time to grow 56 nm of oxide resulted in multiple dislocations throughout the mesa. From [53], reproduced with permission. (© 1990 IEEE.)

were generated in order to investigate different methods of isolating devices from each other and connecting transfer devices to their storage capacitors. An investigation was also made of the relative susceptibilities of patterns A and B to defect generation.

To determine the susceptibility of the STI structures to defect generation, a matrix of oxidation steps was performed and defects observed by TEM analysis. Samples were oxidized at 850, 950, or 1050°C in a wet O_2 ambience to grow the different amounts of oxides required for device fabrication. This approach allowed direct comparison of defect structures in the two cell types within the same chip, thereby eliminating potential across-wafer and wafer-to-wafer differences. Plan-view TEM was used to observe defect structures in these arrays; several hundred cells from each experimental group were examined.

Susceptibility to defect generation was determined in the following way. At a given temperature, samples were oxidized for different times to form oxides up to 200 nm in thickness. Oxidations exceeding 200 nm were not performed because thicker oxides are not required by advanced DRAM processes. Plan-view TEM analysis was then used to determine the point at which stress from the oxidation process resulted in defect generation in the silicon substrate. In most cases, glissile dislocations were the only defects found to be present; however, for the lowest oxidation temperature studied (850°C), stacking faults were sometimes observed.

Figure 7 summarizes the results of the study. For patterns of type B, oxides of 200 nm or less could be grown at all temperatures without the generation of defects. Type A patterns were much more susceptible to dislocation generation. Only at a temperature of 1050°C could 200 nm of oxide be grown without defects; at 850°C, only about 30 nm of oxide could be grown before defects appeared in all cells. To verify that the stress was generated from oxidation of the trench sidewalls, an oxidation barrier (Si_3N_4) was inserted into the trenches following the trench-sidewall passivation oxidation (and prior to filling the trenches with deposited oxide). This minor process modification allowed considerably more oxidation before crystalline defects were generated, confirming the suspected mechanism. The dramatic nature of dislocation generation is demonstrated in **Figure 8** for the oxidation of pattern A at 850°C. These micrographs correspond to the lower left data points in **Figure 7** and show the severe microstructural degradation that can accompany a modest increase in oxide thickness.

From the summary of results, it is clear that both the shape of the trench and the temperature of oxidation are critical factors in the development of defect-free isolation structures. Consistent with the discussion in the previous section, the stress buildup becomes of increasing concern as the temperature of oxidation is decreased. In the previous section, this trend was explained largely in terms of the viscoelastic properties of the oxide: Viscosity increases with decreasing temperature, and the accompanying reduction of stress-relieving viscous flow

creates more stress for the same amount of oxide grown. Another important factor is the effect of crystallographic orientation on oxidation rates. Oxidation rates on surfaces of different crystallographic orientation are known to increase in the order $\{111\} > \{110\} > \{100\}$. The surfaces of the wafers used were along $\{100\}$ planes, while the trench sidewalls were along $\{110\}$ planes. Differences in oxidation rates on these two surfaces were observed by oxidizing unfilled trenches. To grow a 200-nm-thick oxide, the average oxidation rate on the $\{110\}$ surface was found to be about 17% higher than the rate on the $\{100\}$ surface at 1050°C, and 39% higher at 850°C. Therefore, one should expect more sidewall oxidation at lower temperatures for the same amount of oxide grown on the wafer surface, and hence the generation of more stress. These two factors—orientation-dependent oxidation rates of the silicon and viscoelastic properties of the oxide—both play a role in determining the temperature-dependent resistance of a specific isolation pattern to oxidation-induced defect generation.

Further insight into the observed pattern dependence can be obtained by considering a simpler problem: the evolution of stress in one dimension created by oxidizing oxide-filled trenches. Stiffler [14] has approached this by considering a cross section of an STI pattern such as that shown in Figure 5. The geometry of the configuration was defined in terms of the width of the trench W_t and the width of the silicon mesa W_m . The amount of strain in the silicon mesa was estimated at the surface (where it is the greatest) for different amounts of oxides grown along the sidewalls. A spring-and-dashpot analogy is illustrated in Figure 9. The insertion of the wedge in Figure 9 represents the process of oxidation along the sidewall. As oxidation proceeds, both the oxide trench and silicon mesa are strained in order to accommodate the growing oxide layer. The treatment in [9] of viscous flow in the oxide is similar to that presented in Section 2: The SiO_2 is treated as a nonlinear viscoelastic material with a stress-dependent viscosity given by Eyring's relation in Equation (6). The remainder of the analysis is not presented here, and the reader is referred to [14] for more details.

One of the main results of [14] is that stress (or strain) first increases linearly with the amount of oxide grown, and then, above a certain oxide thickness (determined primarily by the oxidation temperature and the geometry of the structure), saturates. This stress behavior is qualitatively the same as that shown for the oxidizing cylinder example in Figure 2(a) and has the same underlying explanation as that presented in Section 2. If the geometry and oxidation conditions are chosen such that the stress saturation level remains below the critical stress for dislocation generation, relatively thick oxides can be grown without introducing damage in the silicon. This appears to be the condition of pattern B for the data

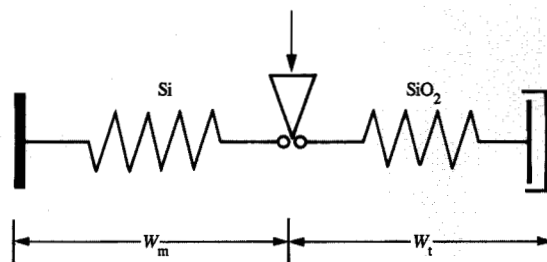


Figure 9

Spring-and-dashpot model of STI process. An oxide-filled trench of width W_t is oxidized next to a silicon mesa of width W_m . Oxidation along the trench sidewall generates stress in a manner analogous to driving a wedge between the two springs.

in Figure 7. If, on the other hand, stress saturation levels can exceed the critical stress for dislocation generation, only oxides below a certain thickness at a given temperature can be grown without introducing defects; this appears to be the case of pattern A for the data in Figure 7.

As discussed in Section 2, saturation of the stress level occurs when the oxide goes beyond its elastic strain limit and further stress relief becomes dominated by viscous flow. Moreover, if the viscosity of the oxide were assumed to be independent of stress (i.e., if low-stress values were assumed for the oxide viscosity), the model would predict that defect-free STI could not be achieved with the low-temperature oxidations used in these experiments. Our results indicate that the reduction of oxide viscosity at high stress levels is an essential feature for models of oxidation-induced stress.

The analysis of [14] provides more details on how the geometry of STI structures (i.e., the dimensions of both W_t and W_m) plays a major role in determining the levels of stress generated during oxidation. The relative dimensions of the trench and active region, W_t/W_m , also play a role in determining stress levels. As intuitively expected, for the same value of W_t/W_m and degree of oxidation, higher levels of stress are generated in finer structures. Analyzing various cross sections of patterns A and B (Figure 6) has shown that the higher susceptibility of pattern A to stress buildup can be explained in terms of the geometry effects predicted by the simple STI model. It is encouraging that such complex processes can be attacked so effectively with simple models based on sound physical reasoning. Still, limitations of the model should also be recognized.

An essential feature of the simple STI model is that it is based on plane-strain analysis. The limitations of this

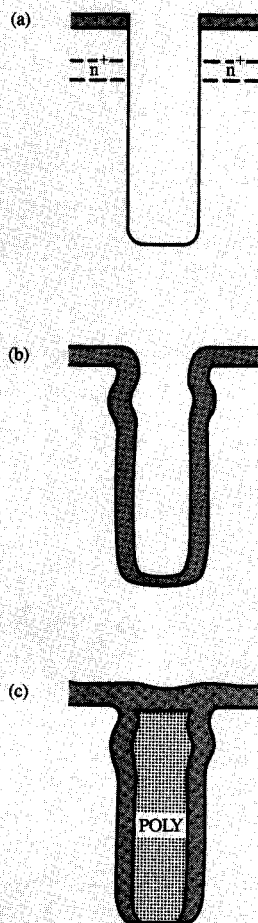


Figure 10

Deep-trench fabrication sequence: (a) Trench is formed by RIE, followed by (b) oxidation, and (c) removal of oxide at bottom of trench, filling with polysilicon, and planarizing.

approach can be appreciated by examining the patterns in Figure 6. Any vertical or horizontal cut along the patterns defines a cross section for analysis. The validity of a plane-strain analysis hinges on the assumption that cross sections of adjacent parallel planes are identical to the plane being examined. Plane analysis is obviously invalid near corners and curved surfaces in the patterns of Figure 6. This is a significant shortcoming of such modeling, since large stresses can develop at corners (an issue we discuss in the following section). Another important shortcoming is that the oxidation rate along the sidewalls is assumed to be the same as the oxidation rate on a planar surface of the same

crystallographic orientation, whereas this is not necessarily true. In Section 2 we pointed out that the oxidation rate can be affected strongly by stress. In high-stress cases, the oxidation rate along the trench sidewall may decrease from its low-stress value. Also, the STI model spatially averages the stress throughout the oxide-filled trenches and silicon mesas, and thus cannot predict the localized stresses that result in the STI patterns.

To adequately address the shortcomings of the model requires a considerably more sophisticated approach—one involving, at a minimum, the use of three-dimensional stress analysis and three-dimensional oxidation models. From this viewpoint, the leverage of the present model can easily be appreciated. Despite its limitations, it correctly predicts the trends in stress generation observed experimentally, and provides an intuitive understanding of oxidation-induced stress as a function of process conditions and pattern geometry.

4. Dislocations nucleated by ion implantation

The foregoing discussions illustrate how oxidation conditions and silicon pattern shapes can determine the susceptibility of IC structures to oxidation-induced defect generation. Although oxidation conditions and device geometries that minimize the stress in the silicon substrate will minimize the probability of dislocation generation, complete avoidance of stress buildup is never accomplished for actual IC structures. A key question is therefore what level of stress can be sustained in the silicon substrate before the onset of dislocation generation. The process of ion implantation often plays a critical role in determining this level.

Ion implantation, by its nature, disrupts the crystallinity of the substrate. A subsequent high-temperature annealing step is always necessary to repair the damage and activate the dopant implanted. Even in unstressed substrates, there is almost always some residual implantation damage left behind after annealing. As long as the damage is confined to areas outside space-charge regions, these residual defects usually have no detrimental effects on device operation. Unfortunately, in stressed material these defects can become dislocations that glide large distances outside the implanted region. Elimination of this effect often requires reducing stress levels below that which would be tolerable without the implantation step.

We illustrate the effect of ion implantation on defect generation using an example from a bipolar IC process. As in the example of Section 3, stresses in the substrate originate during the device-isolation steps; however, a different type of isolation scheme is used. The scheme used creates a "deep-trench isolation." Figure 10 shows the process sequence used to fabricate the isolation trench. The trench is etched to a depth of $4.5\ \mu\text{m}$ using an oxide/nitride layer as an etch mask [Figure 10(a)]. After a

chemical etch to remove RIE damage, the wafer is oxidized to grow approximately 300 nm of oxide. At this stage the trench appears as shown in Figure 10(b). Note the widening of the trench at the depth of the buried subcollector. This is caused by preferential etching of the n^+ layer during RIE damage removal and by the fact that n^+ silicon oxidizes faster than lightly doped material. The trench structure is completed by removing the oxide at the bottom of the trench by etching, filling the trench with polysilicon (POLY), planarizing the surface, and growing an oxide cap [Figure 10(c)].

Several factors contribute to stress buildup during trench fabrication. Stresses originate from the oxidation processes, from differences in thermal expansion of the silicon and oxide, and from the intrinsic stress of the polysilicon. (We defer a discussion of intrinsic stress in polysilicon until the next section, which deals with polysilicon-filled DRAM capacitor trenches.) The matter is more complex because of the three-dimensional nature of the isolation trenches. The cross-sectional view of Figure 10 only partially illustrates how the stresses are generated. Viewed from above, the isolation trench appears as a moat, laid out in a winding pattern as called for by the circuit design (Figures 11 and 12). At locations where trenches form corners, large stresses can be generated—stresses much larger than a plane-strain analysis of a trench cross section such as that in Figure 10 would indicate. A thorough stress analysis of isolation trenches has been presented by Hu [55].

As in the case of the STI patterns in Section 3, several cell layouts were examined. In one type of cell layout, devices were isolated by completely surrounding them with trenches (Figure 11). A reasonable set of process conditions (temperatures, times, oxide thicknesses) was used to create the desired device islands without generating dislocations. However, after subsequent implantation and annealing, dense arrays of dislocations were found to be present in all the cells. The problem is illustrated in Figure 11. A phosphorus ion implantation is performed in the regions indicated in part (a). This implantation is used to make contact with the buried subcollector and is known as a “reach-through” implantation. After annealing to activate the phosphorus, glide dislocations are generated near the corners of the cell that received the implant. As can be seen from a plan-view micrograph of the cell [Figure 11(b)], the dislocations glide outside the implanted area. Although not visible in this micrograph, these glide dislocations can cross-slip to adjacent $\{111\}$ planes. By this process, dislocations glide farther than if they remained on their original glide plane, and a greater proportion of the cell becomes populated with dislocations.

None of these types of defects appeared in similar patterned structures that did not receive implantations, nor

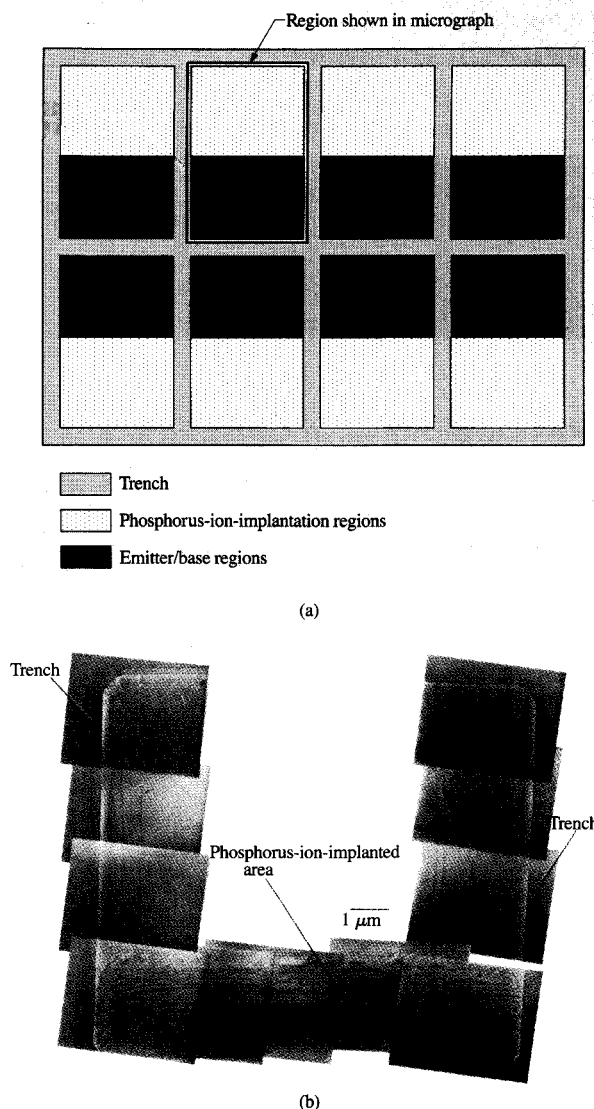
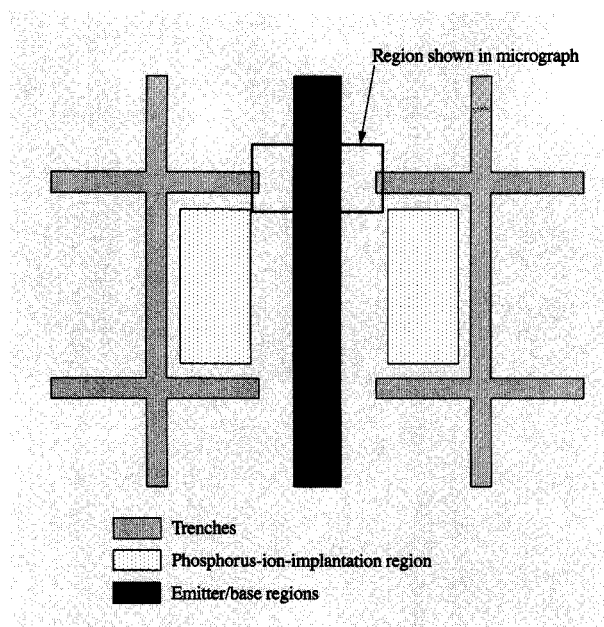


Figure 11

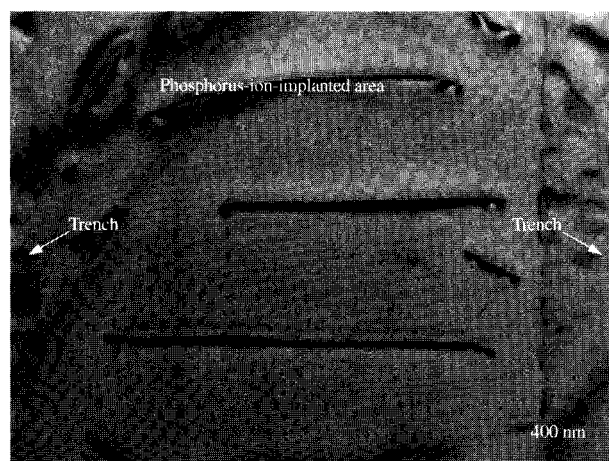
Dislocations generated by ion implantation: (a) Bipolar cell array. (b) TEM micrograph of region highlighted in (a). Dislocations generated by phosphorus ion implantation propagate throughout most of the cell because of stress at the trench edges.

did they appear in unpatterned wafers that received identical implantation and annealing steps.

Why does implantation lead to dislocation generation? The exact details of the processes responsible for defect generation are not known with certainty, but a reasonable description of the situation is as follows. After the isolation process, some amount of residual stress exists in the silicon around the trenches; however, the level of stress is not enough to generate dislocations. Implantation produces



(a)



(b)

Figure 12

Confinement of generated dislocation by changing layout: (a) An alternative cell array layout to that shown in Figure 11. (b) Transmission electron micrograph, indicative that dislocations remained confined to the phosphorus implantation region.

both point defects and extended regions of disorder in the silicon. Each type of defect can serve as nuclei for dislocation formation. Once dislocations are formed, the stress in the silicon causes them to glide. The glide process can easily occur in moderately stressed material, since the energy necessary to induce glide is much smaller than that necessary for the nucleation of dislocations.

Another experiment provides further insight into the problem of dislocation nucleation. Dislocations such as

those shown in Figure 11 can be avoided if phosphorus diffusion from a chemical source such as POCl_3 is used, rather than ion implantation. This result is interesting for two reasons. First, because the covalent bonding radius of phosphorus is smaller than that of silicon ($1.10 \text{ \AA}$ vs. $1.17 \text{ \AA}$, respectively [56]), there is always a possibility that misfit strain adds to the trench-induced strain and subjects the silicon to a stress level beyond its critical shear stress. The phosphorus diffusion experiment shows that in our case misfit strain does not play a role in dislocation generation. Second, it is known that phosphorus diffusion from a POCl_3 source generates silicon self-interstitials, and at much higher levels than oxidation processes [57]. If stress-induced agglomeration of self-interstitials is responsible for the generation of dislocations, there must be something qualitatively different about introducing self-interstitials by ion implantation rather than by oxidation or POCl_3 diffusion. In the case of implantation, some regions of the crystal contain clusters of interstitials at the beginning of the subsequent annealing step, which could then act as the nuclei for dislocation generation. In contrast, oxidation and POCl_3 diffusion are expected to introduce point defects relatively uniformly into the substrate. In addition, it is well known that ion implantation often leads to the phenomenon of transient-enhanced diffusion, in which large diffusion enhancements occur for the first few seconds of activation annealing, followed by a return to normal thermal diffusion rates (see for example the article by Michel et al. [58]). Large diffusion enhancement in a very short time implies a high degree of point-defect supersaturation. It could simply be the case that ion implantation results in larger point-defect supersaturations than oxidation or POCl_3 diffusion. As an alternative to point-defect agglomeration, it could be the extended regions of disorder in the silicon following implantation that turn into dislocations.

To eliminate dislocations with the cell design of Figure 11, new processing conditions must be found that lead to much less oxidation-induced stress. The discussions in Sections 2 and 3 have presented examples of how this can be achieved. Another approach involves the use of a different cell design—one that is less prone to stress buildup. An alternative cell design is depicted in Figure 12. This layout design greatly alleviates problems of stress-induced dislocation generation. Note in Figure 12(a) that the phosphorus-ion-implantation region is located away from any trench edges, and, in particular, is located as far away as possible from any corners formed by intersecting trenches. Figure 12(b) is a TEM micrograph of the region indicated in Figure 12(a). Dislocation half loops extending to the surface can be seen in the phosphorus-ion-implanted region. The important point is that these defects do not propagate out of the implanted region and therefore have no detrimental effect on device performance.

The example presented in this section clearly shows that ion implantation can greatly reduce the tolerable levels of stress in silicon because it provides nuclei for dislocations. Since the energy necessary to move dislocations by glide is orders of magnitude lower than that necessary to overcome the nucleation barrier, dislocations generated by implantation can subsequently glide and multiply in moderately stressed material. The STI example in Section 3 has illustrated how appreciably oxidation conditions and layout geometry can affect the susceptibility of an IC structure to stress-induced defect generation. The example presented demonstrates that ion-implantation processes can further constrain the choice of acceptable process conditions.

5. Dislocations in a DRAM trench capacitor process

Next we examine the origin of dislocations that can emanate from capacitor trenches in a 4Mb DRAM cell if their fabrication is not properly controlled. Dislocations from an uncontrolled process can nucleate predominately after a particular ion-implantation step and (from TEM micrographs) are observed to form distinctive shapes as they propagate away from the capacitor trenches. Thus far, we have described the use of TEM to identify conditions under which the deleterious effects of dislocations can be avoided. We now focus on studying the shapes of the dislocations in order to infer the nature of the stress sources responsible for their movement. This analysis provided a method of developing a process that avoids dislocation generation.

It is worth reiterating that the dislocation problem and analysis discussed here are not tied to a particular IC structure. Although we have chosen to focus on concerns related to trench structures, similar concerns pertain to ICs without trench structures. A good example is provided by the recent work of Onishi et al. [2], who have examined stress-induced dislocation generation in planar-capacitor DRAMs.

• Dislocation generation

Figure 13 depicts a fabrication sequence for a 4Mb DRAM cell, including formation of a PMOS transfer device. During memory operation, charge is read from or stored to a trench capacitor by charge transfer between the PMOS transistor and the capacitor. (The electrical connection between the transistor and capacitor has not yet been formed at the point in the processing shown in the figure.) A trench capacitor [Figure 13(a)] is formed by RIE, lining the inside of the trench with a triple-layer dielectric of oxide/nitride/oxide, filling with polysilicon, and planarizing. Device isolation is achieved by a semirecessed oxidation (SROX) process [Figure 13(b)]. An oxide/nitride layer covers the device-active areas, and the rest of the exposed

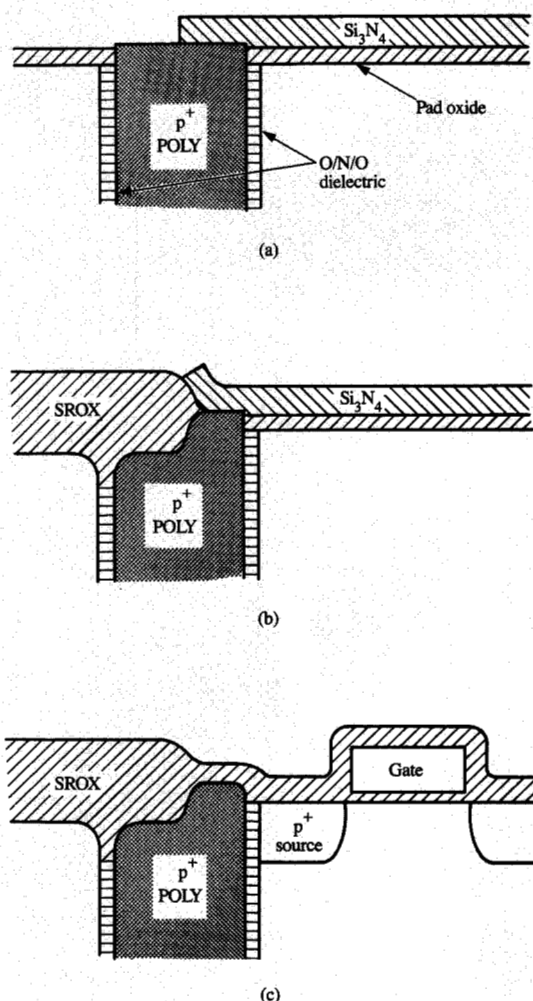


Figure 13

Fabrication sequence for a 4Mb DRAM cell: (a) A capacitor trench is formed with an oxide/nitride/oxide (O/N/O) dielectric liner and a polysilicon "fill." (b) A semirecessed oxidation (SROX) process is used to electrically isolate cells. (c) A high-dose boron implantation is used to form the source and drain portions of the transfer device. Dislocations that originate in the source region appear after annealing for dopant activation.

silicon is oxidized. The trenches are partially covered with nitride during this oxidation. A pivotal point in the processing occurs at the step shown in Figure 13(c). Source and drain are formed by ion implantation of boron. Immediately after annealing (at temperatures above 800°C), gliding dislocations form next to the trench and propagate into the transfer device. The dislocations lie on {111} planes and glide in [110] directions. The defects do not

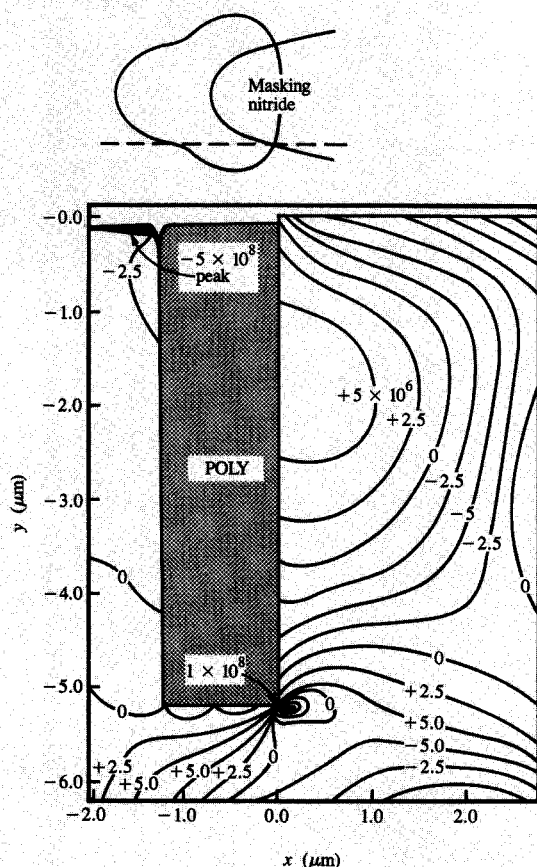


Figure 14

FEDSS simulation. Contours of stress (in dynes/cm²) resolved on the (111) plane, immediately after the SROX step shown in Figure 12(b).

appear if no ion implantation is performed before the SROX process, and also do not appear if the SROX process is omitted. Thus, the trench and isolation structures by themselves do not experience high enough stresses to cause dislocations. The experimental observations suggest that the gliding dislocations nucleate from implantation damage with the assistance of some finite amount of stress in the implanted regions.

Note the presence in Figure 13(b) of the vertical bird's beak along the dielectric liner on the left side of the trench capacitor. This is analogous to driving a "wedge" between the polysilicon and the surrounding silicon. From the discussion in Section 3, where a similar analogy was made to vertical oxidation creating a wedge at the edge of the shallow trench sidewall, it was expected that oxidation along the liner would lead to the development of large

stresses in the surrounding substrate. However, no defects were found on the side of the trench where no oxidation occurred. This result indicates the importance of the nucleation of dislocations by the boron-ion-implantation step. **Figure 14** shows contours obtained from a FEDSS [28] simulation of the stresses in the silicon substrate prior to source-drain implantation. Implantation and defect generation occur on the right side of the trench in **Figure 14**. The contours are calculations of the resolved shear stress on the plane in which the defects lie, and in the direction in which they glide. (The vertical and horizontal axes are in the [001] and [110] directions, respectively; the contours are calculations of the resolved shear stress on the (111) plane in the $[1\bar{1}0]$ direction.)

Figure 15 shows a plan-view transmission electron micrograph of a DRAM cell. Its gate oxide, gate conductor, and oxide isolation have been removed from the device silicon, which has been chemically thinned from the back. The trench capacitor remains attached to the silicon. This region appears dark in **Figure 15** because the trench is deep enough that it is not transparent to the electrons of the electron microscope. Dislocations are found that run from the surface near the edge of the trench adjacent to the transistor through its source.

Avoidance of such dislocation generation was achieved by taking a different approach from that used in the case of the deep-trench isolation example of Section 4 (**Figures 11 and 12**). Rather than change the cell layout, the origins of the stress causing the dislocations were analyzed and process conditions modified to eliminate defect generation. In principle, modification of the cell layout would also be an effective method of eliminating dislocations, for example by moving the source region of the transfer device away from the trench capacitor and connecting the two by a strip of metallization. But this approach would result in a larger, unacceptable cell size—density is, after all, the major driving force behind development of each new generation of memory chips—and would introduce additional processing complexity.

The dislocations in the present case have a more regular morphology than the dislocation tangles associated with the oxidation of shallow trenches (**Figure 8**). Their characteristic features can be seen in **Figure 16**. This figure also illustrates the three-dimensional nature of the DRAM structure. The bowed-out dislocation lines are located on {111} planes that intersect the implanted source region. Their Burgers vectors lie in these planes—which indicates that the dislocations are glissile—and they form an angle of 45° with the wafer surface. The shape of a particular dislocation line is not symmetric with respect to the center plane through the trenches (indicated by section A1-A2); instead, the bow-out is larger in the direction of its Burgers vector. Therefore, the segment with the deepest penetration is close to a pure edge orientation. (In **Figure**

15 this section was so deep that it was removed during thinning of the electron microscope specimen.) The sign of the Burgers vector was determined by conventional diffraction contrast methods. The sign was such that the extra half-planes of the edge components pointed away from the surface. If the dislocation lines are collapsed toward their center of curvature—opposing the driving force that brought them to their observed locations—the region from which the dislocations had originated is revealed, and this origin lies in the implanted region. Upon expansion to the observed shape, the continuity of the crystal requires a surface step along the line where the dislocation intercepts the surface. The observed sign of the Burgers vector requires a step that shortens the surface along this section and indicates yielding to compression; the step is indicated in section A1–A2 of Figure 16.

• Stress analysis

The analysis of the stresses that develop can be carried further to a stage that allows quantitative estimates. A dislocation comes to rest at a position where the stress that causes glide is equal to the forces that oppose further glide. The stress that causes glide is the resolved shear stress on the $\{111\}$ glide planes in the direction of the Burgers vector. The opposing forces are friction stress, line tension forces, and forces that arise from interaction with other dislocations. The outermost dislocation of Figure 15, which had penetrated the deepest, moved unimpeded by other dislocations and expanded to a large radius of curvature. Hence, it was inferred that only the friction stress opposed further glide. The shape of the dislocation line could be used to map the locations where the process-induced shear stress had diminished to the magnitude of the friction stress. The spatial distribution of the shear stresses could then be compared to model calculations derived from reasonable analytic approximations.

The following analysis is similar to the very thorough analysis of film-edge-induced dislocations in silicon substrates by J. Vanhellemont et al. [59, 60]. These authors presented an analysis of forces exerted on a dislocation, utilizing the complete Peach–Koehler relationship. For the present work a simplification is in order. The Peach–Koehler formula produces the glide force that is proportional to the resolved shear stress in the glide plane, and another force component normal to the glide plane. The latter causes dislocation segments to climb out of their glide planes, which requires emission or absorption of point defects. This occurs only if the self-diffusivity is sufficiently high or if a supersaturation of point defects exists. After climb, dislocations can be left in tangled configurations, in which case it is not possible to extract characteristic stress-related elements, such as glide planes and directions [shown in Figure 16(a)]. The current

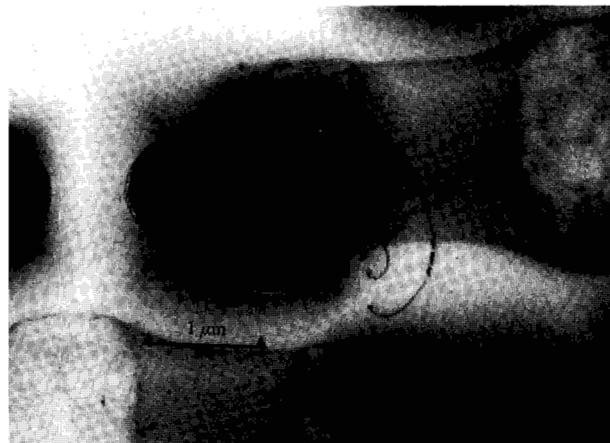


Figure 15

Transmission electron micrograph of a DRAM cell with storage capacitor and device pedestal. Dislocations with distinctive shapes are generated in regions next to the capacitor trench that received a high-dose boron implantation to form the source and drain regions of the transfer device.

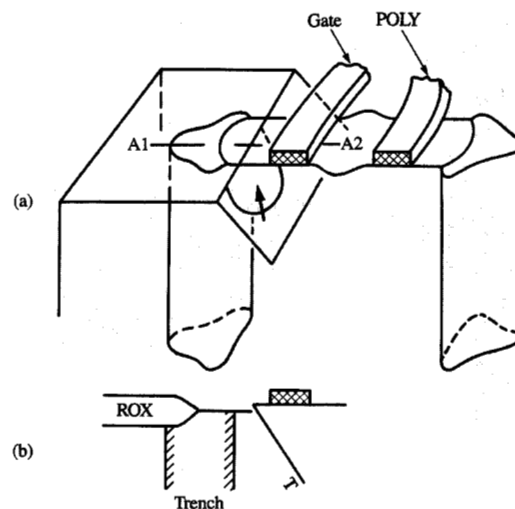


Figure 16

Schematic of DRAM cell: (a) Schematic drawing of two device cells with outline of silicon device pedestal and a (111) glide plane with a dislocation in front of a trench capacitor. (b) Section A1–A2 of (a), showing the surface step associated with the slip of the dislocations in Figure 14.

analysis is, therefore, confined to the glide force. The task is to assume a model for the stress source and to derive the resolved shear stress for the observed glide systems. For the capacitor trenches, two models were considered.

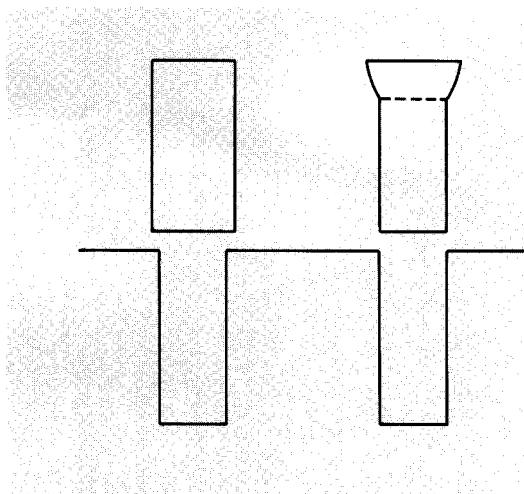


Figure 17

Models for the generation of internal stresses by trench capacitors. Plugs that are too large to fit into openings, either along their entire length or with dilation concentrated at the surface.

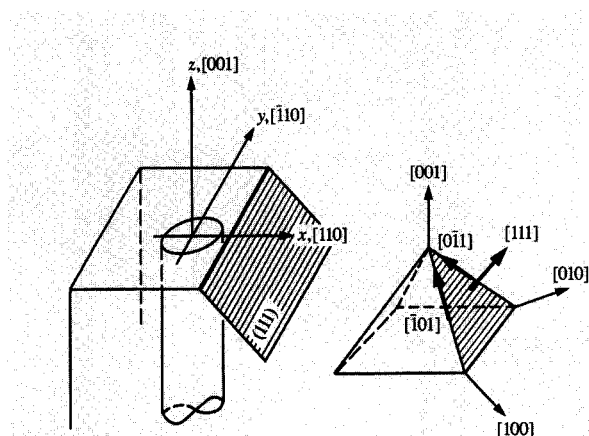


Figure 18

Relationship between coordinates of device geometry and crystallographic elements of crystal defects: glide plane normal $[111]$ and Burgers vector directions $[\bar{1}01]$ and $[0\bar{1}1]$.

The first model was a cylindrical plug that is too large for an opening (Figure 17). The choice of this model was guided by the processing sequence: First, holes are etched into the substrate and lined with thin dielectrics. Then they are filled with chemically vapor deposited (CVD) polysilicon. Deposition processes as a rule form layers that trap intrinsic strains; CVD polysilicon is no exception. A

number of studies have examined the intrinsic stress in thin films of polysilicon deposited on planar substrates [61–66], and have reported polysilicon to be in a state of compressive stress. The compressive nature of the stress is also consistent with our TEM analysis of dislocations.

The second model investigated was a variation of the first: Only the top of the plug is assumed to be too large for the opening. We constructed this model after considering the fact that no dislocations appear after implantation if the trench is not previously oxidized. The concentrated dilation at the top of the plug should then approximate the effect of surface oxidation inducing compression in the silicon.

We show in some detail the analysis for the model of the plug that is uniformly too large to fit into an opening. For simplicity a circular plug in an infinitely large plate (plane stress) is considered. Although the actual trench is not circular and does not extend through the whole thickness of the wafer, this model is an adequate approximation for the region in front of the trenches where the dislocations are observed, according to Saint-Venant's principle: At distances away from the surface of the stress source that are large compared to the dimensions over which the forces vary on the surface, the stress distributions do not depend on the exact shape of the stress source, provided the net resultant forces of the real and idealized stress source are equal.

From Timoshenko's chapter on thermal stress [67], the stress system can be characterized by replacing the differential thermal contraction strains with the intrinsic strain. In cylindrical coordinates its principal components are compressive radial stress,

$$\sigma_r = -A/r^2, \quad (9a)$$

and tensile hoop stress,

$$\sigma_\phi = A/r^2, \quad (9b)$$

where

$$A = \frac{1}{2} \epsilon E R^2, \quad (9c)$$

and ϵ is the (intrinsic) strain to which the plug must be compressed to fit into the opening, E is Young's modulus (1.6×10^{12} dynes/cm² for Si), and R is the radius of the plug, chosen such that it has the same cross-sectional area as the capacitor trench ($R = 0.85 \mu\text{m}$) in the DRAM cell discussed earlier in this section.

Frequently the natural coordinates for models of stress sources are not rectangular ones, and the natural coordinates must be transformed into coordinates aligned with the pattern directions on the wafer. This coordinate system is shown in Figure 18. In the present case this gives rise to three stress components; there are two normal stresses and a shear stress:

$$\sigma_{xx} = A(y^2 - x^2)/(x^2 + y^2)^2, \quad (10a)$$

$$\sigma_{yy} = A(x^2 - y^2)/(x^2 + y^2)^2, \quad (10b)$$

$$\tau_{xy} = -2Axy/(x^2 + y^2)^2. \quad (10c)$$

Finally, resolved shear stresses must be assembled from these components with direction cosines between the different axes as coefficients. For this step the use of a consistent set of crystallographic indices such as those indicated in Figure 18 is very helpful. For the glide plane normal $([111])$ and the Burgers vector directions $([\bar{1}01])$ and $[0\bar{1}1])$, which are indicated in Figure 18, the resolved shear stresses are

$$\tau_{b1} = (-\sigma_{xx} + \tau_{xy})/\sqrt{6}, \quad (11a)$$

$$\tau_{b2} = (-\sigma_{xx} - \tau_{xy})/\sqrt{6}, \quad (11b)$$

respectively. The choice of the plane-stress approximation results in expressions that are independent of depth. Contours of constant resolved shear stress τ_{b1} are plotted in Figure 19 (with arbitrary scale). Each contour reaches its largest distance from the center of the stress source at its intersection with the dashed line, which forms an angle of 22.5° with the x -axis. Along these intersections the resolved shear stress is

$$\tau_{b1l} = \frac{A}{\sqrt{3}r^2}, \quad (12)$$

where r is the radius of the plug. The corresponding figure for τ_{b2} is the mirror image with respect to the plane $y = 0$ (or section A1-A2 in Figure 16). These contours can be considered projections of shear stress values onto a plane parallel to the surface of the wafer. Transmission electron micrographs also show projections of dislocations from a glide plane onto a plane parallel to the surface. Therefore, Figures 15 and 19 can be compared directly.

It is obvious that the asymmetry of the contours with respect to the plane $y = 0$ correctly reflects the asymmetry of the bow-out of the dislocation lines with respect to the center plane A1-A2 in Figure 16. This result supports, qualitatively, the validity of the assumed stress source. Quantitative estimates can also be made. According to the preceding discussion, the shape and position of the dislocation that has traveled the farthest should mark the contour where process-induced stress has diminished to the value of the friction stress. Equating the contour of deepest penetration with the friction stress τ_c allows us to estimate the magnitude of $A = \epsilon ER^2/2$ of the stress source. The interesting contribution to A is the intrinsic strain of the material that fills the trench, ϵ . Equation (12) gives

$$\tau_c = \frac{\epsilon E}{2\sqrt{3}} \left(\frac{R}{r} \right)^2. \quad (13)$$

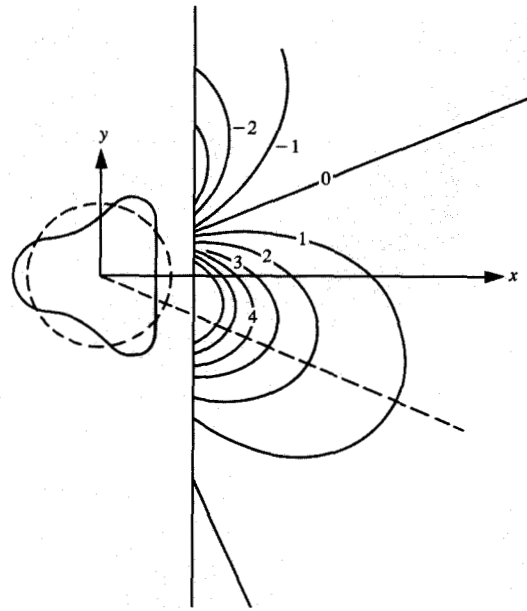


Figure 19

Contours of constant shear stress on (111) planes, resolved in the $[\bar{1}01]$ direction, in arbitrary units.

The distance of farthest glide is measured from micrographs such as Figure 15, giving $r = 1.9 \mu\text{m}$. Using this value in Equation (13) yields

$$\tau_c = 0.9 \times 10^{11} \epsilon \text{ dynes/cm}^2. \quad (14)$$

The value of the friction stress depends on many parameters, e.g., temperature, oxygen content, thermal history of the silicon material. Current views have been summarized by Vanhellefont et al. [59, 60]. The values of τ_c fall within the range $0.1-1 \times 10^8 \text{ dynes/cm}^2$. Using these values in Equation (14) permits us to estimate the intrinsic compression ϵ that must be present in the trenches in order to push dislocations to their observed positions. We estimate ϵ to be in the range $0.1-1 \times 10^{-3}$. These values are in good agreement with those found in a separate study.* We thus conclude that modeling a stress source from the trench region as a swollen cylindrical plug is reasonable.

We have applied the same analysis to the alternative model of a center of dilation concentrated at the wafer surface. The analytic expressions were taken from Nowacki's derivation [68] of the stress of a nucleus of thermo-elastic strain in an elastic semispace. This model predicts that shear stress decreases more rapidly along the glide planes than the swollen plug model: The model with a center of dilation at the surface predicts a $1/r^3$

*J. V. Niccoli, unpublished work, March 1988.

dependence on stress, whereas the swollen plug predicts a $1/r^2$ dependence. Also, the bow-out of the shear stress contours is much less prominent for the center-of-dilation model compared to the contours shown in Figure 19. The rapid decrease predicted by assuming a center of dilation concentrated at the surface does not account for the observed depth of penetration of dislocations.

Considering that no dislocations are formed in the absence of an SROX step, it is a bit surprising that the swollen-plug model alone works so well; that model simulates only the intrinsic stress of the trench fill and does not take account of the SROX process. A detailed comparison of the shape of the computed contours with the dislocation shapes shows that near the trench, the swollen-plug model predictions in Figure 19 deviate from TEM observations. The dislocations spread farther in the lateral direction, parallel to the trench face, than predicted by the model. Deviations from model predictions are not completely unexpected: The circular plug approximation loses accuracy near the trench wall, where the actual shape of the trench becomes important in determining stress distributions. But the lateral spread of the dislocations is also consistent with the existence of an additional stress source concentrated near the surface of the trench. This would, of course, arise from the SROX oxidation.

After combining stress analysis with TEM observations, we conclude that stress from the polysilicon in the trenches is responsible for the deep penetration of dislocations. A radial compressive stress from the trenches predicts the shape of the dislocations quite effectively. However, it appears that this stress is not solely responsible for the propagation of dislocations. Oxidation-induced stress must also play a role. It is likely that oxidation-induced stress from the SROX process—short-range in nature—adds to the stress already present around the trenches to push the dislocations away from the trench edges; the final dislocation shapes and depths of penetration are determined by the longer-range stress fields emanating from the trench fills.

• *Elimination of dislocations*

Two general approaches can be followed to eliminate dislocation generation in DRAM cells: Reduce the amount of stress in the substrate or eliminate the source of nucleation for dislocations. In practice, the approach that can more easily be implemented is the one adopted.

Reduction of the oxidation-induced stress can be accomplished by raising the temperature of oxidation; we discussed the reasons for this in detail in Section 2. The highest allowable temperature is determined by the amount of additional dopant diffusion that can be tolerated. Other, less obvious changes in processing steps can also be made that will reduce stress—for example, changes in masking

nitride thicknesses or the amount of undercutting that occurs in the oxide under the masking nitride during pattern definition. Process-simulation programs such as FEDSS are well suited for examining how these types of changes in processing affect the final amount of stress in the substrate. Process simulation is also very helpful in estimating the amount of dopant diffusion that will result from different thermal cycles.

TEM analysis has been used to identify stress arising from polysilicon as an important contributor to the generation of dislocations. Numerous studies [61–66] have shown that the amount of intrinsic stress in as-deposited polysilicon films depends on a variety of factors, including method of deposition, doping level in the polysilicon, and oxygen content of the films. These studies have also shown that subsequent annealing will change the stress levels from their as-deposited values. Fortunately, there are many different variations of deposition, doping, and annealing that are compatible with the electrical requirement that the final polysilicon act as a capacitor plate. In practice, process conditions leading to the lowest-stress polysilicon-filled trenches can generally be found through experimentation.

The nucleation of defects by ion implantation can substantially reduce the amount of stress necessary to generate harmful dislocations. It is obvious that a great deal more flexibility in choosing processing conditions would be possible if certain implantation steps could be avoided. However, ion implantation is currently the predominantly used method for doping silicon and will not easily be displaced. An interesting variation of the usual implantation and annealing technique involves implanting a dopant into thin metal or silicide layers on the surface and then outdiffusing it into the substrate [69–75]. Metals and silicides typically have high stopping powers for dopants, so the dopants as well as implantation damage remain confined within the layers. Thus far, the primary motivation for investigating outdiffusion from silicides has been the desire to develop a process for forming very shallow junctions. The potential for eliminating stress-induced dislocations may prove to be an additional driving force for studying this doping technique. As such studies continue, alternative diffusion approaches, compatible with IC processing requirements, will undoubtedly emerge.

6. Concluding remarks

Avoidance of the deleterious effects of stress-induced dislocations has become more challenging with each succeeding generation of IC processes. Packing devices more closely on a chip and reducing active device areas and isolation areas leads to the development of higher stresses. In addition, the drive toward low-temperature processing, which minimizes dopant diffusion, also leads to the development of higher stresses by reducing the ability

of the materials used to relieve their stress by flow processes.

On the other hand, our understanding of oxidation-induced stress and its relation to processing conditions has improved significantly in the past few years [13–15, 29, 34–36, 42]. Increasingly sophisticated models of oxidation have resulted in better understanding of how stress during oxidation results in oxide-thinning effects on the corners of silicon structures. This is a positive development: Models that accurately predict oxide shapes under highly stressed conditions are also expected to yield predictions of associated substrate stress. We have also moved beyond the stage of simply performing a matrix of experiments and searching for process conditions where TEM micrographs show no dislocations. We have provided a detailed example of how TEM observations and stress analysis were used effectively to correlate dislocation propagation with stress from polysilicon-filled trenches. In contrast, by only noting under which processing conditions dislocations appear, one could reasonably conclude that oxidation-induced stress alone is responsible for dislocation generation. Subsequent work has shown that dislocation densities can indeed be reduced significantly by using deposition and annealing conditions that minimize the stress arising from deposited polysilicon films. From these types of studies, a widening knowledge base is developing regarding the sources of IC stress, how they appear in device and circuit structures, and how stress can be alleviated through changes in process conditions or modification of material properties.

Present research is directed at gaining a better understanding of the nucleation of dislocations. We believe that excess point defects, such as those introduced during implantation or oxidation processes, somehow form the nuclei for dislocations. However, associated details are not currently understood. For example, it is not understood how point defects that normally form end-of-range dislocation loops are converted into gliding dislocations in the presence of stress. Although, in regions of tensile stress, interstitial point defects easily agglomerate to form the dislocations of interstitial character observed with TEM, gliding dislocations are often found in regions of compressive stress; for example, the gliding dislocations moving away from the trench in Figure 15. Obviously, an understanding of the transition from an excess of point defects to the appearance of gliding dislocations is needed. More knowledge about the details of nucleation may yield new ideas on how to prevent dislocation formation, and could potentially improve our predictive capabilities, i.e., our ability to view a particular process or circuit layout and identify which conditions minimize the likelihood of dislocation generation.

Although concerns regarding stress-induced dislocations in silicon substrates are not new in the silicon integrated

circuit field, our knowledge regarding such dislocations will need to keep pace with the demands of the field if it is to continue to evolve toward high packing densities. Our view is that controlling stress-induced dislocations will remain a challenging but achievable goal.

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