Preface

A remarkable aspect of the microelectronics industry is how quickly it has evolved. The number of on-chip components of silicon integrated circuits has been following the well-known trend of doubling every two years since the early 1960s. This trend is expected to continue, though at a somewhat slower pace due to increased technology complexity and manufacturing cost. The major driving force behind the trend has been the shrinkage of lateral device and circuit dimensions, primarily as a result of photolithographic improvements. However, continuation of the trend is expected to depend increasingly on the shrinkage of vertical dimensions as well.

Current and projected processing of semiconductor devices involves additive processes, in which materials of various types are added to a wafer (substrate) through deposition, growth, implantation, or chemical reactions; and subtractive processes, in which unwanted materials are removed by chemical and mechanical means. Additive and subtractive processes must be compatible with pattern definition, submicron lateral dimensions, and atomic-scale vertical dimensions. Progress of the microelectronics industry will rely strongly on the ability to fabricate smaller and increasingly complex structures. This will require an increase in the fundamental understanding of relevant materials and processes. Levels of defects and contaminants introduced during processing will need to be lowered and/or controlled. Moreover, the control and characterization of relevant surfaces and interfaces will become critical to the processing because of the smaller device dimensions.

This issue focuses on some key areas of materials science for silicon technology that are under investigation at IBM. Each paper provides a state-of-the-art review of a particular area, focusing on the specific contributions of the authors and their colleagues.

The need for accurate definition of submicron-scale patterns in electronic materials during the fabrication of VLSI circuits has been the major driving force behind the introduction of plasma-based anisotropic etching techniques. The paper by Oehrlein and Rembetski presents the principles underlying the achievement of directionality and selectivity in reactive ion etching. It also shows that etch directionality and selectivity can lead to contamination and substrate damage; their minimization requires the introduction of additional treatments, thus complicating processing. Improved etching tools and procedures which minimize contamination and damage are required for increased productivity and reliability.

Higher circuit densities are achieved by developing devices that occupy smaller areas of the substrate and by packing them closer together. The scaling of device dimensions and of associated isolation structures leads to an increase in substrate stress, which produces unwanted dislocations. After nucleation, the dislocations develop within (or move into) regions in which they can affect devices. Two common processes that foster dislocation nucleation are oxidation and ion implantation. In addition, the drive toward low-temperature processing, which minimizes dopant diffusion, can also lead to higher substrate stress by reducing the ability of the materials involved to relieve their stress through flow processes. The problem of controlling stress-induced dislocations is a very challenging one. The paper by Fahey et al. reviews this important area and provides some examples that illustrate the underlying causes of substrate stress, how associated dislocations are generated, and possible solutions.

The continuing miniaturization of silicon devices necessitates an ever-increasing level of sensitivity in the analytical probing of surfaces, interfaces, and defects. Higher reliability requirements and the need for improved control of manufacturing processes dictate a more precise understanding of materials behavior and defect evolution at each process step. Highly sensitive analytical techniques are needed in order to identify underlying physical and chemical phenomena and develop effective manufacturing solutions. Often, especially in realistic structures, that requires the combined use of several such techniques. The paper by Kuan et al. reviews the applicability to the silicon technology of several highly sensitive analytical probing techniques, each with its unique capabilities for materials analysis.

The continuing miniaturization of silicon devices also necessitates improvements in the modeling of the electrical characteristics of such devices, and raises fundamental questions concerning our understanding of the behavior of small devices. Advanced semiconductor devices are characterized by very rapid variations of the electric fields and carrier concentrations. These variations can occur over distances comparable to the distance between scattering events in the semiconductor substrate. Detailed physical models are necessary for microscopic transport to be studied realistically. In addition, three-dimensional models are needed to address the geometrical dependencies of small structures. Increasing either the geometric dimensionality or the physical rigors of a device model often incurs the expense of increased computing times. Therefore, a judicious choice of the model used to study the particular problem at hand is necessary for rapid and efficient learning. The paper by Lee et al. discusses and applies models of various levels of sophistication to characterizing aspects of the electrical behavior of advanced devices. Future directions in numerical device modeling are also presented.

The last paper of this issue, by Rubloff and Bordonaro, discusses an emerging strategy for microelectronics processing in which sequential process steps are linked by

wafer transfer through a clean, controlled environment. This strategy is dictated by the need for component reliability, considering the increasing number and complexity of the process steps required in the manufacture of microelectronic components. Key aspects of the applicability of integrated processing to research, development, and manufacturing are presented. The paper focuses particularly on surface cleaning, low-temperature epitaxy, thermal oxidation processing, and real-time process monitoring and control.

Efforts to increase the fundamental understanding of the materials and processes of strategic importance to the silicon technology are certain to play an increasingly important role in its continued development. The papers in this issue are illustrative of such efforts.

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Guest Editor