TDI charge-coupled devices: Design and applications

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The design and applications of charge-coupled devices (CCDs) operated in the time-delay-and-integration (TDI) mode are reviewed. Design issues regarding the use of the TDI-CCD imager for visible imaging applications are discussed. Aspects pertaining to its parallel array, serial-to-parallel interface, serial register, modulation transfer function (MTF), discrete charge motion, motion synchronization, clocking, number of integrating stages, noise, dynamic range, sensitivity, output uniformity, device yield, pixel size, and spectral response are highlighted in the context of their effect on system performance. Its imaging characteristics are compared to those of the photodiode linear array imager, and design studies and experimental results for a family of TDI-CCD imagers for scanning documents and museum art objects are described.

1. Introduction

The time-delay-and-integration charge-coupled device (TDI-CCD) imager [1, 2] may be one of the earliest CCD imagers to have made use of on-chip signal processing [3]. The general concept of time-delay and integration can be applied to imaging and signal processing in many forms. Since the mid-1970s, many papers have documented the development of TDI-CCD imagers. Their earliest applications were primarily in military reconnaissance and satellite imaging; imager size and resolution were not large. Recently, there has been renewed interest in such imagers, mostly in connection with civilian applications such as document scanning and industrial product inspection. Furthermore, imager speed and resolution have been increased. Imaging in connection with document scanning, multimedia display, facsimile, digitization of conventional silver-halide-based photographic films and prints, museum art object archiving, desktop publishing, and image database generation, to name a few, often require that images be captured with a high-quality, high-speed, high-resolution imaging device. The TDI-CCD imager has been demonstrated to be well suited for that purpose.

In this paper,* we review work on the TDI mode of operation for solid-state CCD imagers. We concentrate on aspects that pertain to the design of monolithic silicon

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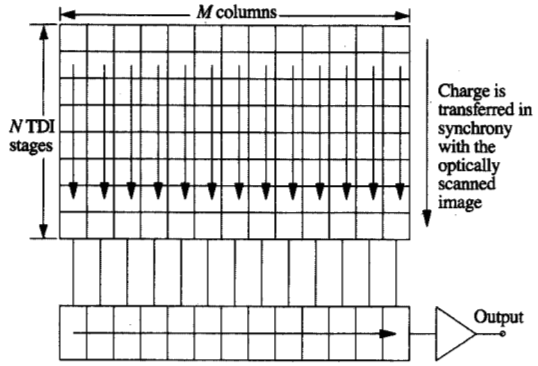


Figure 1

Schematic illustration of the TDI mode of operation.

TDI-CCD imagers for visible imaging. An extensive, although by no means exhaustive, list of references on TDI-CCD imagers is included.

In Section 2, we discuss the basic principles of the TDI mode of operation and examples of TDI applications. In Section 3, we describe aspects to be considered in the design of a high-resolution, high-performance TDI-CCD imager. Aspects of device design specific to the TDI mode of operation are highlighted. General CCD device design issues are not discussed unless they pertain to the TDI mode of operation. In Section 4, we compare the TDI-CCD imager to the photodiode linear array imager; both require mechanical scanning and, in general, compete for the same applications. In Section 5, we present a design case study of a family of TDI-CCD imagers targeted for use in scanning documents, bank checks, and museum art objects.

2. TDI mode of operation

• *Principles of operation*

The principles of time-delay and integration are illustrated schematically in **Figure 1**. The TDI-CCD imager is basically an area imaging array, typically with its length (number of columns) significantly larger than its height (number of rows). Scanning along its length is accomplished electronically by its CCD serial register, and a two-dimensional image is obtained by mechanically scanning the TDI-CCD imager with respect to the image plane.

Consider a time t_i at which the image of line$_j$ of the object to be imaged is focused onto the first row of the array. Signal charges corresponding to the light intensity of line$_j$ are collected in the first row during the line-scan time. At time t_{i+1}, the image of line$_j$ is moved (via mechanical scanning) to the second row, generating signal charges at the second row corresponding to the light intensity of line$_j$. These signal charges are added to (integrated with) the signal charges due to the same line$_j$ of the image (collected during time t_i) being clocked down from the first row. At the same time, the image of line$_{j+1}$ is focused onto the first row. This operation continues until the signal charges due to line$_j$ are clocked to the serial register; the signal of line$_j$ is then quickly shifted out (within one line-scan time) to the output amplifier. For an N-stage TDI-CCD imager, the signal charges collected by the time the signal is clocked to the serial register are due to N times the exposure time in one line-scan time. The sensitivity of the imager is therefore N times that of the same imager with only a single stage, using the same line-scan time.

• *Examples of implementation*

The principles of time delay (shift) and integrate (add), which were first described by Gudmundsen [4] and Texas Instruments [5], have been employed in a variety of applications. TDI has been employed for visible imaging with CCDs [3, 6–35], infrared imaging with CCDs and CIDs [36–50], X-ray and uv imaging with an intensifier [51–54], and some nonimaging applications such as parallel optical signal processing for synthetic aperture radar [55–58] and sonar beam steering [59, 60]. For visible imaging, the TDI-CCD imager was initially used in airborne and tactical reconnaissance [17, 18, 20, 23, 25, 32] and satellite imaging [3, 19, 22, 52]; it was subsequently used in astronomy [27], and, more recently, in document scanning [6–14].

The relative motion between the image and the imager can be achieved in many ways. For example, in airborne reconnaissance, the TDI-CCD imager is carried on board, and the motion of the airplane with respect to the ground image provides the along-track scanning motion [20, 22, 25]; in astronomy applications, the TDI-CCD imager is mounted on the focal plane of an earth-stationed telescope, and the motion of the earth with respect to the stars provides the TDI scanning motion [27]; in document scanning, using a flatbed scanner or camera-type scanning configuration, the TDI-CCD imager is moved in the image plane with a stepping motor to provide the relative motion [6–9]; in scanning such as high-speed bank check scanning, the object to be imaged is transported past a stationary TDI-CCD imager [6, 7].

• *Advantages of TDI*

The long-recognized merits of the TDI mode of operation for imaging include the following:

- Enhanced photosensitivity without sacrificing output data rate. This translates into a high scan speed and/or the ability to image at low light levels.
- Increased signal-to-noise ratio. This permits very low-contrast imaging and provides greater detail in the low-light areas of an image.
- Improved sensitivity uniformity of the pixels as a result of averaging of the sensitivity of many pixels in the TDI column.
- Improved dark-current uniformity of the pixels as a result of averaging of the dark current of many pixels in the TDI column.
- Ability to perform electronic exposure control.

We discuss the factors affecting these aspects of the TDI mode of operation in later sections.

3. Device design

We concentrate on the device design issues of monolithic silicon TDI-CCD imagers for visible imaging. Chamberlain and Washkurak [14] have discussed this in a recent paper. Here, we expand on that paper. The architecture of the TDI-CCD imager (see **Figure 2**) is essentially the same as that of the full-frame-transfer area CCD imager, and the usual design considerations regarding the latter apply to it as well. In the following sections, we address only those device design issues which are specific to the use of the TDI-CCD imager for visible imaging applications. In particular, the examples discussed are drawn from device design considerations applied to the scanning of documents and museum art objects.

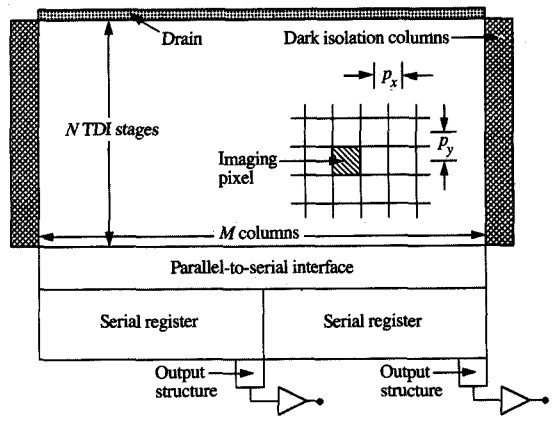


Figure 2

Schematic illustration of the device architecture of a TDI-CCD imager.

- *Parallel array*

The parallel array is the imaging area of the TDI-CCD imager. The photosensitive elements are CCD MOS photogates; photocharges are collected in the potential wells of the parallel CCD array. Hence, the charge capacity of the CCDs in the array should be maximized while at the same time a reasonable pixel size should be maintained (see later discussion) to limit the total length of the imager. Surface-channel CCDs provide a larger charge capacity than buried-channel CCDs. They are inferior to the latter in terms of transfer speed, transfer efficiency, and noise associated with the presence of surface states. The number of transfers in the TDI direction is generally quite small compared to that typically found in CCDs. Also, the transfer speed required of the parallel array is orders of magnitude lower than that required of the CCDs in the serial register. Thus, the disadvantages in using the surface-channel CCD can sometimes be traded off for its higher charge capacity, depending on the application.

The layout of the TDI-CCD imager is usually characterized by a very high aspect ratio, with the number of columns of pixels much larger than the number of TDI stages. The total length of the polysilicon gate electrode of the parallel array is approximately Mp_x, where M is the number of pixels in the horizontal direction (i.e., the number of TDI columns) and p_x is the center-to-center distance between pixels in the horizontal direction (x-direction). This long polysilicon gate electrode may be modeled as a distributed RC transmission line. For a step voltage applied at one end of the transmission line, the time required for its output voltage to rise from zero to 90% of its final value is RC [61–63], where the resistance R and the capacitance C of the electrode are given by

$$R \simeq R_s \frac{L_{\text{electrode}}}{W_{\text{electrode}}}, \tag{1}$$

$$C \simeq C_{\text{area}}(L_{\text{electrode}} W_{\text{electrode}}) + C_{\text{perimeter}} L_{\text{electrode}}, \tag{2}$$

where $L_{\text{electrode}}$ and $W_{\text{electrode}}$ are the total length and width, respectively, of the distributed RC line; R_s is the sheet resistance (in units of $\Omega/\square$), C_{area} is the areal component of the electrode capacitance (in units of F/cm^2); and $C_{\text{perimeter}}$ is the component of the electrode capacitance (in units of F/cm) that depends on the perimeter of both edges of the electrode (e.g., fringing field capacitance). Note that both C_{area} and $C_{\text{perimeter}}$ are determined by the three-dimensional geometries of the electrodes. For example, the polysilicon gate electrodes cross over the field isolations as well as the gate oxide regions; in that regard, it should be noted that the presence of such overlap complicates associated capacitance calculations. Assuming that the polysilicon gate electrodes

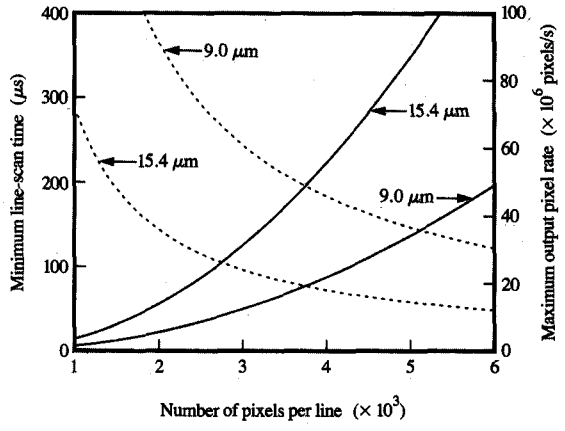


Figure 3

Minimum line-scan time (solid lines) and maximum output pixel rate (dashed lines), calculated as a function of the number of pixels per line, for pixel sizes of 15.4 μm × 15.4 μm and 9.0 μm × 9.0 μm.

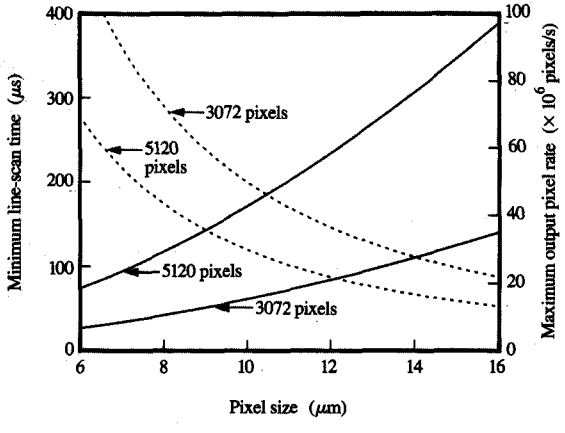


Figure 4

Minimum line-scan time (solid lines) and maximum output pixel rate (dotted lines), calculated as a function of pixel size, for TDI-CCD imagers containing 3072 and 5120 pixels per line.

of the parallel array are driven by clock drivers at both ends of the electrode, it follows that $L_{\text{electrode}} \simeq Mp_x/2$.

The minimum line-scan time, $t_{\text{line-scan}}$ (the time required to scan one line), may be approximated by the number of clock transition times per TDI stage transfer (N_{clock}) times the clock transition time at the location farthest from the clock drive points. The clocking method used determines the value of N_{clock}. Examples of clocking methods are discussed later. For example, a four-phase overlapping double clock with eight moves per stage has eight clock transitions per TDI stage transfer.

For simplicity, we assume that all of the polysilicon levels have the same width and that there is no electrode overlap. This assumption is not correct for realistic electrode configurations, since electrode overlap is required. Because design ground rules usually require the use of different spacings and widths for the various polysilicon layers, the widths of the electrodes are not identical for each phase. Thus, $W_{\text{electrode}} = p_y/N_{\text{electrode}}$, where p_y is the center-to-center distance between pixels in the y-direction (TDI direction) and $N_{\text{electrode}}$ is the number of phase electrodes per TDI stage. The minimum line-scan time is then

$$t_{\text{line-scan}} = N_{\text{clock}} R_s \left(C_{\text{area}} + \frac{C_{\text{perimeter}}}{p_y/N_{\text{elelectrode}}} \right) \left(\frac{Mp_x}{2} \right)^2, \quad (3)$$

which increases with the square of the number of pixels per line. The output pixel rate is $M/t_{\text{line-scan}}$ and varies with $1/M$. **Figure 3** illustrates the minimum line-scan time and maximum output pixel rate for a four-phase overlapping double-clocked TDI-CCD imager fabricated with a 2-μm minimum-linewidth process (15.4-μm × 15.4-μm pixel size) and a 1-μm minimum-linewidth process (9.0-μm × 9.0-μm pixel size) as a function of the number of pixels per line. With decreasing pixel size, the perimeter component of the electrode capacitance (which is due mainly to fringing field capacitance) does not scale in the same manner as the areal component [64]. **Figure 4** illustrates the calculated minimum line-scan time and maximum output pixel rate as a function of pixel size, for 3072-element and 5120-element TDI-CCD imagers.

The RC delay of the parallel clock imposes the lower limit on the minimum line-scan time, since the data rate of the serial register can in principle be kept within the capability of the serial CCDs by increasing the number of output ports. To increase the parallel clock speed, the polysilicon gate electrodes of the parallel array can, for example, be driven by clock drivers at intermediate lengths, which necessitates placing metal-to-polysilicon contacts in the imaging area [65].

- *Parallel-to-serial interface*

At the end of the column, the parallel array terminates in one or more serial registers. The clocked charges undergo a 90° turn as they are transferred from the parallel array to the serial register. Care must be exercised in designing the parallel-to-serial interface to avoid potential barriers and troughs at the corners [12, 66]. This problem is common to

all CCD architectures (e.g., frame-transfer area CCDs) which require a parallel-to-serial interface.

• *Serial register*

The serial register of a high-resolution TDI-CCD imager is typically fairly long because the resolution of the imager is directly proportional to the number of columns in the TDI-CCD imager. This long serial register places such a stringent requirement on the transfer efficiency and transfer speed of the CCDs that use of the buried-channel CCD is required to achieve reasonable performances. For example, in the case of a four-phase CCD, in order to maintain a transfer efficiency of 0.94 in the worst case for a 1536-stage serial register, a transfer efficiency of 0.99999 is required. For a TDI-CCD imager with a large number of pixels per line, the serial register is either multiplexed into two to four horizontal serial registers [30, 67] or sectioned with in-line output taps [30]. This is needed to reduce the number of transfers and to increase the effective output data rate. Employing multiple output ports in the serial register requires that the gain and offset of the different output ports be equalized, and requires extra care in implementation. The tapped serial register requires that the final stage of each serial register section fit in-line within the cell size of the electrodes [11, 68]; this limits the choice of output structures available. Another problem with the tapped serial register, which is less frequently discussed, is the power dissipation of the output amplifier. The output amplifier, which usually consists of one or more source-follower amplifiers, constantly dissipates power and results in local heating of the silicon chip. Since the dark current is exponentially dependent on the temperature [69–72], a small variation in the temperature profile in the chip is easily detected as a dark-current profile.

Figure 5 shows the dark-current profile of a center-tapped 3072 × 32-stage TDI-CCD imager. The output is tapped at the center and the right-hand end of the serial register. The dark current rises near the center and the right-hand side of the serial register, where the output structures are located. During operation (at an ambient temperature of 42°C) inside an air-tight, light-tight, scanning camera, the temperature rise contributes to a peak dark-current deviation of about 17.5% at the "hot" end compared to the dark current at the "cool" end; the rise in temperature from the "cool" end to the "hot" end is about 1.2°C. The tail of the dark-current distribution for that TDI-CCD imager is about 500 pixels (7.7 mm). It is possible that part of the nonuniform dark-current profile is due to hot-carrier-induced photon emission from the MOSFETs of the output amplifier [73]. For high-quality scanning applications, pixel-by-pixel dark-current subtraction in a line is therefore necessary to achieve high performance.

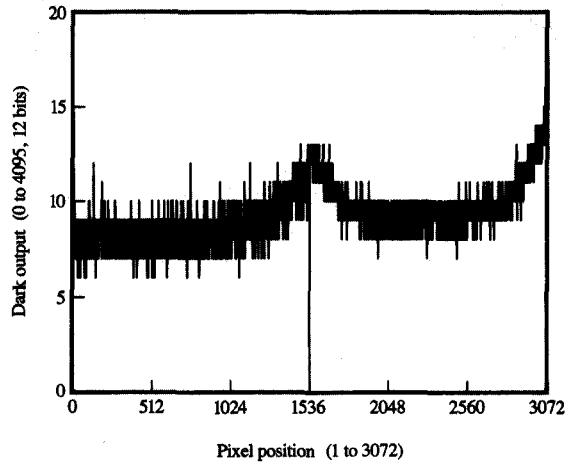


Figure 5

Dark-current profile at 25°C of a center-tapped 3072 × 32-stage TDI-CCD imager. The output structures are located at pixel number 1536 (center) and 3072 (right-hand side). Note the rise of dark current toward the vicinity of the output structure. The dark current has been digitized to 12 bits (4096 levels).

• *Resolution, modulation transfer function (MTF), and clocking*

Charge-coupled device imagers are sampled data imagers. The effective sampling aperture of the photosensitive element plays an important role in determining the resolution of the imager. A measure of the resolution of an imager is the modulation transfer function (MTF) [74–77], which is the magnitude of the optical transfer function (OTF). A simple method to derive the one-dimensional OTF of a photodetector is to consider the one-dimensional Fourier transform $S(f)$ of the spread function $s(x)$ of the detector effective sampling aperture L centered at (x_0, y_0) [78], namely

$$S(f) = \int_{-\infty}^{\infty} s(x) e^{j2\pi fx}\, dx, \tag{4}$$

where f is the spatial frequency, and the spread function $s(x)$ is defined as

$$\begin{aligned} s(x) &= s_0, \quad \text{a constant, for } x_0 - L/2 \le x \le x_0 + L/2 \\ &= 0 \quad \text{for all other } x. \end{aligned} \tag{5}$$

The MTF is then given by

$$MTF(f) = \frac{|S(f)|}{|S(f=0)|}. \tag{6}$$

Substituting (5) into (4), we obtain

$$S(f) = s_o \int_{x_o - L/2}^{x_o + L/2} e^{j2\pi fx}\, dx$$

$$= s_o e^{j2\pi f x_o} \frac{\sin(\pi f L)}{\pi f}. \quad (7)$$

The MTF is then obtained by substituting (7) into (6), giving

$$MTF(f) = \frac{\sin(\pi f L)}{\pi f L}. \quad (8)$$

Note that L is the effective sampling aperture of the photodetector. The Nyquist frequency (f_N) of the imager is determined by the center-to-center spacing (p) of the sampling photo-aperture, namely

$$f_N = \frac{1}{2p}. \quad (9)$$

The MTF can therefore be expressed (excluding the case of ripple clocking; see discussion later) as

$$MTF(f) = \frac{\sin\left(\frac{\pi}{2}\frac{f}{f_N}\frac{L}{p}\right)}{\frac{\pi}{2}\frac{f}{f_N}\frac{L}{p}}. \quad (10)$$

The modulation transfer function of the imager system is the product of all the modulation transfer functions associated with all possible sources [1]. We now discuss the modulation transfer function of the TDI-CCD imager associated with various relevant sources.

An infinitely small sampling aperture ($L \to 0$) should have an MTF equal to unity at all frequencies. For a TDI-CCD imager with center-to-center pixel spacings p_x, p_y, and pixel apertures L_x, L_y, in the x- and y-directions, respectively, the MTF associated with the use of a finite aperture [$MTF_{\text{aperture}}(f)$] is obtained by substituting p_x and p_y, respectively, for p and substituting L_x and L_y, respectively, for L into (10). Thus,

$$MTF_{\text{aperture},x}(f) = \frac{\sin(\pi f L_x)}{\pi f L_x} = \frac{\sin\left(\frac{\pi}{2}\frac{f}{f_N}\frac{L_x}{p_x}\right)}{\frac{\pi}{2}\frac{f}{f_N}\frac{L_x}{p_x}}, \quad (11)$$

and

$$MTF_{\text{aperture},y}(f) = \frac{\sin(\pi f L_y)}{\pi f L_y} = \frac{\sin\left(\frac{\pi}{2}\frac{f}{f_N}\frac{L_y}{p_y}\right)}{\frac{\pi}{2}\frac{f}{f_N}\frac{L_y}{p_y}}. \quad (12)$$

Since the TDI-CCD imager is not a staring imager, the relative motion between the imaging aperture and the image of the focal plane results in an increase in the effective aperture.

Several important sources of degradation in the modulation transfer function that apply specifically to the TDI mode of operation [1] are

- Mismatch between the velocity of the scanned image and the velocity of the signal charge being clocked in the TDI direction.
- Discrete charge motion in the TDI direction.
- Angular misalignment of the columns of the imaging device to the direction of the mechanical scan [53, 79].

When there is a velocity mismatch between the average velocity of the signal charge in the TDI direction and the velocity of the mechanical scan, after a distance of N stages of TDI, the sampling aperture is displaced from its intended position by $Np_y\Delta V/V$, where ΔV is the difference in average velocity between the charge packet and the mechanical scan, and V is the average velocity of the mechanical scan. This causes an increase in the effective sampling aperture and results in an MTF that can be calculated by substituting $Np_y\Delta V/V$ for L in (8), namely,

$$MTF_{\text{velocity}}(f) = \frac{\sin\left(\pi f \frac{Np_y\Delta V}{V}\right)}{\pi f \frac{Np_y\Delta V}{V}} = \frac{\sin\left(\frac{\pi}{2}\frac{f}{f_N}\frac{N\Delta V}{V}\right)}{\frac{\pi}{2}\frac{f}{f_N}\frac{N\Delta V}{V}}. \quad (13)$$

Figure 6 contains curves obtained from (13) for several values of $N\Delta V/V$.

One of the unique aspects of the TDI mode of operation is that the signal charge in the imaging array is moved in *discrete* steps, whereas the mechanical scanning can be almost linear or proceed in discrete steps, depending on the method used for achieving mechanical displacement. This results in a mode in which the signal charge is always either lagging behind the image or is ahead of the image by a subpixel amount and is never in total synchrony with the optical image—namely, in a mode in which the signal charge moves in a "jerky" motion [30], while the scanned optical image moves almost linearly or in discrete steps with step sizes different from those of the charge packet motion. This discrete motion of the charge causes misregistration between the image and the imaging potential wells, and results in a degradation of the MTF in the mechanical scanning (along-track) TDI direction.

In order to calculate the degradation in the MTF due to discrete charge motion, we consider 1) a pattern of charge movement which is dependent on the clocking method for the imaging parallel array and 2) mechanical scanning motion. Illustratively, we assume use of a linear

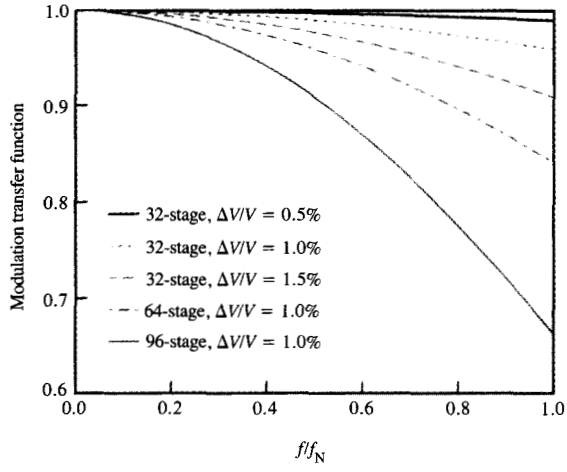


Figure 6

Calculated modulation transfer function associated with a mismatch between the velocity of the mechanically scanned motion and the average velocity of the clocked charge motion.

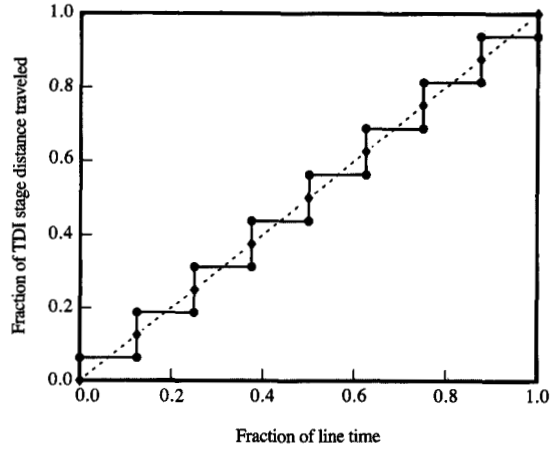


Figure 7

Schematic illustration of the discrete nature of clocked charge motion (solid line) compared to linearly scanned image motion (dashed line).

mechanical scanning motion. Clock patterns commonly employed for the TDI-CCD imager can be found in [12, 14, 28–30, 33, 34]. **Figure 7** illustrates, for the case of a four-phase, overlapping double clock, how the discrete movement of the signal charge due to clocking constantly falls behind the linear movement of the scanned image, but nevertheless has the same *average velocity* as the mechanically scanned image. The motion of the charge packet for a four-phase overlapping double clock is actually more complicated than depicted. At various times, the charge packet is held under two or three electrodes. Thus, the size of the charge packet is variable, and the movement of the centroid of the charge packet is more complex than depicted. The effective sampling aperture due to this discrete charge motion is given by the distance covered by one "move" of the charge packet. For example, for the four-phase overlapping double-clocking example of Figure 7, there are eight "moves" per TDI stage. Thus, the effective sampling aperture due to discrete charge motion is $p/8$. Substituting this effective sampling aperture into L of (8) gives the MTF associated with discrete charge motion [$MTF_{\text{discrete}}(f)$]. **Table 1** lists the effective apertures and $MTF_{\text{discrete}}(f_N)$ at the Nyquist frequency for several common clock patterns.

Figure 8 shows the calculated modulation transfer function in the TDI direction that is associated with the discrete charge motion, for various clocking methods. Essentially, the greater the number of moves per stage, the smoother the motion of the signal charge, and thus the less degradation in the MTF because of discrete charge motion. Four-phase clocking with eight moves per stage results in the highest MTF.

Table 1 Calculated values of $MTF_{\text{discrete}}(f_N)$ for several common clock patterns, where p is the center-to-center spacing of the sampling aperture. For the case of ripple clocks, p is the length of a phase electrode. Linear mechanical scan motion is assumed.

Clock pattern	*Effective aperture L*	$MTF_{\text{discrete}}(f_N)$
Two-phase, overlapping or nonoverlapping clock (two moves)	$p/2$	0.900
Three-phase, nonoverlapping clock (three moves)	$p/3$	0.955
Three-phase, overlapping clock (six moves)	$p/6$	0.989
Four-phase, nonoverlapping clock (four moves)	$p/4$	0.974
Four-phase, overlapping clock (eight moves)	$p/8$	0.994
Four-phase, ripple clock	$4p/3$	0.413
Eight-phase, ripple clock	$8p/7$	0.543

The effect of the clocking method on the vertical resolution of the TDI-CCD imager is best illustrated with a hypothetical example which takes into account MTF_{discrete}

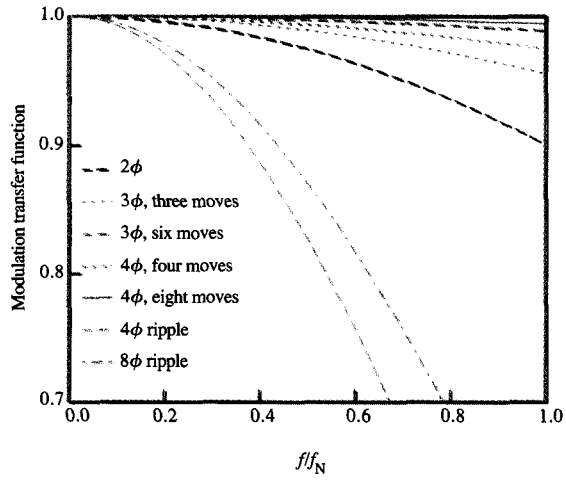


Figure 8

Calculated modulation transfer function in the TDI direction, associated with the discrete nature of the clocked charge motion.

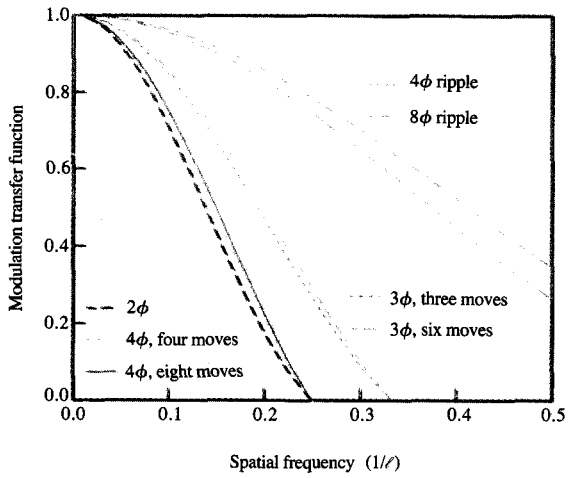


Figure 9

Comparison of calculated modulation transfer function for a hypothetical TDI-CCD imager fabricated with a minimum gate-electrode length of ℓ, assuming the use of the indicated clocking methods.

and MTF_{aperture}. We assume that the minimum center-to-center spacing of each electrode is ℓ. **Table 2** lists the TDI stage length, the effective sampling aperture due to use of a finite pixel size, and the effective sampling aperture due to discrete charge motion, for various clock patterns. Note that a ρ-phase ripple clock stores $(\rho - 1)$ distinct charge packets in ρ electrodes; thus, an N-stage TDI-CCD imager employing ripple clocking contains $N\rho/(\rho - 1)$ pairs of electrodes. **Figure 9** shows the MTF calculated for a hypothetical TDI-CCD imager fabricated with a minimum gate-electrode length of ℓ, using several clocking modes. For a direct comparison, the spatial frequency is shown normalized to the inverse minimum electrode length $1/\ell$, instead of Nyquist frequency, since the use of different clocking methods here results in different Nyquist frequencies.

The charges of TDI imagers that have a small pixel pitch and pixel aperture (hence larger MTF_{aperture}) move forward by a larger fraction of the pixel pitch in one "move" (resulting in a smaller MTF_{discrete}). Although ripple clocking reduces the aperture of the imaging pixel in the vertical direction, the MTF degradation due to discrete charge motion for ripple clocking is quite severe. Thus, the advantages of ripple clocking may not be as large as they appear when we consider only the MTF due to the finite pixel aperture. Furthermore, there are other considerations for ripple clocks, such as maximum parallel clock speed, which must be taken into account.

Velocity mismatch and discrete charge motion cause MTF degradation in the vertical (TDI) direction. MTF degradation in the horizontal direction (x-direction) occurs if the TDI columns are not aligned perfectly with the mechanical scan direction [53, 79]. If the TDI columns subtend an angle θ with respect to the mechanical scan direction, the sampling aperture will have moved a distance of $Np_y \tan\theta$ with respect to the image on the focal plane by the time the charge packet from the top of the TDI column reaches the bottom of the column [79]. The effective sampling aperture for this situation is $Np_y \tan\theta$ (in the x-direction). Thus, the MTF due to angular misalignment is

$$MTF_{\text{alignment}}(f) = \frac{\sin(\pi f N p_y \tan\theta)}{\pi f N p_y \tan\theta} = \frac{\sin\left(\frac{\pi}{2}\frac{f}{f_N} N \tan\theta\right)}{\frac{\pi}{2}\frac{f}{f_N} N \tan\theta}. \quad (14)$$

Figure 10 shows the calculated MTF due to angular misalignment for various numbers of TDI stages. For TDI-CCD imagers with a large number of TDI stages, the placement accuracy of the chip on the package is very important. For example, a misalignment of 0.2° for a 96-stage TDI will decrease the MTF at the Nyquist frequency by 0.954.

Finally, the MTF associated with transfer inefficiency has been discussed by Barbe [1]. The gain and phase shift

due to transfer inefficiency in the x-direction are, respectively,

$$G_{N_{\text{transfer}}} = \exp\{-\varepsilon N_{\text{transfer}}[1 - \cos(2\pi f p_x)]\}, \quad (15)$$

$$\Delta\phi_{N_{\text{transfer}}} = \varepsilon N_{\text{transfer}} \sin(2\pi f p_x). \quad (16)$$

The MTF loss due to transfer inefficiency in the y-direction is

$$MTF_{\text{transfer},y} = \frac{1}{M(a^2 + b^2)}(c^2 + d^2)^{0.5}, \quad (17)$$

where

$$c^2 = \{a - \exp(-Ma)[a\cos(Mb) - b\sin(Mb)]\}^2, \quad (18)$$

$$d^2 = \{b - \exp(-Ma)[a\sin(Mb) + b\cos(Mb)]\}^2, \quad (19)$$

$$a = \varepsilon[1 - \cos(\pi f/f_N)], \quad (20)$$

and

$$b = \varepsilon \sin(\pi f/f_N). \quad (21)$$

In summary, the total MTF for a TDI-CCD imager is

$$MTF_y = MTF_{\text{aperture},y} MTF_{\text{velocity}} MTF_{\text{discrete}} MTF_{\text{transfer},y}, \quad (22)$$

$$MTF_x = MTF_{\text{aperture},x} MTF_{\text{alignment}} MTF_{\text{transfer},x}. \quad (23)$$

The use of three-phase clocks with triple polysilicon gates results in more compact cell layouts. Two-phase clocks are simpler to operate, but have smaller charge capacities than four-phase clocks.

The choice of clocking method also depends on the fabrication process used (for example, use of a double or triple polysilicon gate process), and the application. The clocking method considerations pertain mainly to the clocking of the parallel array, since the parallel array is the imaging area, and the clocking method chosen has a direct effect on the charge capacity, photosite aperture, and signal charge motion.

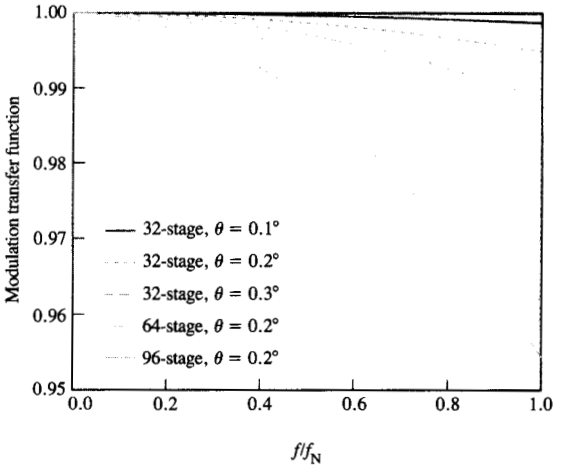


Figure 10

Calculated modulation transfer function associated with angular misalignment between the TDI column and the direction of mechanically scanned motion, for TDI-CCD imagers having differing numbers of TDI stages and misalignments.

• *Number of TDI stages, sensitivity, and exposure control*
In the TDI mode of operation with N TDI stages, the image is "seen" by the imaging array N times as the signal charge is clocked from the top of the parallel array to the serial register. Thus, the exposure time of an image for an N-stage TDI is N times that of a single-stage CCD, and

Table 2 Calculated values of some TDI parameters for various clock patterns. The values are used for calculating the modulation transfer function. The minimum gate electrode length is designated as ℓ.

Clock patterns	*Nyquist frequency* (f_N)	*Effective sampling aperture due to use of a finite pixel size* (L_{aperture})	*Effective sampling aperture due to discrete charge motion* (L_{discrete})
Two-phase, four electrodes, overlapping or nonoverlapping clock (two moves)	$1/(8\ell)$	4ℓ	$4\ell/2$
Three-phase, three electrodes, nonoverlapping clock (three moves)	$1/(6\ell)$	3ℓ	$3\ell/3$
Three-phase, three electrodes, overlapping clock (six moves)	$1/(6\ell)$	3ℓ	$3\ell/6$
Four-phase, four electrodes, nonoverlapping clock (four moves)	$1/(8\ell)$	4ℓ	$4\ell/4$
Four-phase, four electrodes, overlapping clock (eight moves)	$1/(8\ell)$	4ℓ	$4\ell/8$
Four-phase, eight electrodes, ripple clock	$1/(2\ell)$	ℓ	$4\ell/3$
Eight-phase, sixteen electrodes, ripple clock	$1/(2\ell)$	ℓ	$8\ell/7$

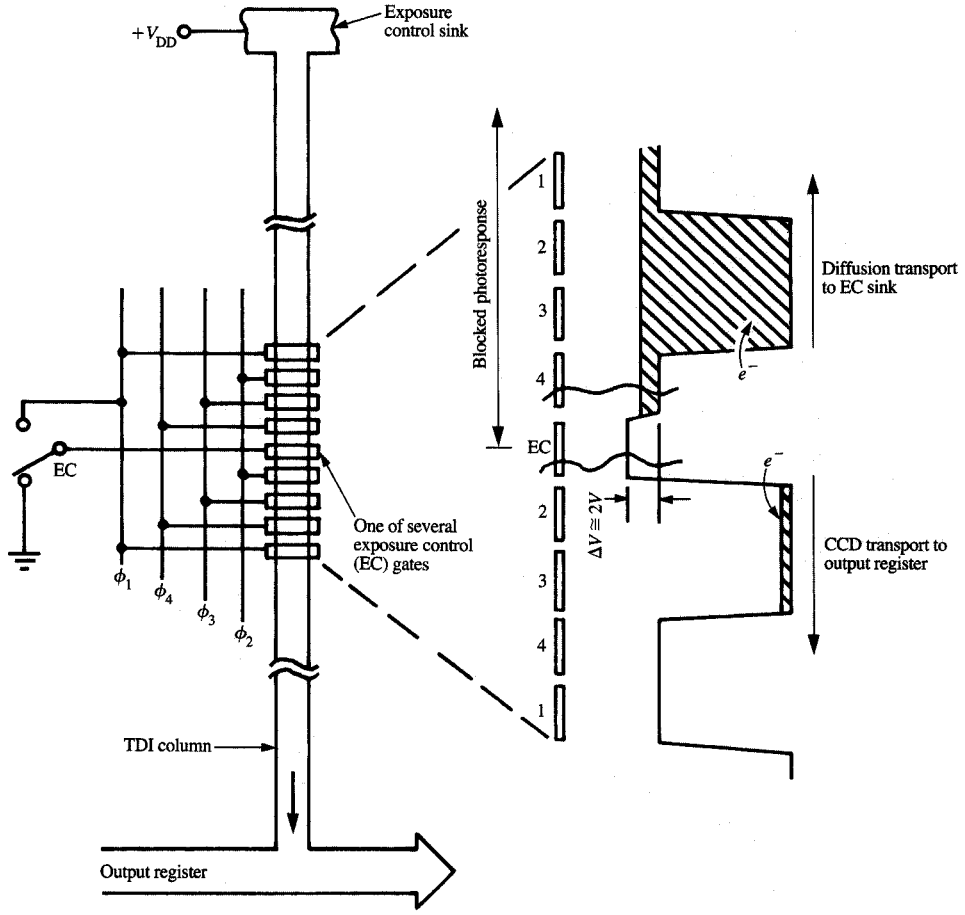


Figure 11

Electronic exposure control for a TDI-CCD imager. From [33], © 1980 IEEE, reproduced with permission.

the scanning responsivity of the CCD is thereby increased N times. It is possible to achieve on-chip electronic exposure control using TDI [3, 26, 29, 31, 33, 80] by reducing the number of TDI stages. **Figure 11** shows the electronic exposure control system of Farrier and Dyck [33]. In their system, use is made of a four-phase clock, and the exposure control (EC) electrode is the phase 1 electrode. When this EC electrode is connected to the phase 1 clock, normal TDI operation takes place. When it is grounded while the rest of the four-phase clocks are clocked between V_1 and V_2 ($V_2 > V_1 > 0$), a potential barrier is established at the EC electrode which blocks charge transfer beyond the EC gate. The pool of signal charge between the top of the TDI column and the EC electrode (which accumulates toward the EC electrode by clocked charge transfer) is ultimately removed from the imaging area by diffusive transport over the normal clock potential barriers back to the n^+ sink diode at the top of the TDI column.

While electronic exposure control can increase the dynamic range of the imager, it is not without its disadvantages [80]. For a given clock voltage range (dictated by the fabrication process used), the voltage barrier required for the EC electrode reduces the normal clock voltage range from V_2 to $(V_2 - V_1)$; hence, the charge capacity is reduced. Furthermore, the diffusive transport of unused signal charge requires a charge concentration profile which is high at the EC electrode and low at the n^+ sink diode. The magnitude of this diffusion current determines the saturation level of the imaging light flux. This limitation can be removed by clocking the unused part of the TDI stages in reverse, which

necessitates the use of separate clock lines for the unused part of the TDI imaging array.

For applications in which the ambient light is not controlled (such as airborne reconnaissance), electronic exposure control is useful. For other applications (such as in document scanning), where the light source is a system design parameter, electronic exposure control may not be important, since exposure can be adjusted by properly designing the light source of the scanner.

• *Noise, dynamic range, and signal-to-noise ratio*

Noise is a very important consideration in the design of solid-state imagers. There have been many excellent theoretical and experimental papers in the literature [81–87] on the subject of noise in CCDs in general. The issue of noise and dynamic range of the TDI-CCD imager has recently been discussed by Chamberlain and Washkurak [14]. Although we do not cover the details of noise analyses for the CCD, we do, however, list the relevant equations and highlight some considerations that are specific to the design of TDI-CCD imagers for document and museum art object scanning applications.

The noise of the TDI-CCD imager arises from the parallel imaging array, the serial shift register, and the output structures.

In the parallel array, the major noise sources are

- Interface state trapping noise (for surface-channel CCD only).
- Bulk trapping noise (for buried-channel CCD only).
- Dark-current shot noise.
- Transfer inefficiency shot noise.
- Photon shot noise.

In the serial register, the major noise sources are

- Interface state trapping noise (for surface-channel CCD only).
- Bulk trapping noise (for buried-channel CCD only).
- Dark-current shot noise.
- Transfer inefficiency shot noise.

In the output structures, the major noise sources are

- Reset noise.
- Output source-follower thermal noise.
- Output source-follower $1/f$ noise.
- A/D conversion quantization noise.

The expressions relating the rms noise to the device physical parameters are listed below without derivation. We refer the reader to the original literature for their derivations. **Table 3** lists the terminology employed and the values of the parameters for a 3072 × 32-stage TDI-CCD imager (TDI-4) described in Section 5.

The expression obtained for the noise due to trapping of carriers by interface states [81] is

$$\overline{(N_{\text{interface trap}})^2} = 2 \ln (2) kTN_{\text{ss}} N_{\text{transfer}} A_{\text{gate}} . \quad (24)$$

This noise is insignificant in buried-channel CCDs.

The noise due to bulk traps [83, 85] consists of a filling noise and an emptying noise due to variance of the emission of trapped carriers in the bulk traps. The capture time for carriers by bulk traps is very short compared to normal clock periods; the bulk traps are effectively filled instantaneously by carrier capture. Thus, there is no variance during the portion of a cycle during which they are filled [83, 85].

The expression obtained for the noise due to the filling and emptying of bulk traps is [83, 85]

$$\overline{(N_{\text{bulk trap,empty}})^2} = N_{\text{transfer}} V_{\text{SIG}} \sum_i N_i^t \exp\left(-\frac{T_t}{\tau_i}\right)\left[1 - \exp\left(-\frac{T_t}{\tau_i}\right)\right], \quad (25)$$

$$\overline{(N_{\text{bulk trap,fill}})^2} = N_{\text{transfer}} V_{\text{SIG}} \sum_i N_i^t \exp\left(-\frac{N_Z T_c + T_t}{\tau_i}\right)\left[1 - \exp\left(-\frac{N_Z t_c + t_t}{\tau_i}\right)\right], \quad (26)$$

where N_Z is the number of zeros before a one, t_t is the transfer time, T_c is the clock period, N_i^t is the volume density of the ith bulk trap with emission time τ_i, and V_{SIG} is the volume in the bulk with which the signal charge interacts. Note that the bulk trap filling noise is dependent on the number of preceding zeros; it also depends on the size of the charge packet, because as the charge packet size changes, the volume of the silicon bulk trap it interacts with varies. The transfer time t_t is a function of the clock waveform [85]. This bulk trapping noise is present only for buried-channel CCDs. For surface-channel CCDs, it is not significant, because the charge packet essentially resides at the surface inversion layer, and the bulk volume with which it interacts is small.

The dark charge collected during the integration time and during transit from the imaging array to the output structure is characterized by a Poisson distribution, and is a shot noise. The variance of the dark charge is thus equal to the mean of the dark charge collected [81, 88], namely

$$\overline{(N_{\text{dark},\tau})^2} = J_D A_{\text{coll}} \tau_{\text{coll}} / q, \quad (27)$$

where the collection area (A_{coll}) is the effective area under which the dark charge is collected; τ_{coll} is the total collection time of the dark charge ($\tau_{\text{coll}} = t_{\text{line}} N_{\text{stage}}$ for

Table 3 Terminologies and values of parameters for the 3072 × 32-stage TDI-4 imager of Section 5.

Symbol	*Units*	*Definition*	*3027 × 32-stage imager TDI-4 of Section 5*
$\overline{(N_{source})^2}$	dimensionless	Mean square number of noise electrons for a noise source	
$\sqrt{\overline{(N_{source})^2}}$	dimensionless	Root mean square number of noise electrons for a noise source	
N_{phase}	dimensionless	Number of clocking phase	4 (parallel and serial)
$N_{transfer}$	dimensionless	Number of transfers	
L_x	cm	Length of CCD cell in the x-direction	15.4×10^{-4} (parallel), 15.4×10^{-4} (serial)
L_y	cm	Length of CCD cell in the y-direction	15.4×10^{-4} (parallel), 62.0×10^{-4} (serial)
A_{gate}	cm^2	Area of one CCD gate electrode	5.93×10^{-7} (parallel), 2.39×10^{-6} (serial)
A_{pixel}	cm^2	Area of one CCD cell	2.37×10^{-6} (parallel), 9.55×10^{-6} (serial)
A_{coll}	cm^2	Dark-current collection area	1.19×10^{-6} (parallel), 4.77×10^{-6} (serial)
N_{ss}	$cm^{-2}\ eV^{-1}$	Interface states density (average over relevant energy ranges)	5×10^{10}
kT	eV	Thermal voltage	0.02585
N_{signal}(full)	dimensionless	Number of electrons at saturation (full well)	3.75×10^6
t_{line}	s	Line-scan time	6.2×10^{-3}
N_{stage}	dimensionless	Number of TDI stages	32
M_{stage}	dimensionless	Number of serial register stages	1536 (two ports)
ε	dimensionless	Transfer inefficiency	10^{-4} (parallel), 10^{-5} (serial)
J_D	$A\ cm^{-2}$	Dark-current density	10^{-9}
t_c	s	Serial register clock period	4×10^{-6}
C_o	F	Total capacitance at the floating diffusion output node	0.57×10^{-12}
C_{gate}	$F\ cm^{-2}$	Gate capacitance per unit area of the source-follower input transistor	7.67×10^{-8}
g_m	S	Transconductance of input transistor of the source-follower amplifier	7.32×10^{-3}
W	cm	Gate width of input transistor of the source-follower amplifier	218×10^{-4}
L	cm	Gate length of input transistor of the source-follower amplifier	3.6×10^{-4}
b	bits	Number of quantization bits of the A/D converter	12
S	A/W	Photosensitivity	186×10^{-3}

parallel array, and $\tau_{coll} = t_c M_{stage}$ for the serial register). The expression obtained for the dark current (using standard terminology [69–72]), is

$$I_{dark} = \frac{qn_i W_g A_{bulk}}{\tau_{gr}} + qn_i s A_{surface} + \left(\frac{qn_i^2}{N_B}\right)\left(\sqrt{\frac{D_p}{\tau_{po}}}\right) A_{bulk}, \quad (28)$$

The generation of electron–hole pairs by photons is a process characterized by a Poisson distribution, and the photon shot noise can be expressed [81, 88] as

$$\overline{(N_{h\nu})^2} = N_{\text{signal}} = SA_{\text{pixel}} H\tau/q, \tag{29}$$

where H is the irradiance and τ is the exposure time. The rms photon shot noise increases as the square root of the mean signal. For any CCD imager, the photocarrier generation sets the limit for the maximum attainable signal-to-noise ratio at the saturation signal level.

The transfer inefficiency introduces shot noise because of the charge packet left behind (which is also characterized by a Poisson distribution) [81]. The variance of that charge packet is therefore given by the mean

$$\overline{(N_\varepsilon)^2} = 2\varepsilon N_{\text{phase}} \times \left[N_{\text{CCD}}(N_{\text{signal}} + N_{\text{background}}) + \frac{N_{\text{CCD}}\left(N_{\text{CCD}} + \dfrac{1}{N_{\text{phase}}}\right)}{2} \frac{J_{\text{D}} A_{\text{coll}} \tau_{\text{stage}}}{q} \right], \tag{30}$$

where N_{CCD} is the number of CCD stages in the transfer, $N_{\text{background}}$ is the background charge which is not photon-generated (e.g., dark charge transferred from the parallel array to the serial register), and τ_{stage} is the collection time of the dark current within one stage (not one phase) of transfer. The last term arises because the dark charges are constantly being accumulated while the charge packet is being transferred. The term N_{signal} is the number of signal electrons at the start of the N_{CCD} stage transfer. When the signal electrons are accumulated in each transfer, as is the case for the vertical transfer of the TDI-CCD imager parallel array, the full signal is obtained only at the end of all of the transfers. The expression for the transfer inefficiency noise is

$$\begin{aligned}\overline{(N_\varepsilon)^2} &= 2\varepsilon N_{\text{phase}} \left[N_{\text{stage}} \left(\frac{N_{\text{stage}} + \dfrac{1}{N_{\text{phase}}}}{2} \right) \times \left(\frac{SA_{\text{pixel}} Ht_{\text{line}}}{q} + \frac{J_{\text{D}} A_{\text{coll}} t_{\text{line}}}{q} \right) + N_{\text{background}} N_{\text{stage}} \right] \\ &= 2\varepsilon N_{\text{phase}} \left[\left(\frac{N_{\text{stage}} + \dfrac{1}{N_{\text{phase}}}}{2} \right) \times (N_{\text{signal}} + N_{\text{dark(parallel)}}) + N_{\text{background}} N_{\text{stage}} \right]. \end{aligned} \tag{31}$$

The reset noise is the noise due to charging the floating diffusion diode through the reset switch. The expression obtained for the reset noise [81, 88] is

$$\overline{(N_{\text{reset}})^2} = \frac{kTC_{\text{o}}}{q^2}. \tag{32}$$

That noise source can be effectively eliminated by a correlated double-sampling (CDS) circuit at the output [78, 85, 88, 89].

The input transistor of the source-follower output amplifier displays thermal and $1/f$ noise. The expressions obtained for these sources of noise [81, 90–92] are

$$\overline{(N_{\text{amp,thermal}})^2} = \left(\frac{C_{\text{o}}}{q}\right) \frac{4kT\alpha\Delta f}{g_{\text{m}}}, \tag{33}$$

$$\overline{(N_{\text{amp},1/f})^2} \propto \frac{N_{\text{ss}}\Delta f}{WLf}, \tag{34}$$

where W and L are the width and length of the source-follower input transistor, α is a constant having a value from about 2/3 to 10 [81, 90], and Δf is the bandwidth. The correlated double-sampling (CDS) circuit [78, 88, 89] usually employed at the CCD output circuit effectively filters out the $1/f$ noise of the input transistor [85, 89, 93].

The analog-to-digital conversion quantization noise can be expressed [78] as

$$\overline{(N_{\text{quantize}})^2} = \frac{1}{b}\left[\frac{N_{\text{signal}}(full)}{2^b}\right]^2. \tag{35}$$

Using the parameters listed in Table 3, we calculate the rms noise of a 3072 × 32-stage TDI-CCD imager. The speed at which this TDI-CCD imager is operated is moderate and corresponds to that used, for example, in high-quality camera-type color scanning [7–9] of museum art, for which illumination power must be kept low.

In **Figure 12** is shown the calculated signal-to-noise ratio for unity scene contrast as a function of the number of signal electrons (N_{signal}), for TDI-CCD imagers having different numbers of stages. **Figure 13** shows the calculated components of the noise electrons of the 3072 × 32-stage TDI-CCD imager of Table 3. At high signal levels, the signal-to-noise ratio is dominated by the photon shot noise ($\sqrt{N_{\text{signal}}}$ dependence). At low signal levels, the noise due to trapping by interface states (the imaging parallel array is a surface-channel CCD) dominates the noise, and is greater than the quantization noise and the dark-current shot noise in the parallel array. For buried-channel parallel array designs, the quantization noise and dark-current shot noise in the parallel array dominate the low-signal-level noise. For applications in which there is more illumination power available (e.g., in office document scanning), the TDI-CCD imager can be operated at a higher speed, and the dark-current shot noise can be further reduced.

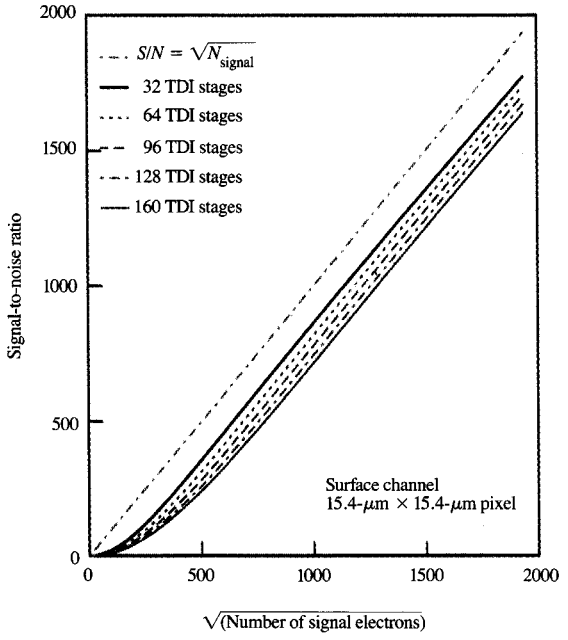


Figure 12

Calculated signal-to-noise ratio as a function of signal level. The signal-to-noise ratio at a high signal level is limited by photon shot noise and follows an $\sqrt{N_{signal}}$ dependence. Unity scene contrast is assumed.

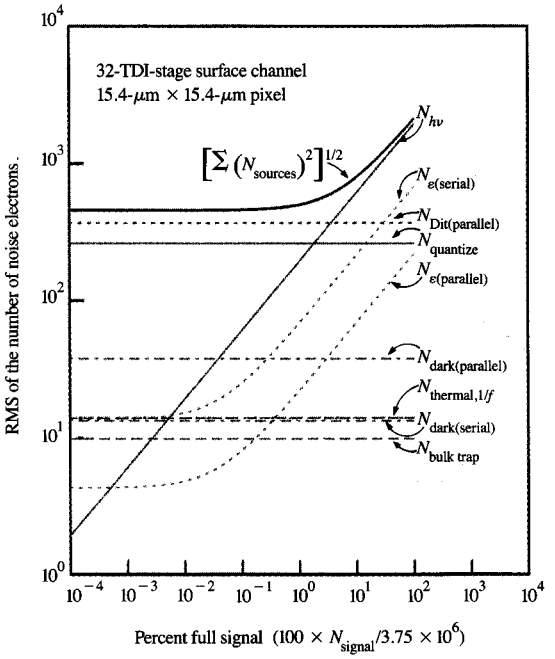


Figure 13

Calculated numbers of noise electrons arising from various sources for a 32-stage TDI-CCD imager, assuming use of a surface-channel parallel array design. Unity scene contrast is assumed.

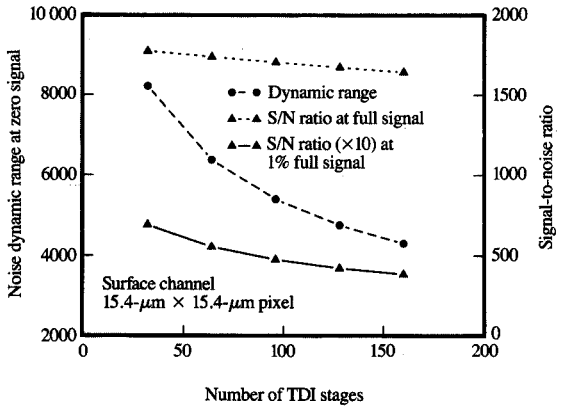


Figure 14

Calculated noise dynamic range at zero signal and signal-to-noise ratio assuming use of a surface-channel parallel array, as a function of the number of TDI stages.

The noise dynamic range at zero signal is defined as the ratio of the maximum signal to the noise at zero signal. **Figure 14** compares the noise dynamic range at zero signal and the signal-to-noise ratio for unity scene contrast for TDI-CCD imagers having different numbers of TDI stages, assuming the same device characteristics, integration line-scan time, and full charge capacity. The dynamic range and the signal-to-noise ratio decrease with an increase in the number of TDI stages mainly because of an increase in the noise associated with the presence of interface states and the dark-current shot noise. The noise dynamic range at zero signal for a buried-channel parallel array design is larger than that of a surface-channel parallel array design because of the absence of noise due to trapping by interface states. For a buried-channel parallel array design, the dynamic range and the signal-to-noise ratio decrease slightly with an increase in the number of TDI stages, mainly because of an increase of dark-current shot noise. Note, however, for the buried-channel case, if the same amount of signal charge is collected, the integration line-scan time is proportionally shorter for devices with more TDI stages. Thus, the amount of dark-current noise should be independent of the number of TDI stages. In this case,

the signal-to-noise ratio and dynamic range for the buried-channel parallel array design are virtually independent of the number of TDI stages.

Figure 15 compares the signal-to-noise ratio at various signal levels for buried-channel and surface-channel parallel array designs having the same pixel size. Since the charge capacity per unit area of the buried-channel design is smaller, use of the buried-channel parallel array design leads to a smaller signal-to-noise ratio at the photon-shot-noise-limited region (high signal levels). However, buried-channel parallel array designs are found to lead to lower noise at low signal levels. Thus, the signal-to-noise ratio for the buried-channel parallel array design at low signal level is superior. The crossover point in Figure 15 is at about 1% of full signal. For applications in which the illumination is controllable (e.g., document scanning), a surface-channel parallel array design offers a larger signal-to-noise ratio for a larger range of signal levels than does a buried-channel parallel array design.

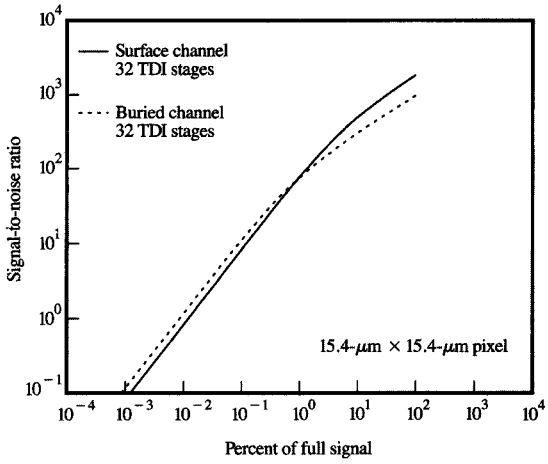


Figure 15

Comparison of the expected signal-to-noise ratio for TDI-CCD imagers at various signal levels, assuming the use of a buried-channel parallel array design and a surface-channel parallel array design. The comparison is for an identical pixel size. Unity scene contrast is assumed.

- *Pixel size*

The pixel size of the TDI-CCD imager is an important consideration in its design [20]. Considerations such as charge capacity, signal-to-noise ratio, carrier diffusion MTF loss [94], MTF of the imaging optics [20, 95], chip size, and yield have been well documented in the literature. **Table 4** compares the advantages of using large vs. small pixel sizes.

Apart from the signal-to-noise ratio discussed in the previous section, pixel size has a direct impact on imager size. This has several ramifications: For example, for a 15.4-μm × 15.4-μm pixel size in the imaging area, the chip length would have to be about 48 mm for a 3072-element TDI-CCD imager [13]. This is an appreciable chip length, considering that in order to accommodate such a large size, the cost of the optical components required would be expensive and the back focal plane would have to be longer—making a more compact scanner system more difficult to achieve. Furthermore, the larger associated chip area would have an impact on chip yield, mechanical stability, handling ease, etc.

From the example cited above, it is inferred that it would be impractical to fabricate a 4096-element TDI-CCD imager using a pixel size of 15.4 μm × 15.4 μm. In addition, the associated long polysilicon gate-electrode length of the parallel array would impose an upper limit to the line-scan speed of large arrays because of the RC delay considerations discussed earlier. However, a large pixel size is always desirable from the viewpoint of charge capacity, signal-to-noise ratio, and MTF loss due to charge carrier diffusion [94]. These aspects of the TDI-CCD imager reflect the opposing requirements that exist of *imager resolution* and *charge capacity*, a trade-off which is common to area imagers, e.g., the frame-transfer CCD.

Table 4 Comparative advantages of using large vs. small pixel size.

Large-pixel advantages	*Small-pixel advantages*
Larger charge capacity	Smaller chip size, higher chip yield
Higher signal-to-noise ratio	Simpler mechanical design and handling
Lower MTF degradation because of carrier diffusion	More compact optical system
Higher MTF of optical system	Smaller RC delay of parallel array

Other considerations regarding the pixel size that are less frequently discussed are the large aspect ratio of TDI-CCD imager chip architecture, and the associated photolithographic exposure system required to produce such a chip. The optical field size of a typical 5× stepper is about 25–30 mm. For a pixel size of 9 μm × 9 μm, a 3072-element TDI-CCD imager would have a chip length of about 28 mm, which is close to the maximum field size of typical 5× steppers. Therefore, the use of 1× full wafer exposure lithography would be necessary for chips with larger sizes; otherwise, field stitching would be required. However, 1× full wafer exposure lithography requires the

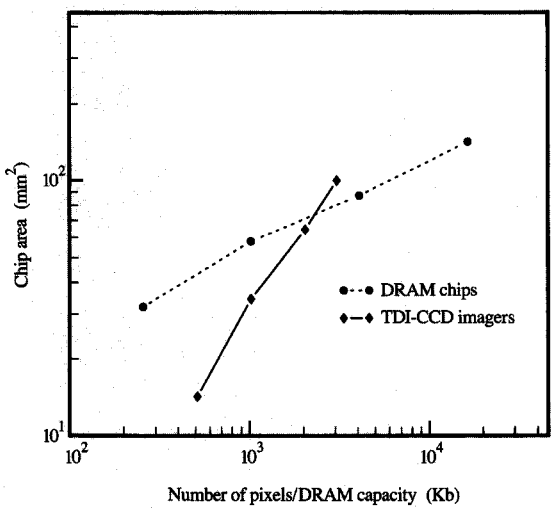


Figure 16

Comparison of the chip area of TDI-CCD imagers and DRAMs. The TDI-CCD imager data represent the family of TDI-CCD imagers of Section 5. The DRAM data were obtained from IEDM and ISSCC papers presented by various IBM authors, and represent the evolution from a 1-μm to a 0.35-μm minimum-feature-size capability.

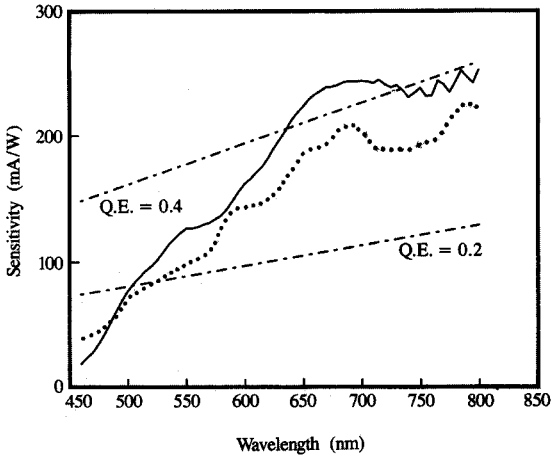


Figure 17

Typical spectral sensitivity of a TDI-CCD imager, with (solid line) and without (dotted line) polyimide layers present.

use of more relaxed design ground rules than does 5× lithography, making the design of an imager having a small pixel difficult.

Figure 16 shows that TDI-CCD imager chip sizes are already comparable to the state-of-the-art DRAM chips. The problem of limited yield for large chip sizes cannot be ignored, because CCD imagers cannot employ the redundancy techniques used in DRAMs. It should be noted that in the course of evolution toward higher-density memory chips, continued innovations have been employed to achieve reductions in memory cell size. Thus, Figure 16 shows that the chip area has been a sublinear function of memory size. For the case of CCD designs, the CCD cell structure has been basically the same throughout each generation. Large CCD arrays have been designed by enlarging chip size; thus, associated chip area has increased linearly.

- *Spectral response*

The TDI-CCD imager for visible imaging employs MOS photogates in its imaging area. The presence of polysilicon gates in the imaging area results in two undesirable features in spectral response:

- Absorption of light by the polysilicon gates, resulting in poor photosensitivity, especially in the blue (short wavelengths) [96].
- Uneven quantum efficiency across the spectrum due to multiple-layer reflections by the MOS gates [97].

The spectral responsivity $R(\lambda)$ and quantum efficiency $\eta(\lambda)$ are defined [78] as

$$R(\lambda) = \frac{q\eta(\lambda)}{hc/\lambda} \quad \left[\frac{\mathrm{A}}{\mathrm{W}}\right]$$

or alternatively as

$$R(\lambda) = \frac{q\eta(\lambda)}{hc/\lambda}\beta_v A_p \quad \left[\frac{\mathrm{V}}{\mathrm{J\ cm^{-2}}}\right], \tag{36}$$

where hc/λ (the energy per photon) $\simeq 1.24 \times 10^{-6}\, q/\lambda$, q is the electron charge, h is Planck's constant, c is the velocity of light, λ is the wavelength of light (in meters), β_v is the conversion coefficient of the output detection node in units of V/C, and A_p is the photosite area in cm^2.

Figure 17 shows the spectral sensitivity of typical TDI-CCD imagers with polysilicon (400 nm) MOS gates in the imaging area [12]. The quantum efficiency is not only affected by the absorption of light by the polysilicon gate, but is also strongly dependent on the interference effects of the multiple-layer films on the gate structure [97]. For the imagers of Figure 17, one contains two layers of polyimide (between the first metallization layer and the second, and above the second), and the other contains no polyimide layers. In the case of the former, multiple-layer interference effects occur. The low sensitivity below 500 nm is due primarily to absorption by the polysilicon

gates. The fine structures of the responsivity between 500 nm and 800 nm are due primarily to the multiple-layer structure of the MOS gates [67]. For λ between 550 nm and 650 nm, the quantum efficiency (without optimization) is typically between 0.2 and 0.4 for polysilicon photogate CCDs. This quantum efficiency is low compared to that of silicon photodiodes, which typically can achieve a quantum efficiency of from 0.5 to 0.7 [88, 98].

Interference effects associated with the dielectric layers of the MOS gates can be optimized by choice of layer materials and thicknesses to produce the desired fine structure in the responsivity [21, 67, 97]. Dyck and Wight [21] described in detail an example in which the dielectric layers (materials and thicknesses) above the MOS gates were optimized to achieve a quantum efficiency of up to 0.5. Anagnostopoulos et al. [96] showed that by using a thin (150-nm) polysilicon gate, the blue response can be improved (as a result of reduced absorption of light by the polysilicon gate). Another way to achieve good, uniform quantum efficiency is to use indium tin oxide (ITO) transparent electrodes as the MOS gates [3, 26, 31]. For high-quality color imaging applications where custom tailoring of the spectral response of the imager to match specific spectral characteristics (e.g., the color-matching function of the human eye) [99] is required, it is important to achieve a smooth sensor spectral response.

Figure 18 shows the spectral sensitivity of a TDI-CCD scanner with RGB colored glass filters that were custom-designed to match the CIE Standard Observer [100]. The spectral transmittances of the colored glass filters used were smooth, with no local irregularities. The irregular spectral characteristics of the scanner were due mainly to the nonuniformity of the spectral response of the TDI-CCD imager. Finally, for applications in which a controlled light source is employed (e.g., document, museum, and graphic art imaging), the deficiencies of the spectral response of the TDI-CCD imager can be compensated by using a custom-designed light source (e.g., a blue-enhanced fluorescent lamp) [7, 101].

4. Comparison with the photodiode linear array imager

Both the photodiode linear array imager and the TDI-CCD imager compete in similar application areas. Both require mechanical scanning in the y-direction; thus, the designs of their imaging systems are similar. In this section, we compare the advantages and disadvantages of these two types of imagers.

The photodiode linear array imager usually is able to offer a higher pixel count (hence higher resolution) than the TDI-CCD imager, since it can employ a bilinear or quadrilinear CCD architecture [102]. By placing a CCD serial register on either side of the photodiode sensors, the pixel pitch can be halved for a given CCD cell size. Single-chip linear array imagers with 3000 to 8000 elements have been reported [95, 103–109], whereas the largest single-chip TDI-CCD imager [13] has yet to exceed 3000 elements. In **Figure 19** a comparison is shown of the

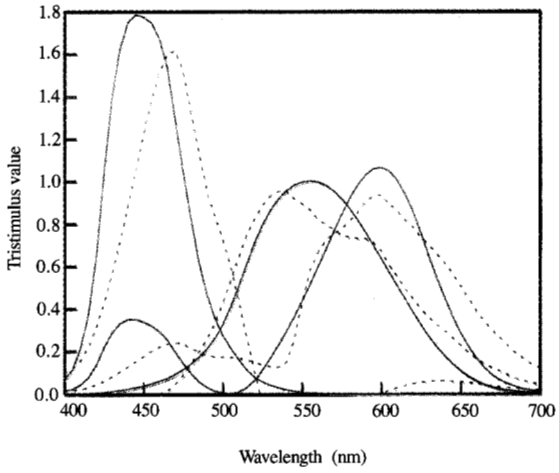


Figure 18

Spectral sensitivity of a scanner (dashed lines) using a TDI-CCD imager and colored glass filters that were custom-designed to match the spectral characteristics of the CIE Standard Observer (solid lines).

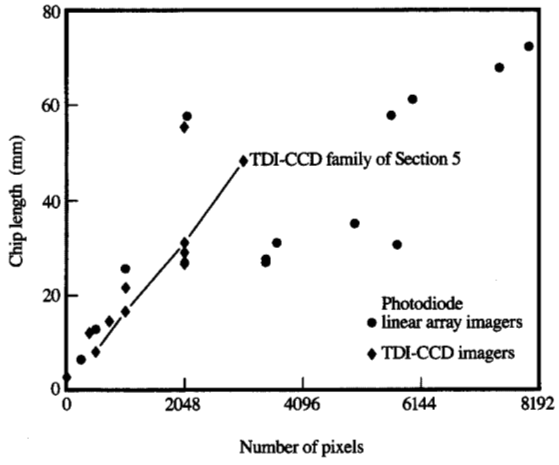
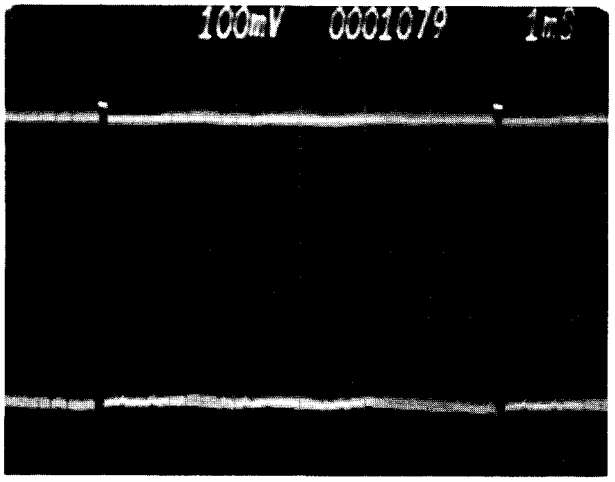
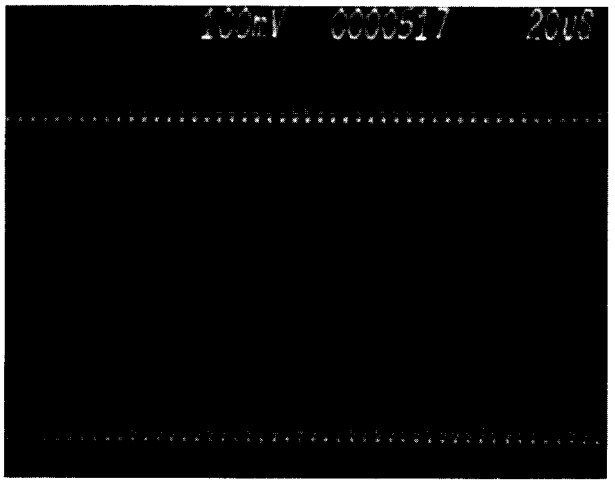


Figure 19

Comparative chip lengths and numbers of pixels for a sampling of experimental and commercial TDI-CCD imagers and experimental and commercial photodiode linear array imagers.



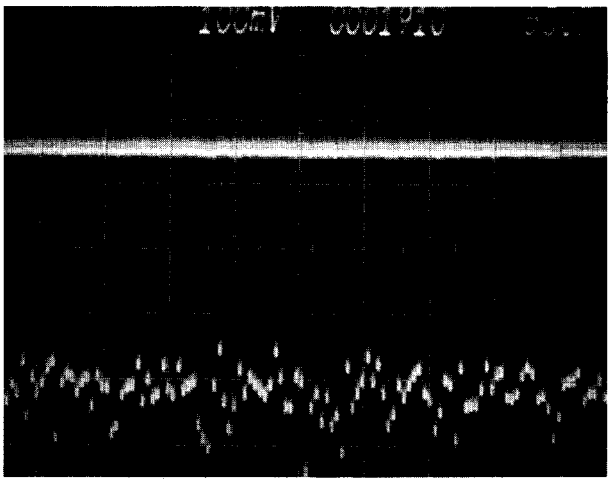
(a)



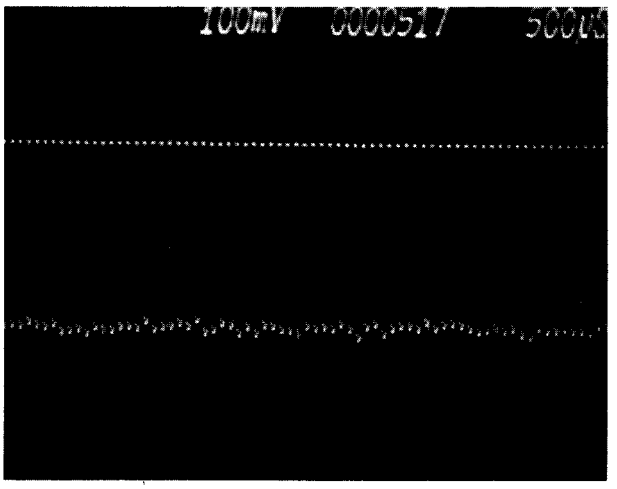
(b)

Figure 20

Oscillographs of output with diffuse uniform illumination, illustrating photoresponse uniformity: (a) Full scan line. (b) Detail of about 50 cycles of the scan. From [13].



(a)



(b)

Figure 21

Oscillographs of dark output, illustrating improved uniformity in the TDI mode: (a) Frame transfer mode. (b) TDI mode. In each case, integration time was 209 seconds. From [13].

device pixel sizes of several TDI-CCD imagers [6, 12, 13, 31, 110, 111] and photodiode linear array imagers [95, 103–109, 111].

The use of MOS photogates results in a nonuniform spectral responsivity and a lower quantum efficiency. For applications in which a uniform quantum efficiency is required, the photodiode linear array imager is superior. Since TDI operation increases the exposure of the imager without increasing the line-scan time, the quantum efficiency does not truly reflect the imaging speed of the TDI-CCD imager. For a meaningful comparison with other CCD architectures, one needs to examine the "scanning responsivity" [12] (or effective responsivity). For a specified line-scan time, an N-stage TDI-CCD imager receives N times the exposure received in one line-scan time. Thus, the "scanning responsivity" (or effective responsivity) of such a TDI-CCD imager is the responsivity multiplied by the number of TDI stages. In a photodiode linear array imager, the number of TDI stages is unity. As a result, the lower quantum efficiency of the TDI-CCD imager can be more than compensated for by the increase in exposure offered by the TDI mode of operation. For example, for the same line-scan time, a 32-stage TDI-CCD imager with a quantum efficiency of 0.2 would have 11 times the scanning responsivity of a photodiode linear array with 0.6 quantum efficiency ($32 \times 0.2/0.6 \simeq 11$).

The pixel-to-pixel photoresponse uniformity of the TDI-CCD imager is excellent compared to that of the

Table 5 Architecture, features, and applications of a family of TDI-CCD imagers designed in the authors' laboratory.

Imager designation	*Architecture*	*Features and applications*
TDI-2S	512 × 32-stage, one output port, 20-MHz pixel rate	10–15 s/page, office ambient illumination, for optical character recognition
TDI-2	2048 × 32-stage, one output port, 20-MHz pixel rate	0.8–1.5 s/page, flatbed scanner, 240 pels/in. for A4 document
TDI-3	1024 × 32-stage, eight output ports, 96-MHz pixel rate, electronic exposure control of 1× and 32× sensitivity	350 document-in./s (40 Federal Reserve Bank checks per second) at 250 W, *f*/2.8, 240 pels/in.
TDI-4	3072 × 32-stage, two output ports, 24-MHz pixel rate	1–2 page/s, camera-type scanner for museum art object and high-resolution scanning
TDI-5	3072 × 64-stage, two output ports, 24-MHz pixel rate	1–2 page/s, camera-type scanner for museum art object and high-resolution scanning

photodiode linear array imager. This is a result of the photoresponse averaging of all the pixels in the same TDI column; assuming independent irregularities, any local photoresponse nonuniformity is reduced by $1/N$ because of the N-stage averaging. **Figure 20** illustrates the output uniformity of the 3072 × 32-stage TDI-CCD imager recently described by Schlig [13]. The averaging effect is also exhibited by its extremely uniform dark-current distribution. **Figure 21** shows the dark current of the imager with 32-stage TDI averaging and without such averaging (signal charges clocked out in frame-transfer mode). Pixel-to-pixel uniformity is important in order to obtain good gray-scale images.

The size of a TDI-CCD imager chip increases with the number of integration stages. This has an adverse impact on imager chip yield, and limits the practicality of implementing a tri-color (RBG), three-array TDI-CCD imager chip. On the other hand, trilinear (three linear arrays on the same chip) photodiode array imagers have already been implemented [109]. An integrated color imager chip is highly desirable for color scanning.

In the photodiode linear array imager, scanning is carried out line by line. Thus, scanning can be stopped at any arbitrary position and restarted at the same scan line without losing the integrity of the signal charge. This cannot be done with the TDI imager. One common reason for stopping while scanning is that for high-resolution scanning, the data buffer of the host computer/controller may not be large enough to capture the entire page of the image in memory.

Finally, when making fair scanning speed comparisons of image scanners, it is important to either 1) compare the irradiance required to attain a specified signal-to-noise ratio (usually limited by photon shot noise at high signal levels) at a fixed line-scan time, or 2) compare the line-scan time required to attain a certain signal-to-noise ratio at a specified irradiance. A comparison of the percentage of photocharge saturation at a certain irradiance and line-scan time is not meaningful, because the signal-to-noise ratio must be taken into consideration.

5. Design case studies of a family of TDI-CCD imagers

In this section, we describe a family of TDI-CCD imagers [6, 7, 11–13] designed for various document and museum art object scanning applications. **Table 5** summarizes the architecture, features, and applications of the imagers, which are characterized by the following:

- Use of a surface-channel CCD in the parallel imaging array to maximize the photocharge capacity of the CCD per unit area. This is traded off against the buried-channel CCD's better transfer efficiency and lower noise at low signal levels (due to transfer inefficiency and interface state trapping; see the section on noise). Because the line-scan time is typically relatively long, the lower speed of the surface-channel CCD is not a disadvantage here. Transfer inefficiency of the surface-channel CCD is not a limitation for 32 stages of TDI.
- Use of a buried-channel CCD serial register to maximize the speed and transfer efficiency. Speed and transfer efficiency are important in the serial register, since the number of transfers is relatively large.
- Use of a four-phase, overlapping, double clock to maximize the charge capacity of the CCD and minimize the MTF associated with discrete charge movement.
- Use of a tapped output structure (TDI-3, TDI-4, and TDI-5) to increase the effective pixel output rate.
- Use of a floating diffusion output diode and virtual drain output structure [11].
- Use of 32 to 64 stages of TDI to achieve a 10× to 20× scanning responsivity improvement over photodiode linear array imagers. The number of TDI stages is kept relatively small to minimize MTF degradation due to

velocity mismatch and angular misalignment, and to maximize device yield.

The imagers were fabricated at IBM manufacturing lines with a nominally 2-μm NMOS process involving the use of two polysilicon layers and two metallization layers. The process was originally intended for NMOS logic applications. Because of the need for the fabrication process to remain compatible with the existing NMOS processes, some CCD device performance was sacrificed. For example, the thicknesses of the gate oxide, the gate polysilicon, and the dielectric layers above the gate polysilicon layer could not be optimized to achieve peak CCD performances and desirable spectral responses.

The TDI-2S imager has been demonstrated to be useful for scanning office documents in ambient illumination, without additional lighting. A prototype flatbed scanner (with auto-document-feeding) using the TDI-2 imager has been designed and constructed, and found to be useful to scan A4-sized (~8.5 in. × 11 in.) documents at 1.5 seconds per page (40 pages per minute), 240 pels per inch, with 8-cd/cm^{-2} fluorescent illumination. The TDI-3 imager has been employed in a bank check scanner that can scan at a rate of 350 in./s (equivalent to 40 Federal Reserve checks per second) with 250 W of illumination, at an aperture of $f/2.8$ and a resolution of 240 pels/in. The TDI-4 imager has been employed in a 12-bit, high-quality, high-resolution, color, camera-type scanner for scanning museum art objects under moderate to low illumination. This camera-type scanner fully exploits the excellent pixel uniformity and scanning responsivity in a demanding application which requires a high signal-to-noise ratio (for subsequent color calibration and processing).

6. Concluding remarks

The trend in solid-state imagers has been toward higher performance and higher quality. For the TDI-CCD imager, further development of high-resolution chips with large numbers of pixels per row is inevitable. For example, for scanning A4-sized office documents, a 2074-element TDI-CCD imager provides 240 pels/in. If the resolution is to be increased to 400 pels/in., a TDI-CCD imager with 3456 elements would be required. As discussed in an earlier section, the dilemma of chip size limitation and pixel size is still unresolved. The reduction in minimum feature size and increase in overlay accuracy resulting from the lithographic techniques associated with ULSI development should permit the design of imagers with a smaller pixel size. However, when chip size reaches the limit of the stepper, 1×, full wafer exposure lithography must continue to be used (resulting in larger overlay inaccuracies and precluding the design of small pixels) unless stitching techniques can be employed [112]. More importantly, one must keep in mind that if pixel size is to decrease, the charge capacity and the signal-to-noise ratio of the CCD will decrease, unless a new CCD structure can be developed which can achieve a large charge capacity without significantly increasing the layout area of the CCD cell in the imaging parallel array [113, 114]. This has already been applied to area imagers [115–117].

As imaging applications expand from conventional black-and-white office document scanning into other applications such as film and photograph scanning (both for consumer and archival purposes), museum art object scanning, and electronic publishing, to name a few, the acquisition of high-quality color images should become increasingly important. For high-quality color image acquisition, it is desirable to use a colorimetric imaging system with a spectral response similar to that of the human eye. Compared to conventional RGB color separation, a colorimetric color imaging system permits faithful color representation independent of the capturing and display/printing devices and avoids metamerism [8, 9, 99]. Toward achieving this goal, it would be highly desirable to achieve a smooth and uniform spectral response for the TDI-CCD imager.

The use of on-chip integral color filters may not be practical for producing high-resolution TDI-CCD imagers because of chip size (hence yield) limitations. The use of off-chip color imaging methods that make use of a color filter wheel, color filter stripes, a grating, dichroic filters, or prism beam splitters, all have certain limitations and leave much to be desired. For the most common methods (involving use of a color filter wheel, color filter stripes, or dichroic filters), the transmittance of the blue filter required is considerably less than that of the red and green filters that are also required. Compounded with the low photosensitivity of the polysilicon MOS gate TDI-CCD imager, the blue color scan is very slow compared to the red and green scans.

The TDI-CCD imager offers a significant improvement in overall system photosensitivity and pixel-to-pixel photoresponse uniformity over the photodiode linear array imager. New applications which are served only by the TDI-CCD imagers should become mature and complement the capabilities of other types of CCD imagers. For the imaging of museum art objects, because use must generally be made of a low illumination, the TDI-CCD imager appears to be preferable.

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