# Reactive ion etching technology in thin-film-transistor processing

by Y. Kuo

**This paper discusses reactive ion etching (RIE) process issues in preparing thin-film transistors (TFTs) for liquid crystal displays (LCDs). Three areas were examined in detail: gate metal etch, dielectric etch, and a-Si:H etch, both intrinsic and $n^+$ doped. Although there are different requirements for each step, the basic principles for the etching process are similar. For example, each process includes three major mechanisms: plasma-phase chemistry, particle transport phenomena, and surface reactions. All data on the etching results were interpreted according to these principles. Finally, a TFT characteristic curve based on RIE of some of the most critical process steps is presented.**

## Introduction

The active-matrix addressing method is the leading method in driving high-quality liquid crystal displays (LCDs) [1]. There are two kinds of semiconductor devices, i.e., diodes and thin-film transistors (TFTs), that are commonly used as the driving unit for each pixel. Because of their gray-scale capability, TFTs are more often used in LCDs than are diodes. **Figure 1** shows structures of two of the most popular inverted, staggered TFTs. Compared with the process shown in Figure 1(b), the process of Figure 1(a) is simpler because it needs one less mask. The wet etching method is popular in preparing these TFTs. However, the process of Figure 1(a) includes a very critical etching step in which the heavily doped $n^+$ layer must be selectively etched from the intrinsic a-Si:H layer. This is difficult to achieve with wet etching. A plasma etching method is often used for this purpose [2, 3]. There are other areas, such as opening small vias, sloping the sidewall, and descumming of developed photoresist, where the plasma etching method shows clear advantages over the wet etching method. This makes plasma etching an effective alternative.

There are some unique features in the TFT/LCD etching process that are different from those in other microelectronics etching processes. For example, the inverted, staggered structure has the gate patterned and

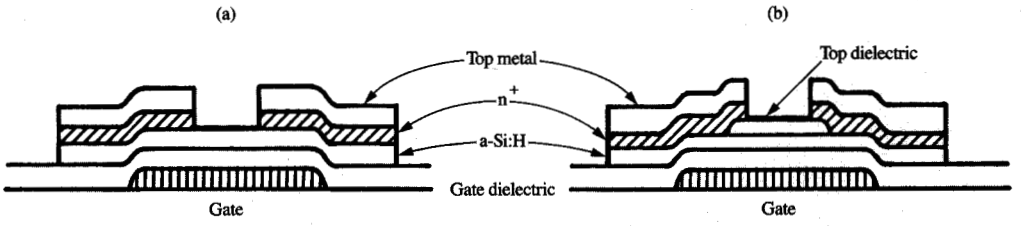


**Figure 1**

Structures of conventional inverted, staggered thin-film transistors.

etched first. Other thin films are then deposited on top of the gate. Because of this, step coverage is an important issue, and the profile of the etched gate metal must be tightly controlled. In preparing a-Si:H TFTs, the semiconductor and dielectric films are often deposited by the low-temperature plasma-enhanced chemical vapor deposition (PECVD) method, e.g., at a temperature lower than 350°C. These deposited films contain a large amount of hydrogen, which is critical to the film quality and interfacial density of states. Compositions of the PECVD silicon nitride and silicon oxide vary with the deposition temperature and other process parameters. For TFT applications, they are usually nonstoichiometric. When these films are treated at a temperature higher than the deposition temperature, they lose hydrogen and their compositions change. TFT device characteristics change with the variation of the film composition. Each film in a TFT is very thin, varying from a few tens of nanometers to less than half a micron. The etch selectivity between two adjacent films is critical. Sometimes uncommon materials are used in the fabrication of TFTs. For example, metal oxides such as $Ta_2O_5$ have been used as part of the gate dielectric material. This metal oxide layer must later be etched off the gate metal; process information for this step is scarce.

The LCD substrate is usually a transparent glass that has a multicomponent composition. It is subject to HF attack and cannot stand a temperature higher than 600°C. The plasma attack of the glass must be minimized. The substrate size is usually larger than a silicon wafer; it can be 10 inches on a side or larger. Since the entire plate of the LCD must function properly, each glass substrate is equivalent to a die in VLSI technology. A high aperture ratio (percentage of the transparent area in a pixel) is needed for a display for backlight efficiency. Therefore, the majority of the display area is transparent. During the etch, the masked area is much smaller than the exposed area, except in some special layers such as that of the via.

In this paper, we describe the application of RIE processes to various stages of a-Si:H TFT processing. The controlling mechanism of each RIE step is discussed. Common issues in an etching process such as the etch rate and etch selectivity are examined.

## Experiment

The a-Si:H film was deposited in a Solarex PECVD reactor using pure silane. $SiN_x$ was deposited in the same reactor using silane and ammonia at 430 mTorr and 250°C. Heavily doped n-type a-Si:H films, which have a typical resistivity of 100 Ω-cm, were deposited in a Technics or Solarex plasma system using 1% phosphine in silane at 275 mTorr and 275°C. Molybdenum, tantalum, and $Ta_2O_5$ were sputter-deposited from corresponding targets. Films were deposited on Corning 7059 glass substrates or on (100) silicon wafers. No etch-rate differences were detected between these two substrates. Samples were patterned using Shipley 1350J positive photoresist exposed through a line-and-space test pattern. An Oriel exposure table equipped with a mercury lamp was used for the exposure step. For the sloped etching of molybdenum, the photoresist was hard-baked at 180°C for one half hour to flow the photoresist. A thick layer of the film, e.g., 0.5–1 μm, was used in the etch experiments to determine the average film etch rate. The photoresist thickness was about 1.5 μm.

A Plasma-Therm 2480 plasma reactor [4] was used for RIE experiments. During the process, the plasma was monitored with an emission spectroscope. F and Cl concentrations reported in this paper were taken from emission spectra. They were in arbitrary units and were not corrected with the actinometry method. Therefore, they are only indications of the true concentrations. The cathode self-bias voltage was also recorded. Film etch rates were determined from film thickness measurements. Electron spectroscopy for chemical analysis (ESCA) and auger electron spectroscopy (AES) were used to study the

surface composition and bonding information before and after the etch. We used these results, in combination with process conditions, to explain the surface contamination, damage, and possible reaction mechanisms of an etch process. Electron spin resonance (ESR), which measures the density of unpaired electrons of a solid, was used to detect $SiN_x$ damage. ESR signals of the $SiN_x$ films were measured before and after etch. Therefore, the damage was proportional to the differential ESR signal. ESR was used to detect both the surface damage and the bulk damage. For a short period of etch time, the damage was restricted to the surface. The $CF_3Cl$ etched surface contained various elements from the plasma and the substrate. No polymer was detected. Damages such as the dangling bonds were immediately passivated by air before the analysis was done. They could not be detected by ESR. TFTs and test structures were used to measure the current leakage between the source and the drain of the TFT after RIE of the $n^+$ layer.

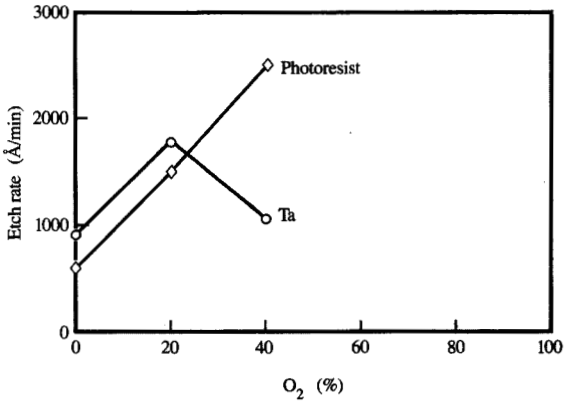


**Figure 2**

Tantalum and photoresist etch rates as a function of $O_2$ concentration in the mixture $CF_4 + O_2$ at a total flow rate of 100 $cm^3$/min, at 100 mTorr, 1000 W.

## Results and discussion

• *Gate metal etch*

In an inverted, staggered TFT structure, the gate metal line step is one of the major step coverage problems of the finished device. If the gate line is etched in a very sloped shape, e.g., 30°, the step coverage problems can be minimized. In addition to material and process difficulties, highly conductive metals such as copper and aluminum are not proper gate metals for TFTs because of the difficulty in controlling the etched slope. Refractory metals such as molybdenum and tantalum are popular TFT gate metals, although their conductivities are lower than those of copper or aluminum. These metals have reasonable conductivities and are resistant to high process temperatures. Tantalum can be easily anodized to form a self-aligned gate dielectric structure. When these metals are sputter-deposited directly onto glass, they have a columnar structure, which cannot be etched to form a sloped wall with a wet solution. A RIE photoresist-erosion method can be an effective method for etching molybdenum lines with various angles [4].

In a computer simulation study, it was found that to achieve a fine line with a slope angle less than that of the original masking photoresist, the photoresist etch rate must be higher than the metal etch rate [5]. Therefore, etch rates of both materials (i.e., the metal and the photoresist) must be taken into consideration. The photoresist etch rate is related to the oxygen concentration in the feed stream and the ion bombardment energy [6, 7]. The molybdenum etch mechanism is more complicated than the photoresist etch mechanism. It is a function of the plasma-phase chemistry (such as the fluorine, chlorine, and oxygen concentrations), the ion bombardment energy, and surface reactions. It was observed that in the $CF_3^+$ ion beam etch process, carbon residues were formed on the molybdenum surface [7]. This residue can be a rate-limiting step in the whole etching process. In the $CF_4/O_2$ etching process, the carbon residue did not play an important role, because the molybdenum etch rate was affected more by the plasma-phase chemistry than by the ion bombardment energy [5]. A RIE process that gives a high molybdenum etch rate, such as one using a $CF_3Cl/O_2$ or $CF_2Cl_2/O_2$ plasma, is improper for this application, because the resulting photoresist-to-molybdenum etch rate ratio is less than 1 over a wide process range.

**Figure 2** shows the etch rate of tantalum and photoresist in $CF_4/O_2$ plasmas. This etch characteristic is similar to that of molybdenum in $CF_3Cl/O_2$ plasmas; e.g., the etch rate vs. $O_2$ curve has a peak between 20% and 40% $O_2$ concentrations. For molybdenum etched in a $CF_4/O_2$ plasma, the etch rate curve peaked at around 80% $O_2$ [5]. This etch curve is also similar to the fluorine concentration curve, which indicates that the tantalum etch is related to the plasma-phase chemistry. The change of self-bias voltage is not consistent with the etch rate. The photoresist-to-tantalum etch rate ratio increases monotonically with the increase of $O_2$. The ratio reaches 1 when the $O_2$ concentration becomes greater than 25%. To obtain a very sloped tantalum line, we have to add more than 25% of $O_2$ to the $CF_4$ gas. When $CF_3Cl$ was used to replace $CF_4$ to etch tantalum, the etch rate was increased almost an order of magnitude [8]. However, the photoresist etch rate decreases with the replacing of one F with one Cl [4]. The photoresist-to-tantalum etch rate ratio

in the $CF_3Cl/O_2$ plasma is lower than that in the $CF_4/O_2$ plasma. The former is therefore not useful in preparing a sloped tantalum gate structure.

If the gate metal is directly deposited on the glass substrate, the glass is exposed to the plasma in the over-etch period. Therefore, the phenomenon of plasma attack of glass must be addressed. Major components of the Corning 7059 glass are $SiO_2$ (49%), $Al_2O_3$ (10%), $B_2O_3$ (15%), BaO (25%), and $As_2O_5$ (1%). After exposure to the $CF_4$ (80%)/$O_2$ (20%) plasma at 100 mTorr and 1000 W for five minutes, the surface contains only aluminum oxide and barium oxide, as determined by AES [9]. The glass etch rate was about 100 Å/min. In a typical molybdenum or tantalum etch process, the over-etch time is much shorter than five minutes. Therefore, the plasma attack of the glass is negligible under a typical molybdenum or tantalum sloping process.

- *Dielectric etch*

In an inverted, trilayer TFT structure, a thin-film dielectric material is used for both the gate dielectric and the channel passivation material. PECVD films such as $SiN_x$ or $SiO_x$ are the most common dielectric materials for TFTs. These films are different from their corresponding LPCVD films in several ways, e.g., the hydrogen content, the adjustable stress, and the variable component ratios. These characteristics affect their wet and dry etch rates. Both a high etch rate and a high etch selectivity between the dielectric and the a-Si:H layer are required. Several papers dealing with factors affecting the $SiN_x$ RIE etch rate have been published [10–12]. In the $SiN_x$ etch, surface reactions involve the removal of both Si and N. Si usually forms volatile products, such as $SiF_x$, which are easily removed from the surface. In the $SiO_2$ plasma etch, it is well known that a carbon source is needed to remove the O component in the film, and that $CF_x$ radicals are major suppliers of the surface carbon. Since CN is a known gas-phase component in the $SiN_x$ plasma etch process, it is very possible that $CF_x$ radicals are effective etchants for $SiN_x$. Under the same process conditions, the $SiN_x$ etch rate decreases in the order of $CF_4 > CF_3Cl \sim C_2F_6 > CF_2Cl_2$. The etch rate in the $CF_4$ plasma is an order of magnitude higher than the others. Both the plasma-phase etchant (e.g., F and $CF_x$) concentrations and surface reactions contribute to the etch mechanism. In the $C_2F_6$ plasma, ion bombardment energy determines the etch rate; this means that surface reactions control the etch rate. These reactions have nothing to do with the surface hindrance layer formation, because no surface carbon residue is detected on the $C_2F_6$ etched surface. The addition of $O_2$ into $CF_2Cl_2$ increases the $SiN_x$ etch rate consistently. For high $O_2$ concentrations, e.g., 80%, the etch rate is an order of magnitude higher than that without $O_2$. Both the effective etchant concentrations and the ion bombardment energy of the plasma are enhanced by the existence of $O_2$, and both have a direct impact on the $SiN_x$ etch rate. The plasma potential usually has to be measured with an intrusive method such as the Langmuir probe. We did not measure the plasma potential in our experiments. The RIE reactor in these experiments has an anode-to-cathode area ratio of about 1.5. On the basis of a first-order estimation, the potential drop from the plasma to each electrode is inversely proportional to the area ratio to the fourth power. The potential drop to the cathode is about 5.1 times that to the grounded anode; the absolute value of the cathode self-bias voltage is higher than that of the plasma potential. In this case, therefore, the plasma potential is not a major contributor to the ion bombardment energy. The $CF_4$ plasma supplies a high etch rate ratio of $SiN_x$ to a-Si:H. The etch ratio increases with a decrease of the self-bias voltage. In the low self-bias voltage range, the ratio varies drastically with process parameters such as pressure [11]. This indicates that the etch ratio is controlled more by the plasma-phase chemistry than by the ion bombardment energy. A high selectivity is especially important in the opening of the source/drain vias, where the a-Si:H should be etched to the minimum extent possible.

Other common dielectrics in the TFT applications are metal oxides such as $Ta_2O_5$ and $Al_2O_3$. These oxides are usually used in combination with $SiN_x$ to form the gate dielectric structure. They have a high dielectric constant and are vulnerable to chemical attacks. During the etch of the top passivation and the a-Si:H layers, these metal oxides are not attacked by the etchants. Therefore, the probability of a top-to-bottom metal short is greatly reduced with the use of a metal oxide gate dielectric layer. In some applications the metal oxide must be selectively etched with minimum attack of the gate metal. For example, when tantalum is used as the gate metal, $Ta_2O_5$ can be formed by an anodization process. The $Ta_2O_5$ film must be etched off to expose the tantalum gate for the gate contact formation. It is difficult to find a suitable wet chemistry for this application.

**Figure 3** shows the tantalum and $Ta_2O_5$ etch rates as functions of the feeding gas composition. In a $CH_3F/CF_3Cl$ mixture, the Ta etch rate increases drastically with the $CF_3Cl$ concentration. In the $CH_3F/CF_3Cl$ plasma, the self-bias voltage decreases with the increase of the $CF_3Cl$ concentration in the range of 10–40%. However, the Ta etch rate increases with the $CF_3Cl$ concentration. When $CF_3Cl$ is replaced with $CF_4$, the Ta etch rate decreases. It has been proved [10] that under the same self-bias voltage, pressure, and flow rate, the F concentration in the $CF_4$ plasma is higher than that in the $CF_3Cl$ plasma. These relations are similar to those in the etch of a-Si:H. We conclude that Cl is a more effective etchant for Ta than is F. The competitive reactions between F and Cl for etch sites must be determined from very delicate surface-

analysis techniques which are not discussed in this paper. Compared with the Ta etch rate in the pure $CF_3Cl$ plasma, the etch rate is lowered by the $CH_3F$ gas [9]. The Ta etch is probably related to the Cl concentration in the plasma phase when there is no surface hindrance, such as the formation of carbides or polymers. The $Ta_2O_5$ etch rate first increases with $CF_3Cl$ concentration and then is independent of the $CF_3Cl$ concentration. If the plasma etching phenomena on the Ta and $Ta_2O_5$ surfaces are similar to those on the silicon and $SiO_2$, the probability of hindrance formation on the $Ta_2O_5$ surface is much lower than that for the Ta surface. The constant $Ta_2O_5$ etch rate in the high $CF_3Cl$ concentration region suggests that the $Ta_2O_5$ etch is limited by the supply of the effective etchants. If we apply the same etching principle of $SiO_2$ to $Ta_2O_5$, $CF_x$ radicals should be effective etchants, because they can form volatile products with Ta and O in the film. It has been proved that under the same power, the $Ta_2O_5$ etch rate is of the order of $CF_4 > CH_3F > CF_3Cl$ [13]. Therefore, F is more important than Cl in the etch of $Ta_2O_5$. Figure 3 shows that the $Ta_2O_5$-to-Ta etch rate ratio is greater than 1 when the $CF_3Cl$ concentration is below 25%. At a higher concentration, the ratio is less than 1. When the $CF_3Cl$ is replaced by $CF_4$ in the $CH_3F$ mixture, the $Ta_2O_5$-to-Ta etch ratio is always greater than 1. Both etch rates are lower than corresponding rates in the $CF_3Cl$ plasmas. In a separate experiment, a similar result has been found; i.e., a high $Ta_2O_5$-to-Ta etch selectivity has been achieved with a plasma containing an appropriate number of hydrogen and fluorine radicals [13].

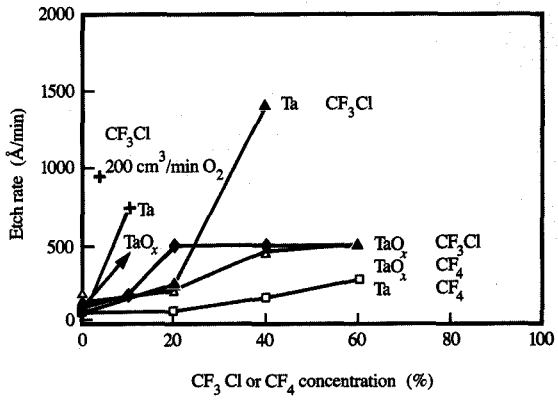


**Figure 3**

Tantalum and tantalum oxide etch rates vs. $CF_3Cl$ or $CF_4$ concentration in the mixture $CH_3F$ + $CF_3Cl$ or $CF_4$ at a total flow rate of 100 $cm^3$/min, at 100 mTorr, 2300 W, 20°C.

- *a-Si:H etch*

There are two kinds of a-Si:H films used in a TFT: intrinsic a-Si:H, used as a device active island, and heavily doped $n^+$ a-Si:H, used to form an ohmic contact layer to source and drain. For a-Si:H, a high etch selectivity to $SiN_x$ is required. For $n^+$, a high selectivity to the intrinsic a-Si:H or a high selectivity to $SiN_x$, depending on the device structure, is required.

There are two kinds of differences between a-Si:H and crystalline silicon: chemical and physical. The chemical composition difference is primarily the hydrogen content. The a-Si:H film reported in this paper contains more than 15% hydrogen. Both single-crystal and polycrystalline silicon contain much less hydrogen, usually less than a few percent. If hydrogen is released from a-Si:H during RIE, it may enhance the surface polymer formation in the fluorocarbon plasma, slowing down the a-Si:H etch rate. The large amount of hydrogen in the a-Si:H film occupies available Si bonds. The network of the a-Si:H film is composed of fewer Si–Si bonds than that of crystalline silicon. To remove one Si atom from the film during the etch, we must break four Si–Si bonds for crystalline silicon, but less than four bonds for a-Si:H. This enhances the a-Si:H etch rate. The difference in morphology between these two types of silicon is not important in the RIE process, because the surface is rendered amorphous by the ion bombardment. The resistivity of intrinsic single-crystal silicon is constant, i.e., $2.3 \times 10^5$ Ω-cm. The resistivity of intrinsic a-Si:H depends on the deposition condition, which is between $10^9$ and $10^{11}$ Ω-cm for a good-quality film [14]. The conductivity affects the silicon etch rate only when it is so heavily doped that surface electrical properties, such as the Fermi level and the electron transfer characteristics, are changed [15, 16]. Since plasma etching is a chemical process, surface reactions constitute one of the key steps. Therefore, chemical compositions, such as hydrogen content, are more important than the electrical conductivity and the morphology in the RIE of intrinsic silicons. Experimental results show that under the same RIE conditions, the a-Si:H etch rate is slightly higher than that for single-crystal silicon [17]. For the a-Si:H film, under the same process conditions, its RIE etch rate decreases in the order of $CF_4 \sim CF_3Cl > CF_2Cl_2 > C_2F_6 > CHF_3$ [10]. However, because the cathode self-bias voltage with these gases present decreases with an increase in the Cl content, the a-Si:H etch rate actually increases with an increase of the chlorine content under the same ion bombardment energy. The enhancement of the a-Si:H etch rate with the addition of chlorine can be hindered by the presence of hydrogen. For example, in the $CF_2Cl_2$/HCl plasma, the a-Si:H etch rate does not increase with the HCl concentration, although the ion bombardment energy increases [12]. The addition of $O_2$ into the $CF_{4-x}Cl_x$ freon

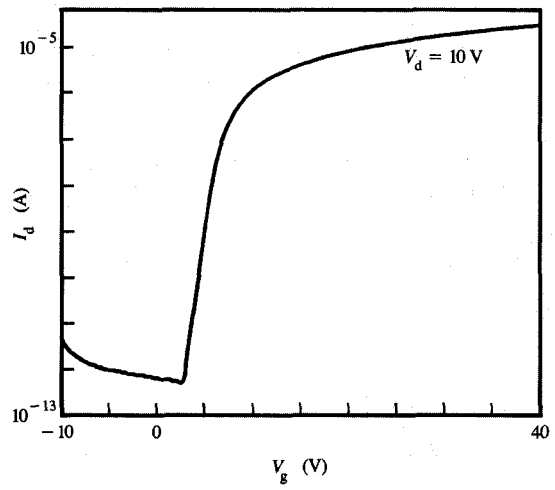


**Figure 4**

$I_d$–$V_g$ curve of a two-photomask, self-aligned, trilayer TFT; $L$ = 37 $\mu$m, $W$ = 60 $\mu$m, $\mu_{fe}$ = 1.05 cm$^2$/V-s, $V_t$ = 2.74 V.

gases increases the a-Si:H etch rate because of the increase in etchant concentration and ion bombardment energy as well as the removal of surface carbon [12]. The etch rate ratio of a-Si:H to $SiN_x$ increases with the chlorine concentration in the plasma. The ratio decreases with the introduction of $O_2$ into the plasma, indicating that ion bombardment enhancement is less selective than chemical reaction. The ratio is always greater than 1.5 in $CF_2Cl_2/O_2$ plasmas.

In a wet KOH $n^+$ etch process, a conductive residue is intermittently left on the $SiN_x$ surface after the etch. This residue is difficult to remove without damaging the device. It has been shown that a RIE process can be used to etch the $n^+$ effectively from the $SiN_x$ surface [18]. An etch rate ratio greater than 10 has been achieved with the pure $CF_2Cl_2$ plasma [19]. The ratio increases with the chlorine content and the pressure. To obtain a high ratio, a high-chlorine-content plasma with a low ion bombardment energy must be used. The $SiN_x$ film is damaged by an extended exposure to the $CF_3Cl$ plasma. The surface damage is limited to the top 60 Å, which forms an oxynitride dielectric layer after exposure to the air. No current leakage has been detected through the damaged layer, although bulk damage has been detected on an extensively etched $SiN_x$ film with ESR. There is a threshold period of several minutes before the ESR difference can be detected [20].

In the bilayer TFT structure, a selective etch of $n^+$ from the intrinsic a-Si:H is required. This is difficult to achieve with a wet etching method or a plasma etching method with fluorine-type chemistry [21]. It has been shown that an etch rate ratio higher than 1.7 can be achieved with $CF_3Cl$ or $CF_2Cl_2$ plasma [20]. Chlorine radicals are responsible for the selectivity. The electrical property difference between these two films, rather than the chemical composition difference, affects the electron transfer process from the substrate to the adsorbed chlorine during the etch, which contributes to the etch rate difference [16].

- *TFTs prepared with RIE processes*

The transfer characteristics of a two-photomask, self-aligned, trilayer TFT are shown in **Figure 4**. A detailed description of the process can be found in [22, 23]. The molybdenum gate was reactive ion etched with $CF_4$ 50 cm$^3$/min/$O_2$ 50 cm$^3$/min, 50 mTorr, and 500 W. The $n^+$ layer was etched with a $CF_2Cl_2$ 80 cm$^3$/min/$O_2$ 20 cm$^3$/min plasma. The trilayer is composed of gate $SiN_x$ 1200 Å / a-Si:H 350 Å/$SiN_x$ 2200 Å. The $n^+$ layer is 600 Å thick. The channel length is 37 $\mu$m, and the channel width is 60 $\mu$m. The TFT had a saturation mobility of 1.05 cm$^2$/V-s and a threshold voltage of 2.74 V, estimated on the basis of the following equation:

$$I_{ds} = 1/2\mu(W/L)C(V_g - V_{th})^2,$$

where $I_{ds}$ is the drain current, $\mu$ is the field-effect mobility, $W$ is the channel width, $L$ is the channel length, $C$ is the capacitance of the gate dielectric, $V_g$ is the gate voltage, and $V_{th}$ is the threshold voltage.

## Conclusion

RIE processes useful in preparing TFTs were reviewed in this paper. In preparing the gate pattern, the RIE process can supply a sloped molybdenum or tantalum wall by properly adjusting the $O_2$ concentration in $CF_4$ gas. Plasma attack of Corning 7059 glass during the sloping process is negligible. $SiN_x$ dielectric can be etched at a high rate and with a reasonable selectivity to a-Si:H with a $CF_4$ plasma. A selective etch of $Ta_2O_5$ from Ta has been achieved with a $CH_3F/CF_4$ plasma; it is difficult to get good selectivity with a chlorine-containing plasma. Both intrinsic and $n^+$ a-Si:H layers can be effectively etched with $CF_{4-x}Cl_x$ plasmas. The etch rate increases with $x$ under the same self-bias voltage. The a-Si:H-to-$SiN_x$ etch rate ratio also increases with $x$. The existence of hydrogen, originated from HCl, hinders the chlorine effect on the etch rate and the etch ratio, although the ion bombardment energy is increased. The addition of $O_2$ can increase the etch rate, but not the selectivity. A selective $n^+$-to-a-Si:H etching process can be obtained with the $CF_3Cl$ or $CF_2Cl_2$ plasma. A two-photomask, self-aligned, trilayer TFT has been

prepared with RIE processes applied to slope-etch the molybdenum gate and to selectively etch $n^+$ from the top $SiN_x$. The device characteristics are as good as those prepared with wet etching methods.


## Acknowledgment

The author would like to acknowledge C. Burstell and P. Fryer for the deposition of metals and $Ta_2O_5$ films and P. Wagner for the deposition of PECVD films.


## References


1. Y. Kuo, "Thin Film Technologies in Active Matrix Addressing System of LCDs," *SPIE Proc. Display Syst. Opt. II* **1117**, 114–122 (1989).
2. T. Matsumoto, M. Hayama, N. Nakagawa, H. Sakamoto, K. Kobayashi, H. Takasago, and T. Yamazaki, "5 & 10 Diagonal Color AM-LCD Addressed by a-Si TFTs Using Precisely Controlled Fabrication Processes," *Conference Record, International Display Research Conference*, IEEE, Society for Information Display, and Advisory Group on Electron Devices, San Diego, CA, October 4–6, 1988, pp. 65–69.
3. M. Ikeda, M. Ogawa, and K. Suzuki, "Low Resistance Copper Address Line for TFT-LCD," *Proceedings of Japan Display '89*, 1989, pp. 498–501.
4. Y. Kuo and J. R. Crowe, "Slope Control of Molybdenum Lines Etched with RIE," *J. Vac. Sci. Technol.* **8**, 1529–1532 (1990).
5. Y. Kuo, "Factors Affecting the Molybdenum Line Slope by Reactive Ion Etching," *J. Electrochem. Soc.* **137**, 1907–1911 (1990).
6. A. Picard and G. Turban, "Plasma Etching of Refractory Metals (W, Mo, Ta) and Silicon in $SF_6$–$O_2$—An Analysis of the Reaction Products," *Plasma Chem. Plasma Process.* **5**, 333–351 (1985).
7. D. Thomson and C. R. Helms, "Studies of the Etching of Si, $SiO_2$ and Mo by Carbon Fluorine Compounds Using Real Time Auger Spectroscopy," *ECS Ext. Abstr.* **84**, 508 (1984).
8. Y. Kuo, "Reactive Ion Etch of Sputter Deposited Tantalum—Process and Mechanisms," *ECS Ext. Abstr.* **91**, 677–678 (1991).
9. Y. Kuo, "Reactive Ion Etching of a Multicomponent Glass Substrate," *SPIE Proc.* **945**, 103–108 (1988).
10. Y. Kuo, "Reactive Ion Etching Selectivity of PECVD Silicon to Silicon Nitride—Feeding Gas Effects," *J. Vac. Sci. Technol.* **8**, 1702–1705 (1990).
11. Y. Kuo, "Reactive Ion Etching of PECVD Amorphous Silicon and Silicon Nitride Thin Films with Fluorocarbon Gases," *J. Electrochem. Soc.* **137**, 1235–1239 (1990).
12. Y. Kuo, "The Role of Oxygen in the $CF_2Cl_2$ Reactive Ion Etching of PECVD Films," *MRS Proc.* **223**, 249–254 (1991).
13. Y. Kuo, "Reactive Ion Etching of Sputter Deposited Tantalum Oxide and Its Etch Selectivity to Tantalum," *J. Electrochem. Soc.* **139**, 579–583 (1992).
14. V. Augelli, "Conductivity of Undoped GD a-Si:H," *Properties of Amorphous Silicon*, 2nd Ed., INSPEC Publications, New York, 1989, pp. 185–190.
15. G. C. Schwartz and P. M. Schaible, "Reactive Ion Etching of Silicon," *J. Vac. Sci. Technol.* **16**, 410–413 (1979).
16. C. J. Mogab and H. J. Levinstein, "Anisotropic Plasma Etching of Polysilicon," *J. Vac. Sci. Technol.* **17**, 721–730 (1980).
17. Y. Kuo, "Reactive Ion Etching of PECVD Amorphous Silicon and (100) Crystalline Silicon with $CF_4$ and $CF_3Cl$ Gases," *ECS Ext. Abstr.* **89**, 300–302 (1989).
18. Y. Kuo, "Reactive Ion Etching of PECVD $n^+$ a-Si:H and Silicon Nitride—Selectivity and Plasma Damage," *ECS Ext. Abstr.* **90**, 158–159 (1990).
19. Y. Kuo and M. S. Crowder, "Reactive Ion Etching of $n^+$ a-Si:H. Plasma Damage to PECVD Silicon Nitride Film and Application to Thin Film Transistor Preparation," *J. Electrochem. Soc.* **139**, 548–552 (1992).
20. Y. Kuo and M. S. Crowder, "Reactive Ion Etching of PECVD $n^+$ a-Si:H and Plasma Damage to PECVD Silicon Nitride Film," *Proc. ECS 8th Plasma Processing Conf.* (G. S. Mathad and D. W. Hess, Eds.) **90**, 324–334 (1990).
21. I. Haller, Y. H. Lee, J. J. Nocera, Jr., and M. A. Jaso, "Selective Wet and Dry Etching of Hydrogenated Amorphous Silicon and Related Materials," *J. Electrochem. Soc.* **135**, 2042–2045 (1988).
22. Y. Kuo, "A New Process Using Two Masks to Prepare Tri-Layer Thin Film Transistors," *J. Electrochem. Soc.* **138**, 637–638 (1991).
23. Y. Kuo, "A New Thin Film Transistor Structure and Its Processing Method for Liquid Crystal Displays," *SPIE Proc.* **1456**, 288–299 (1991).



*Received July 25, 1991; accepted for publication December 15, 1991*



**Yue Kuo** *IBM Research Division, Thomas J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598 (YKUO at YKTVMV, ykuo@watson.ibm.com).* Dr. Kuo received his B.S. in chemical engineering from the National Taiwan University in 1974. He received his M.S. and Ph.D. degrees, both in chemical engineering, from Columbia University in 1978 and 1979, respectively. He joined IBM in 1987, and has since worked on thin-film transistor process technology. Dr. Kuo is a senior member of the Institute of Electrical and Electronics Engineers, the Electrochemical Society, the International Society for Optical Engineering, the Materials Research Society, and the Society for Information Display.