Functional testing of TFT/LCD arrays

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The thin-film-transistor liquid crystal display (TFT/LCD) is emerging as the leading flat-panel display in computer applications. TFT array characterization is important to the research, development, and manufacturing of TFT/LCDs. This paper describes a new Dynamic Array Tester developed for that purpose and describes some examples of its use.

Introduction

Of all the flat-panel technologies, only the TFT/LCD is expected to pose a serious challenge to the cathode ray tube [1]. TFT/LCD prototypes have already demonstrated full color capability, a requirement of high-information-content displays. TFT/LCDs also have an inherent immunity to high ambient light levels while operating at low levels of power consumption, a characteristic not shared by electroluminescent or plasma displays. Many companies have recognized the advantages of the TFT/LCD, and the total investment in this technology is now approaching two billion dollars [2].

TFT/LCD technology shares many similarities with silicon integrated circuit technology, such as dynamic random access memories (DRAMs). Both involve film deposition, although TFT/LCD technologies employ lower-temperature processing. In both, photolithography and etching are used to pattern each level. Both structures employ random addressing capability. Many characterization and yield management techniques are also applicable to both. The operating mode of a TFT/LCD is not digital, however, but analog, because the light output varies as a smooth function of the voltage stored [3]. Therefore, functional testing of TFT/LCDs is much different, as will be seen.

There is growing interest in testing and repair techniques for these displays [4–8]. We have developed a Dynamic Array Tester that characterizes TFT arrays. The Dynamic Array Tester can detect, locate, and grade both line faults and pixel faults in a TFT array. It can be used as an in-line manufacturing screen to sort product into pass, fail, or repair categories, and this sorting can be done immediately after the arrays have been fabricated and again after the display has been filled with liquid crystal. It can also be used to verify array designs and perform failure analysis.

Thin-film-transistor (TFT) arrays

A display device generally consists of a two-dimensional array of individually controlled picture elements (pixels). In an active-matrix thin-film-transistor liquid crystal display (AM TFT/LCD), there is one set of horizontal metal lines and, on another plane, a second set of vertical metal lines. At an individual pixel the gate line is connected to the gate of a thin-film transistor (TFT), and the data line is connected to one of its source/drain terminals (see **Figure 1**). The other source/drain terminal is

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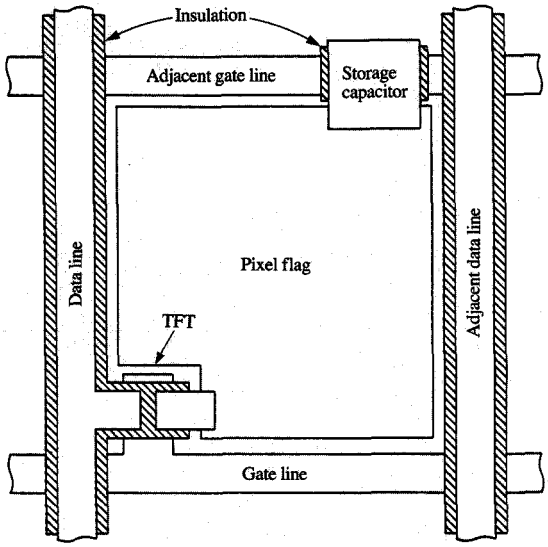

Figure 1

Example of a pixel layout. Here the adjacent gate line is used as the storage capacitor counter electrode. Some designs use a separate line for this purpose.

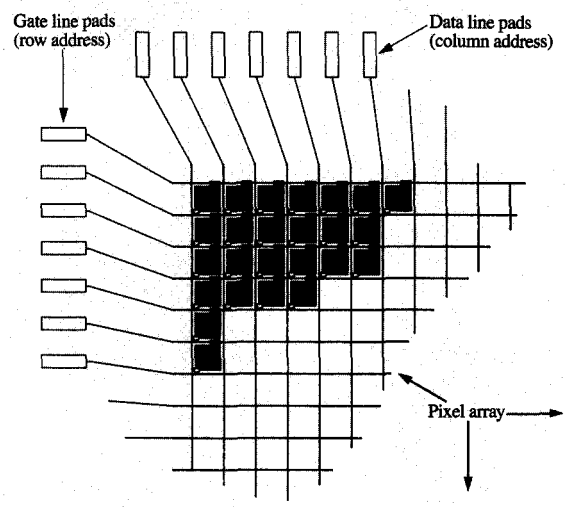

Figure 2

Magnified view of the upper left corner of a TFT/LCD backplate. Pixel centers vary around 0.2 mm, line widths around 0.02 mm. The topmost gate line is used only as a counter electrode for C_S.

connected to a transparent conductor, sometimes called a flag because of its shape, that is isolated from the surrounding pixels and serves as one electrode of a capacitor. The two-dimensional array described above is fabricated on a glass substrate (back-plate) and is called the TFT array.

On a second piece of glass (front-plate), there exists a blanket layer of transparent conductor that serves as the other electrode for all the pixel capacitors. For a color display, this second piece of glass also contains a repetitive pattern of red, blue, and green filters, with one filter positioned over each pixel and separated from the others by a black matrix. The triad combination of a red, a blue, and a green pixel is called a color pixel. The two pieces of glass are aligned and cemented together with spacers (several μm thick), with a liquid crystal between them. Finally, linear polarizers are added to the outer surfaces of each piece of glass.

The pixels are controlled by applying a voltage to a selected horizontal (or gate) line and to a vertical (or data) line. In normal operation a selected pixel must sample the potential present on its associated data line at a time determined by its associated gate line pulse. This pulse switches the TFT to the ON state briefly. While ON, the liquid crystal pixel flag potential becomes equal to that of the data line. When the TFT returns to the OFF state, there remains a potential on the flag which affects the optical transmission of the pixel, as intended by the display system. The pixel must now retain this potential one frame time until it is refreshed by the next gate pulse. Voltage placed on the capacitor controls the rotation of linearly polarized light through the twisted nematic (TN) liquid crystal, so that each pixel is now an electro-optical element that modulates the amount of light from an areally uniform backlight.

Fabrication of the TFT array on the first piece of glass is similar to the processing of integrated circuits on silicon chips, although the dimensions involved are much larger. In fact, the TFT array closely resembles the array portion of a DRAM chip, since a storage capacitor is often fabricated on the TFT array to provide more charge storage at each pixel and to reduce some of the nonlinear effects of the liquid crystal capacitor. Consequently, the TFT array can be represented by **Figure 2**, where each element consists of storage capacitors randomly addressed through a TFT access device.

Like a DRAM chip, the TFT array is a good in-line test vehicle. It can be used to qualify a new processing technology. It is possible to make rapid quantitative measurements under operational conditions that detect and locate yield detractors; in this capacity, the TFT array is an excellent yield-management tool.

There are multiple benefits to be gained from testing TFT arrays. In-line testing of unfilled TFT arrays in a

manufacturing environment saves millions of dollars because faulty arrays are repaired or scrapped before incurring the expense of color filter and black matrix fabrication, glass assembly, liquid crystal filling, line drivers, and driver assembly. A second opportunity for in-line testing exists after glass assembly and filling but before drivers are attached. When the backlight is in place, front-of-screen testing can be performed simultaneously with array testing.

Array testing can also benefit failure analysis. Line and pixel faults are readily detected and catalogued by test software. Tester analysis of line and pixel integrity can identify the nature and location of a fault, and additional diagnostic tests can be used for probing further. Failure analysis is an important component of yield management, since early identification of yield detractors reduces cost and focuses attention on the relevant processing sector.

Data from normally behaving pixels are also helpful in characterizing new array designs. The Dynamic Array Tester measures pixel charging and leakage behavior as well as the gate threshold and transconductance of the pixel TFT. It is able to determine gate line delay and sensitivity to the pulse parameters associated with display operation.

Thus, the TFT array provides an exceptional opportunity to verify designs during development, to save money and manage yield in manufacturing, and to facilitate failure analysis. What is needed to take advantage of this opportunity, of course, is an array-testing machine.

Sensing charge

Each pixel consists of a sample and hold circuit, as shown in **Figure 3**. The flag is represented as a capacitor C_F, which may have a value in the range 50 to 250 fF. C_F actually consists of parallel components, including a fabricated storage capacitor C_S, and the flag parasitic capacitance to the surrounding data and gate lines, and, for a filled display, a liquid crystal capacitance C_{LC}. The TFT has associated gate-to-drain and gate-to-source capacitances C_{GD} and C_{GS}.

Each pixel must meet minimum requirements for acceptable display quality. When the TFT is ON, the resistance must be small enough to conduct sufficient current in the time allotted. When it is OFF, the resistance must be large enough to prevent significant leakage from flag to data line. C_S leakage must be low so that the charge is retained for the entire frame time.

In addition, each line must meet minimum requirements. If there is an erroneous potential on all or part of a data line, a vertical line defect will appear. A gate line error causes a horizontal line defect. These errors can be caused by line discontinuities, crossing shorts, or adjacent line shorts. Variations of TFT performance, either localized or widely distributed, will cause a corresponding degradation

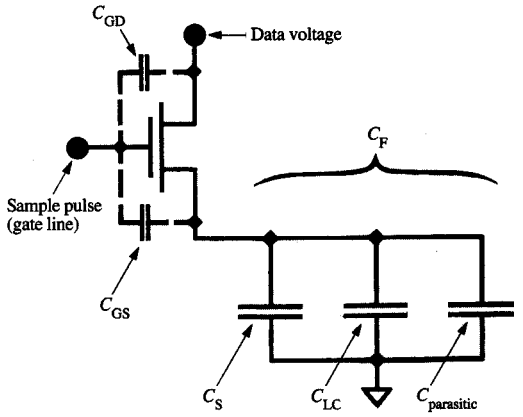

Figure 3

Simplified equivalent circuit of a pixel.

of image quality. How wide these variations are within each back-plate determines its ultimate disposition, i.e., finished display or trash bin. A TFT/LCD flat-panel display tester must detect the presence of the majority of these pixel and line defects if it is to be of value to the designer or manufacturer.

Since each pixel is a sample and hold device within an addressable array, it can be exercised as an analog data storage device before or after the front-plate is attached and filled with liquid crystal. Also, its stored data can be retrieved, given the correct sequence of write and read excitation and connection of a suitable detection device. When an unfilled plate is tested, the liquid crystal capacitance C_{LC} is absent, and less charge will be written for a given data voltage. An apparatus which can address, write, and read analog charge within a display array has the potential to fully test that display. This is the fundamental principle of the Dynamic Array Tester.

Now consider the read function of such a tester. The TFT device is one in which the channel is OFF unless the gate voltage exceeds some positive threshold V_T above either of the other terminals, that is, V_D or V_F. For convenience, let us say that the inactive, or hold, state of the pixel occurs when $V_D = V_G = 0$ V. Suppose a charge previously written now resides on the flag terminal as a positive voltage. The best way to remove all the charge from the pixel is to raise the gate while holding the data line at 0 V. An operational amplifier configured as an integrator is useful in holding the data line at 0 V while simultaneously collecting the charge Q across the terminals of the feedback capacitor C_I. **Figure 4** shows such a

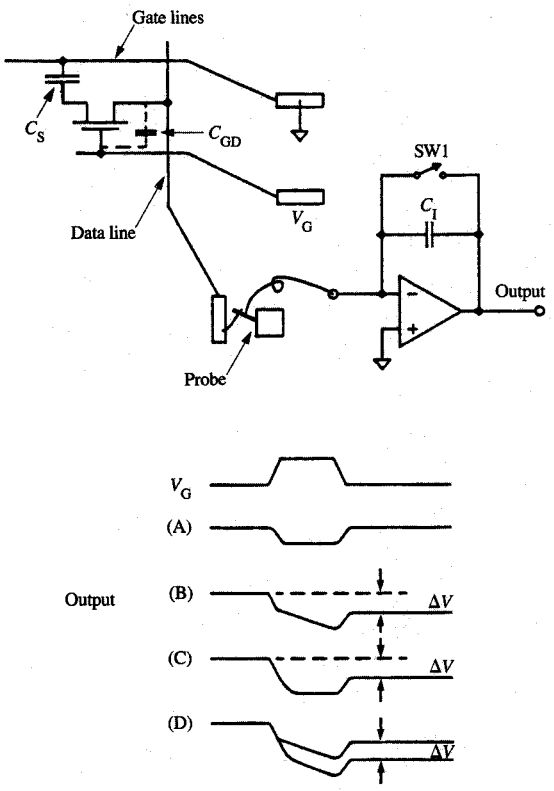

Figure 4

Basic sense circuit. An integrating operational amplifier collects charge from a selected pixel while holding the data line at 0 V. No charge is lost because the data line is at zero potential before and after the read operation. When no charge is stored on the pixel flag, the integrator response appears as in (A). Only the gate pulse is coupled through C_{GD}. Knowing the size of V_G and C_I, we can measure the magnitude of C_{GD}. In the case where leakage current is present between the data and gate lines, waveform (B) is seen. The slope during the gate pulse is proportional to $-1/R_{leak}$. If charge is present, the output appears as (C). The amount of charge is proportional to ΔV. Output (D) depicts an error-correction technique (see text).

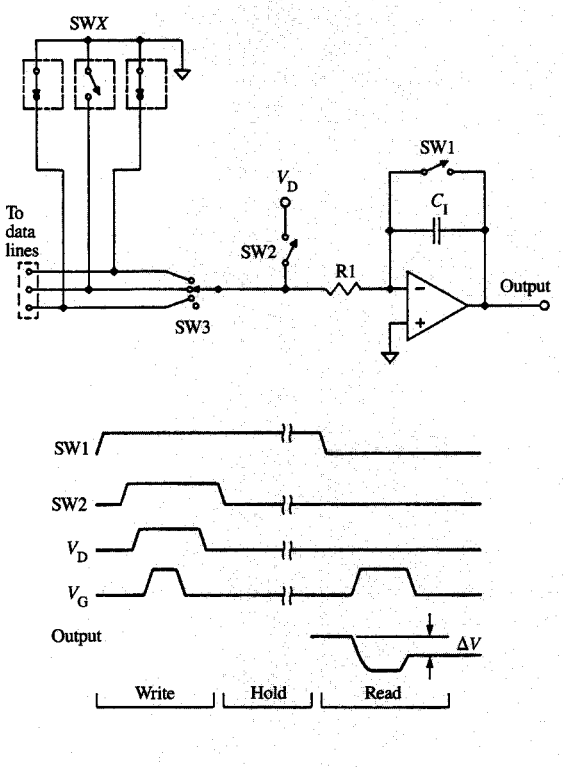

Figure 5

Switching added to the integrator. The timing diagram shows how the gate and data lines are pulsed in a standard write/read cycle. All pulse times and voltages are under software control.

circuit. Some minimum gate pulse width and voltage are required to fully transfer the charge. SW1 is used to reset the integrator to zero prior to the read operation. The output is $\Delta V_{OUT} = -(Q/C_I)$.

The more charge held in the pixel, the more negative the output will be after the gate pulse. Close examination of the output response vs. time reveals information regarding various qualities of the pixel. Examples given in Figure 4 show output responses to selected pixel conditions.

Output (C) in Figure 4 is an ideal waveform. Actually, leakage current paths may exist in a TFT array. This presents a problem in making charge measurements because leakage current changes the integrator waveform. Notice that both outputs (B) and (C) have a ΔV after the gate pulse, but one is from gate leakage and the other from transferred charge. The tester must be able to recognize charge transfer when such leakage currents are present. To solve this problem, two readings are taken: the first with charge written on the pixel, the second without. Data from these two conditions, when subtracted, reveal the difference voltage proportional to the charge [output (D)].

Anything which interferes with writing, reading, or holding charge will cause an unexpected output at the integrator. For example, if a gate or data line is not continuous, no pulse will be seen on the output. If there is a low-resistance short from data line to gate line, the output will go rapidly negative. Therefore, this method detects a variety of defects in TFT arrays at electronic speeds.

Writing charge

Having described a useful read circuit, we now discuss the method of placing charge on the pixel flag capacitance.

Figure 6

Closeup view of the Dynamic Array Tester used at the IBM Eastview Research Laboratory.

This is done by pulsing the data and gate lines to effect the same sample and hold function described above.

The addition of switches between the data line and integrator as shown in **Figure 5** provides control of data line voltage and timings. The switches are shown set to the read mode position. In write mode V_D is connected to the selected data line through SW2 and SW3. V_D can range from 0 to about 12 V. In write mode, resistor R1 limits input currents at the integrator. The output voltage is not used at this time. The selected data line follows the V_D terminal, while other lines are held to 0 V by the switches SW*X*. This is important because part of C_F consists of capacitance that is parasitic to the adjacent data line. It is also important to hold data lines that are not being tested to 0 V to provide a widely distributed ground system as a reference plane. Gate line selection and pulse generation are accomplished by adapting one of the commercially available display row drivers to the Dynamic Array Tester system.

The circuit described above is contained on a printed circuit card; sixteen of these sense/write cards can be seen in the foreground of **Figure 6**, which is a close-up view of a Dynamic Array Tester used at the IBM Eastview Research Laboratory. Another sixteen cards are located behind the probe assembly. Also visible in this picture are the flexible cables connecting the sense cards to the probe assembly and the ribbon cables connecting the gate line drivers and sense/write cards to the system card. A TFT array is shown on the holder, which is in the "unload" position.

Parameter extraction

Data gathered by systematic manipulation of test timings and voltages can be used to evaluate the response from a pixel under varied stimuli. Some of the pixel parameter extraction routines we have developed are discussed here. Refer to **Figure 7** for illustrations of these discussions.

We have discussed the analysis of various integrator output waveforms in determining the behavior of a pixel. Computer analysis requires that data collected be converted to digital form. For the case where the waveform of the integrator is to be analyzed, a set of data is collected by operating the pixel repeatedly under identical conditions while sampling the output voltage at a

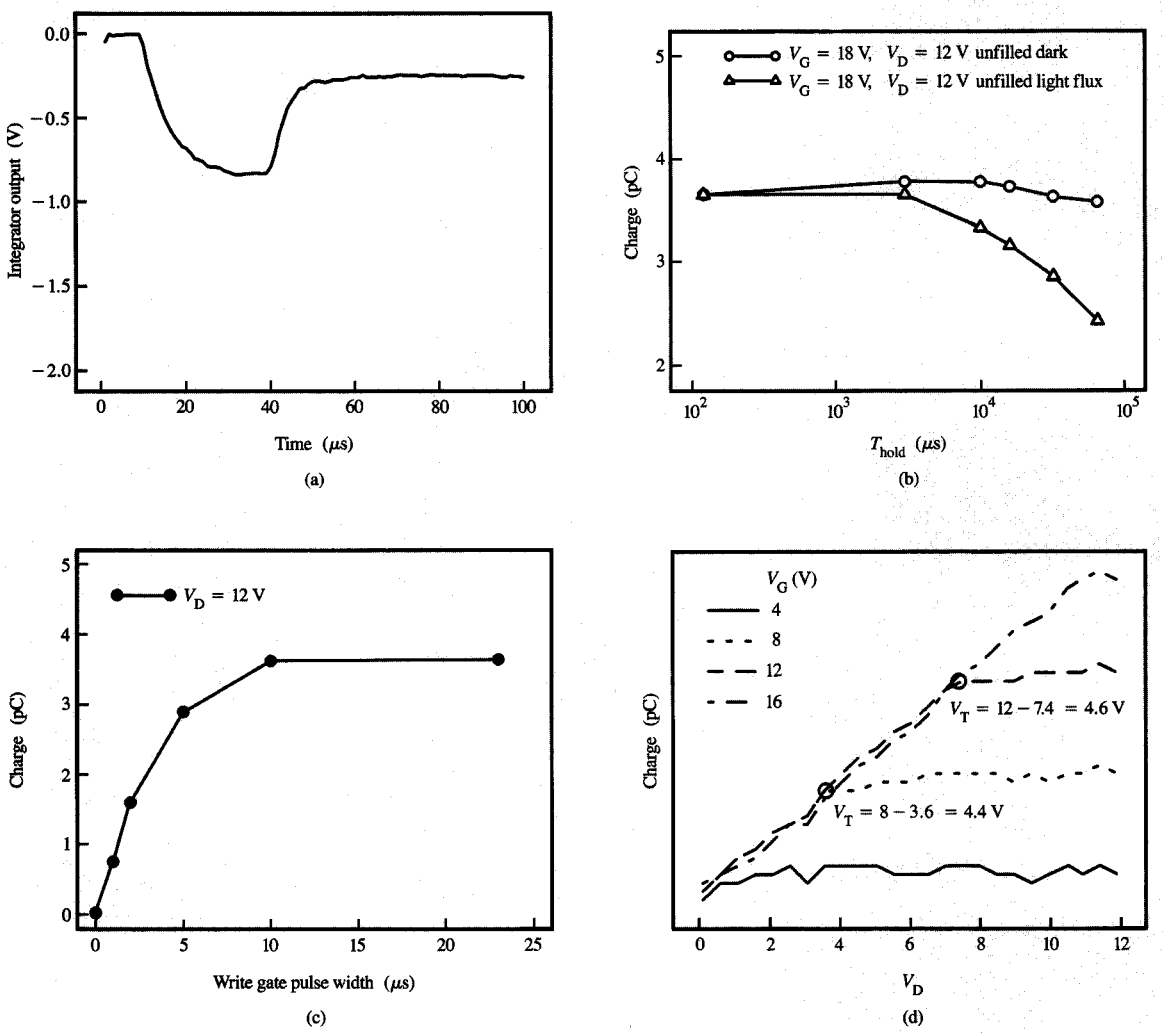

Figure 7

Several example pixel characteristics gathered by the Dynamic Array Tester: (a) Output waveform; (b) average charge vs. T_{hold}; (c) average charge vs. charge time; (d) cell charge-transfer response.

later time each cycle until all of the waveform is collected [Figure 7(a)]. Once the data have been collected by the computer, they can be analyzed for various qualities, and graphically displayed. Gate rise time, size of C_{GD}, and charge transferred can be determined by this data set.

A test of pixel charge vs. hold time (T_{hold}) entails operating a cell repeatedly until data have been collected for the range of hold times desired. When displayed graphically, the total effect of leakage currents is evident. When this is done before and after filling, the contribution made by the liquid crystal may be deduced. Figure 7(b) shows the influence of ambient room lighting on an unfilled back-plate.

Similarly, increasing the width of the write gate pulse from zero causes a corresponding increase of retained charge. The plot of this series [Figure 7(c)] clearly shows the time constant of the pixel circuit. Gate line rise-time degradation can be determined by examining cells at varying distances from the gate driver.

Another test is used to ascertain the relationship between stored charge and data line voltage under different gate voltages. Here V_D is varied while V_G is held at several

constant values. Figure 7(d) shows an example of this test, where V_T is estimated from the intersection of the slopes.

A test system

A complete test system provides an interface with an operator, performs test functions, analyzes data, and logs the results. **Figure 8** gives an overview of our system.

System control resides with an IBM PS/2® that is connected to the tester through a digital I/O board on the Micro Channel® bus. The hardware design of the Dynamic Array Tester provides control of most test conditions to the software. All test parameters, including row and column addresses, pulse timings, and voltage levels, are available for manipulation by the test program. As required by the various tests, conditions can be set for writing a pixel with a wide range of values. **Figure 9** shows an example of a complete test system. This system is currently in use for manufacturing line testing of VGA displays.

The tests that an operator would execute on the Dynamic Array Tester fall into two broad categories. In the first are standardized manufacturing line tests which

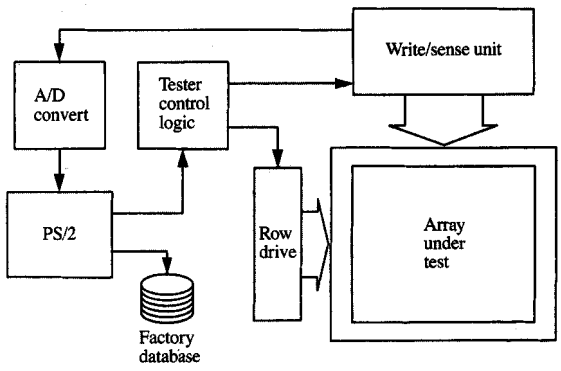

Figure 8

Dynamic Array Tester system. Test parameters for each array type are transmitted to the tester logic for execution. Data collected are analyzed and summarized by the PS/2 software. Repair, quality, and disposition data are stored in the database for use in later manufacturing steps.

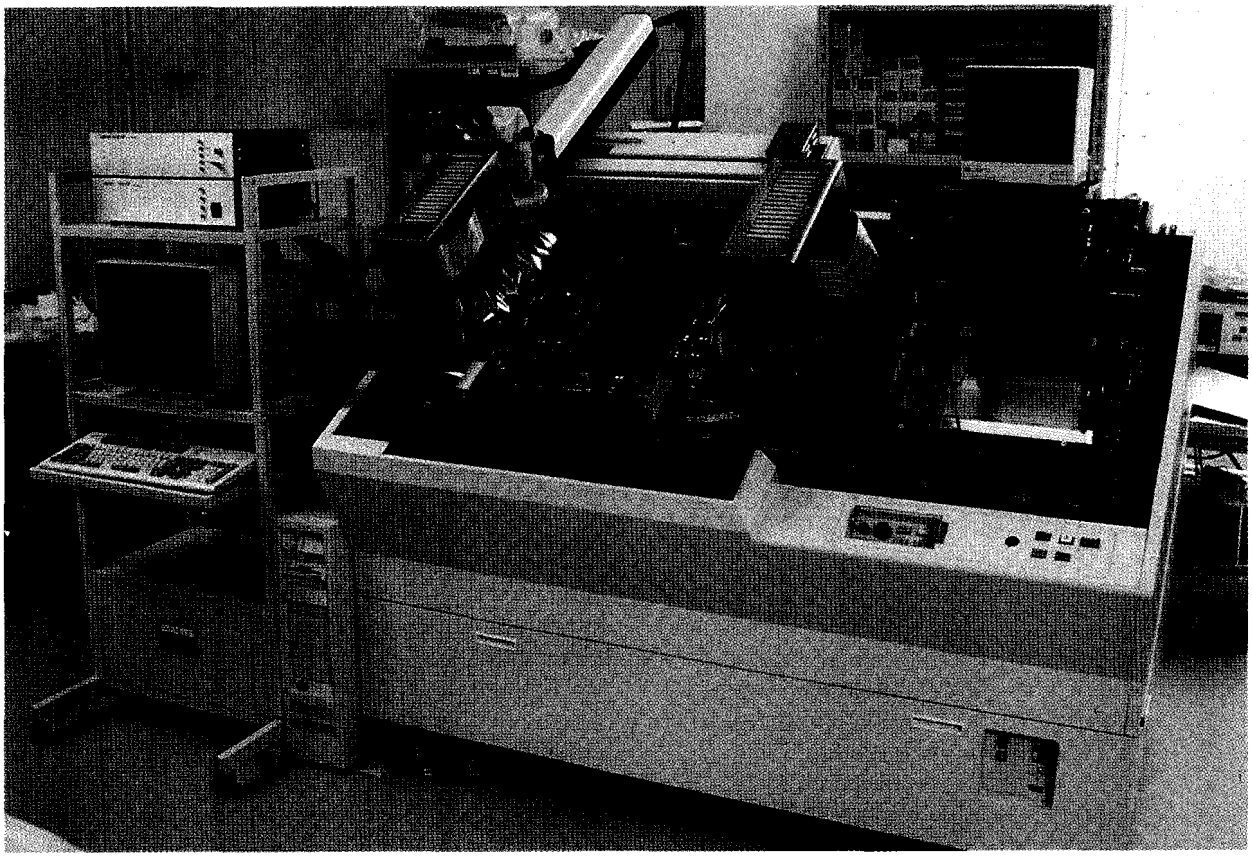

Figure 9

DTI Array Tester. This tester is used by Display Technologies Incorporated for testing arrays to be used in VGA displays.

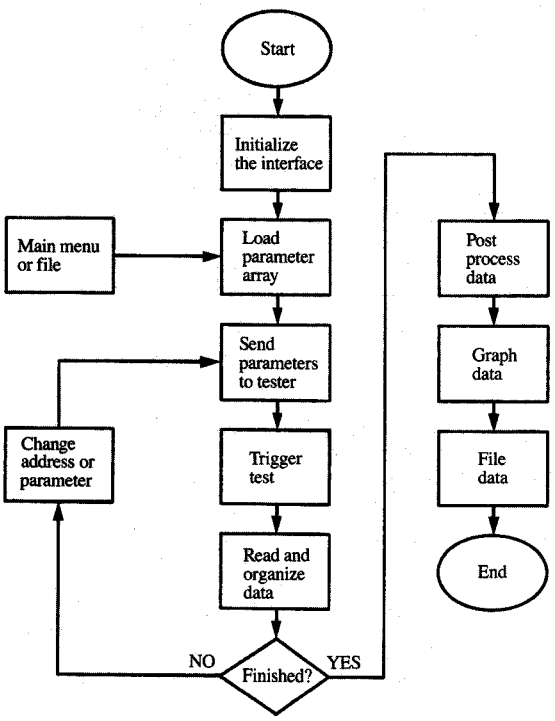

Figure 10

Test software flow diagram.

evaluate overall array quality and identify candidates for rejection or repair. These tests, because there is no variation from panel to panel, are run together as a batch job to give a consistent picture of array performance. These testing conditions are determined by a parameter file that is edited only to suit changes in display type. Once this file is established, the software runs the test series without operator intervention.

In the second category, the operator has control of all the functions and parameters, so that unique tests may be performed on any pixel. A menu of the test and control parameters is presented to the operator for verification or modification. This second category of tests is used by designers or failure analysis personnel who are looking for causes of design problems or array defects.

The flow of the typical program would follow the chart shown in **Figure 10**. The first task is to initialize the interface. Next, depending on the type of test, the parameters are input either from the operator's menu or from a parameter file. Voltages are then converted into values to be sent to digital-to-analog converters. At this point the program proceeds to one of two test loops. One of these is to address a particular pixel and then test that pixel repeatedly, changing only one parameter. For example, in the waveform test a pixel is tested with all conditions held constant while the sample time is stepped in small increments. In the second type of loop, all of the parameters remain fixed while the pixel addressed is changed.

While looping, the computer repeats the cycle of sending parameters to the tester, triggering a test, reading the analog-to-digital converters, and storing the data in a memory array. After exiting the loop, the software analyzes the data by looking for specific response signatures as described above. Defect locations are identified, and in some cases the results are graphically represented. This is of great value when pass/fail screening of a display is done, or when repairs are to be made. Defect data are sent with any panel for repair tool use. Bar charts and $X\,Y$ graphs can be automatically generated to show charging uniformity and transistor characteristics. Data are retained on disk for statistics, repair verification, and comparison with later tests, including final optical inspection.

Test system economy

We have discussed detection of line and pixel defects and characteristics at a single location. Testing an entire array in a manufacturing line environment, however, requires a strict protocol that will avoid error and shorten test cycles. The condition of lines, for example, must be known before pixel testing can begin, because they are the means of access to the array. To accomplish this, a screening test has been implemented to verify the quality of all lines for use in testing the array. This is done in two stages. First, gate line screening is done by looking for a correct gate pulse signature [Figure 4(a)] at two data lines, one near the driven end of the gate, the other at the far end. The gate line is good if the signature is present at both ends. If the signature is missing at either end, the gate line is broken in the middle or in the fan-in area, or the contact is failing. A failing line is flagged and becomes a candidate for defect isolation. Every gate is checked in this way, and a log of inoperable gate lines is generated. More detailed testing to pinpoint the location of gate defects for possible repair is done after the data lines are screened. When the number of defective lines exceeds an acceptable limit, the panel is immediately rejected, and testing is halted. Immediate termination of testing when the first defect limit is reached saves test resources.

The topmost and bottom-most working gates are used to evaluate all data lines by writing to every pixel along these two gate lines. The read waveform is examined for characteristic signatures. Every data line is placed in a quality category.

The NORMAL category data line has acceptable C_{GD} (as determined by the correct output step size at the fall of the gate pulse), has a stored charge of nominal value, and has gate line leakage within the acceptable limit. A check that these requirements are met at both ends verifies that the data line is continuous through the array. When a discontinuity is detected, it is logged for later testing in which the exact location of the defect is pinpointed.

Lines that do not fit the NORMAL category are further evaluated. A data line having no response at either end of the line is broken somewhere outside the array, such as in the region between the array and the I/O pads. A fast drop of the integrator output at the rise of the gate indicates a possible short. If the gate capacitance coupling is smaller than normal, there may be a short to the adjacent data line, which can be verified by further analysis.

After the quality of all gate and data lines is known, the entire array is scanned in a write/read operation to evaluate all pixels for shorts and charge retention. A map of the panel defects is analyzed for repair actions, if required, and a recommendation is made for disposition of this array. **Figure 11** shows an example of a defect location map in which the defects are identified.

Analyzing line and pixel performance in a manufacturing environment requires that integrator response data be obtained as rapidly as possible for reasons of efficiency. High-speed data conversion, increased data transfer bandwidth, and parallel sense operations help solve this problem. Also, only a few data points actually have to be collected to do the analyses of line quality, shorts, and charge retention. It is only during design verification or failure analysis that a large amount of data is collected on individual pixels.

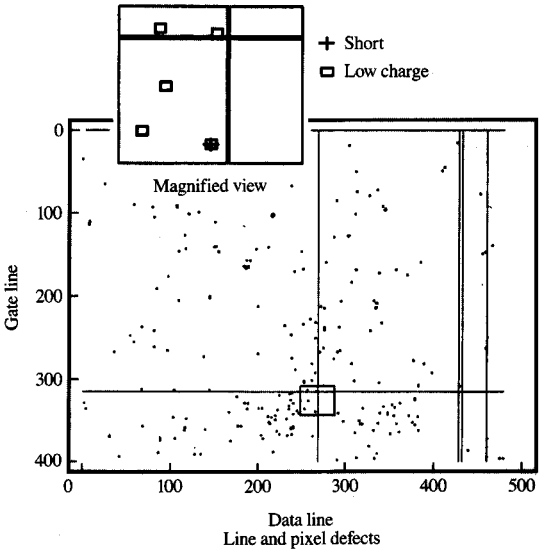

Figure 11

Sample defect map. Vertical and horizontal lines represent data line and gate line defects, respectively. The box shows a magnified view where the individual pixel defect is identified by type. This experimental plate is good for evaluating the test system, but clearly has too many defects for product use.

Summary

Use of a unique Dynamic Array Tester system is expected to reduce manufacturing costs substantially. Taking advantage of inherent topography, the Dynamic Array Tester directly exercises the active and passive elements of a TFT/LCD display array. Software control of test parameters yields a wide range of characteristic extraction capabilities. Use of the Dynamic Array Tester conserves materials and processing resources by avoiding continued fabrication of substandard parts. Detected faults can be evaluated for repairability, and rapid identification of yield detractors focuses attention on the relevant processing sector, hastening yield improvement. The Dynamic Array Tester also has a role as a technology development tool, providing quick feedback in process evaluations. Its employment in the laboratory and on the factory floor will substantially aid the advance of TFT/LCD products.

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