IBM Enterprise System/9000 Type 9121 system controller and memory subsystem design

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A system controller supporting two processors, two independent memory banks, and a channel subsystem has been implemented within a single air-cooled thermal conduction module for the IBM Enterprise System/9000™ Type 9121 processors. Improvements in technology densities, usage of CMOS and emitter-coupled logic on the same substrate, and innovations in the system controller design were required to achieve the one-module objective. In addition, system reliability is improved with a storage key error-correction code, and storage allocation options are increased with a combined main/expanded store design. In conjunction with the system controller development, a new memory subsystem has been designed for the 9121 system. Innovative large-system memory packaging techniques and functional changes in the data accessing methods have culminated in a memory board which supports up to one-gigabyte system storage.

Introduction

This paper highlights the innovations of the IBM Enterprise System/9000™ (ES/9000™) Type 9121 system controller (SC) and memory subsystems. Discussion of these innovations will sometimes require comparisons with previous machines; in general, the SC and memory subsystems of the Enterprise System/3090™ (ES/3090™) [1] serve as the base for these comparisons. The 9121 system exploits an improved chip technology which offers increased circuit density and permits two families of bipolar circuits on the same chip: differential current switch [2] and emitter-coupled logic [3]. Up to 121 chips can be mounted on the 9121 thermal conduction module (TCM); each of the bipolar chips contains 2620 internal

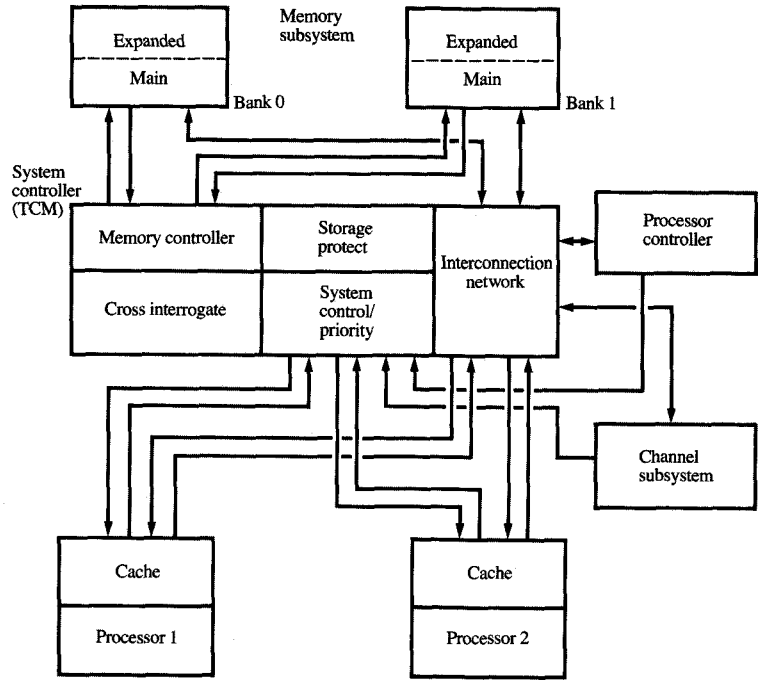

Figure 1

High-level diagram of ES/9000 Type 9121 system controller, showing data paths to and from interconnection network, and primary system control and memory control interfaces.

differential current switch (DCS) cells and 228 signal I/O pins. To permit an air-cooled design, the SC primarily uses ultralow- and low-power DCS circuits. These circuits have a speed-to-power ratio superior to those of previous emitter-coupled logic (ECL) technologies. To further reduce power, the SC has constructed the ESA/390™ storage-protect array [4] with complementary metal oxide semiconductor (CMOS) technology. The extremely low power dissipation and high density of the CMOS array chip [5], designed for the 9121 system, were vital to the SC development. The ES/9000 systems are the first to incorporate CMOS and bipolar technologies in the same TCM.

The section on system controller function reviews the role of the SC in the 9121 system. Next, the single-TCM packaging constraint and its effect on the SC development are discussed. The novel features of the design are described in the section on design enhancements, followed by a review of the 9121 memory subsystem and sections on its design strategies and packaging details.

System controller function

In a multiprocessor system, the SC provides several important functions: access to storage, storage control, storage protection, data consistency, data integrity, and data recovery. These functions are performed by the elements of the SC illustrated in **Figure 1**. The storage access function is handled by the system control and interconnection network. Storage control is the domain of the memory controls, storage protection the domain of the storage-protect element. The primary purpose of the cross-interrogate element is to maintain data consistency. Data integrity and recovery are handled by the interconnection network and memory controller.

- *Storage access*

The system controller executes the channel subsystem and processor controller storage requests, as well as the processor storage requests which cannot be serviced by the processor cache. Management of the storage-requestor interconnection network is handled by the system

control/priority logic, which contains and maintains queues for all requests: main-storage reads and writes and expanded-storage reads and writes. Memory bank conflicts, interconnection resource conflicts, and conflicts occurring during paging operations are detected by the priority logic. (A paging operation involves the transfer of a 4KB page of data between main store and expanded store.) The system controls invoke the storage protection and data consistency functions in parallel with storage read accesses. If the SC determines that the accessed data line is protected, the requestor is notified of the violation and the access is aborted. The data consistency function ensures that the most recent copy of data within the system is returned to the requestor on read accesses.

- *Storage control*

The memory control element of the 9121 SC contains hardware dedicated to the initialization and testing of the memory subsystem [6]. This element also initiates the memory array read and write operations, and sequences the transfer of fetch data from the memory subsystem and the transfer of store data to the memory subsystem. Up to 128 bytes (or one line) of array data can be read or written during each storage access. Eight bytes (or one double word) are transferred per cycle between the SC and memory subsystem. The 9121 memory subsystem, like most memory subsystems, incorporates dynamic random access modules (DRAMs) to achieve high memory density.

- *Storage protection*

In a multi-user environment it is important to protect a user's data from other users. The storage-protect element of the SC maintains a storage-protect key [4] array for this purpose. One key is associated with each 4KB page of main storage. All accesses to main storage are subject to protection, and the SC enforces this safeguard by comparing the requestor's access key with the key stored in its array. In addition, the storage-protect array contains change and reference bits which are set whenever data within a page have been changed or referenced. These bits are examined and cleared by the ES/9000 operating systems and significantly improve system performance by reducing the frequency of page faults [7]. With this referencing information a working set of pages can be developed for each user, and these working sets can be paged into main store before the operating system performs the task switch restarting execution of a user's job.

- *Data consistency*

Multiple copies of data are allowed in the 9121 system as each processor incorporates a high-speed store-in buffer, or cache. The changed line of data residing in the cache is not written back to main storage until another processor or the channel subsystem requires it, or until this line is cast out to make room for the line most recently accessed by the processor. The cross-interrogate element of the SC contains and maintains copy directories of each of the processor's caches. These directories are searched during requests for storage to determine where the latest copy of data resides. Some processor requests for data can thus be serviced via cache-to-cache transfers [8].

- *Data integrity and recovery*

A single-bit error correction, double-bit error detection (SEC/DED) code is used throughout the 9121 memory subsystem. The interconnection logic generates one check byte for each double word of store data prior to transmission to the memory subsystem. The DRAMs of the memory subsystem are organized such that each DRAM contains at most one bit of a code word. In this way, any single DRAM failure results in only single-bit (correctable) errors. In addition, the memory controller executes a complement/recomplement procedure [9] in an attempt to recover data with two or more bits in error.

Single-TCM constraint

The overall system objective of constructing a dyadic (two-processor) machine within a single frame required a one-TCM system controller design. Even with the improved 9121 technology density, no prior-art SC design with expanded storage controls and a fully overlapped memory data transfer capability would have fit within one TCM. Both the chip count and the I/O count of the 9121 TCM would have been significantly exceeded with prior-art implementations. Concessions have been made in the SC design, which is similar in many respects to that of the ES/3090 system controller. Many design trade-offs were proposed and analyzed with respect to their impact on chip count savings, I/O count savings, functional loss, and performance loss. These proposals included

- Elimination of the expanded storage array, its interface, and the expanded storage controller.
- Consolidation of the memory control and system control data flow and error-correction circuitry.
- Replacement of the unidirectional memory data interface with a bidirectional interface.
- Consolidation of the multiple trace arrays.

In the end, all of these items were incorporated into the SC design.

- *Expanded storage*

Elimination of the expanded storage array and interface not only reduced the SC I/O and cell counts, but it also circumvented the costly expanded storage subsystem

development effort. However, the 9121 system could not exclude the pageable storage feature because there are user applications which require it. To achieve the above reductions and to retain the expanded storage function, the system has physically combined main storage and expanded storage into one array. The 9121 system provides flexibility in the assignment of physical storage locations to main or expanded storage. This new feature, which is invoked during system configuration, permits optimal storage allocation for different applications.

The performance impact of combining main and expanded storage was evaluated. The increased utilization of the memory data bus during paging operations does not affect uniprocessor performance because these operations are synchronous; i.e., the processor does not issue other storage requests until the paging operation is complete. The dyadic performance is slightly affected because the other processor may issue storage requests during a paging operation. The method of buffering the data being paged between main and expanded storage was the more pertinent concern. Buffering of data within a processor's cache during paging of data between main and expanded storage would result in substantial performance loss. A dedicated paging buffer design, as found in the ES/3090 expanded storage controller, was rejected because it required an excessive number of additional SC chips. One store-back buffer (in the SC) already existed for each processor; it served to hold data being cast out of a processor's cache until the memory subsystem was available for receiving the data. With minimal additional circuitry this buffer was designed also to hold lines of data being paged between main storage and expanded storage. The performance and circuit count objectives were met at the expense of increased complexity in the controlling of the store-back buffer. Use of the store-back buffer during paging operations is a novel feature of the 9121 system.

Double usage of the store-back buffer requires special control functions. Previously, data held in the store-back buffer could be stored into memory as soon as a data path was established, since the cross-interrogate and storage-protect functions are only required when fetching data. Now, however, the cross-interrogate and storage-protect functions must be invoked before unloading of page data from this buffer. This creates the potential for system deadlocks, and three design changes were made to eliminate this hazard. First, the priority function was modified to accept paging operations only when deadlocks can be avoided. Second, the cross-interrogate function was enhanced to prevent cast-out operations which would overwrite the contents of the store-back buffer while this buffer is being utilized for a paging operation. Third, the system controls were modified to cancel paging operations and reschedule them upon detection of resource conflicts.

- *Consolidation of data flow*

The memory controller and system controller data flows were consolidated to reduce SC chip count. The primary function of the previous memory controller [1] data flow was to provide data read and write patterns for storage subsystem testing, to check the error-correction code word (ECC) on storage reads, and to attempt recovery of multibit data errors via the complement/recomplement procedure. Additionally, the memory controller staged the read and write data. The system controller data flow or interconnection network buffered the store data on cast-out operations (as mentioned previously), generated the ECC check bits prior to storage writes, checked ECC on storage reads, and returned the data to the requestor. Elimination of the redundancies in the memory controller data flow not only reduced chip count but also eliminated many TCM I/Os. Because of the staging of fetched data in both the memory controller and the interconnection network, the processors observed increased request latency in the ES/3090 system. Thus, data fast paths [10] were added between the memory controller data flow and processors to bypass the system controller staging. The elimination of the data fast path I/O was the additional benefit of the consolidated design. **Figure 2** illustrates the new interconnection network (with fast paths eliminated).

Only two data registers of the original memory controller data flow remain in the 9121 design. These registers provide the data patterns for storage subsystem testing and are used in the complement/recomplement procedure. Although they reside in the system controller data flow chips, the memory controller manages the loading and sourcing of these registers. Again, added complexity in controls has made possible a reduction in chip count.

- *Memory data interface*

A bidirectional memory data bus design was selected over a separate unidirectional fetch and store data bus design to conserve SC chips and I/O. The unidirectional design allows maximal overlapping of storage requests at the expense of high I/O count. Performance loss in the bidirectional design was modeled. The degradation in a uniprocessor system was extremely small, and the loss in dyadic performance was minimized by a design which permitted some operation overlap. Simultaneous fetch data and store data transfers are not possible in a bidirectional design; however, the memory controller overlaps array operations and data transfers when busing conflicts can be avoided.

- *Trace arrays*

Trace arrays are arrays which retain the cycle-by-cycle history of control signals within a TCM. It would be extremely difficult to trace hardware design problems

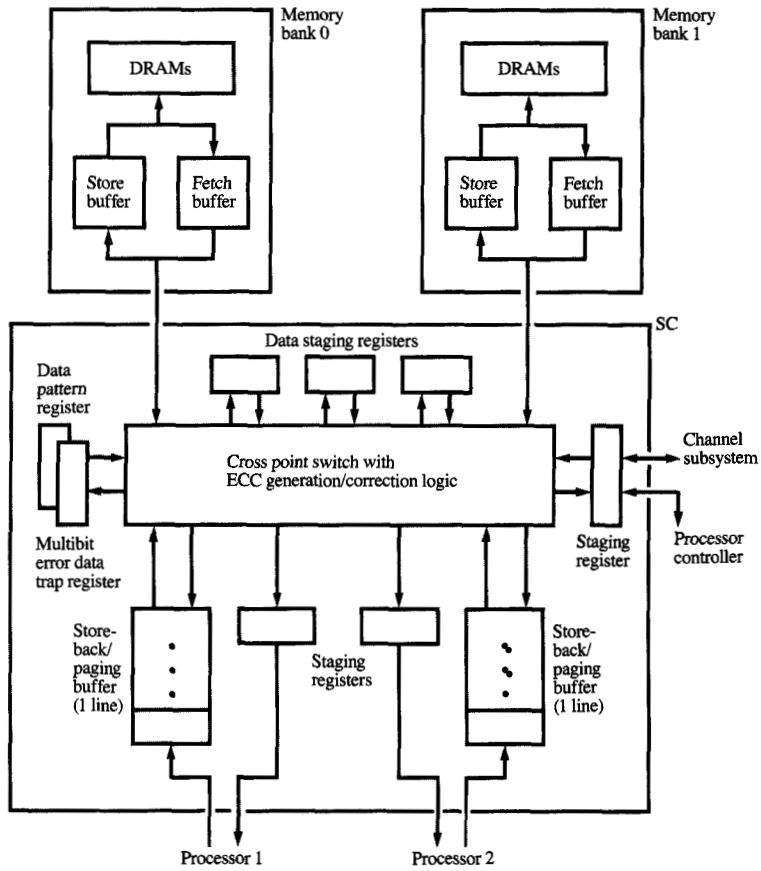

Figure 2

ES/9000 Type 9121 interconnection network and memory data flow.

without such arrays, since internal TCM nets are not easily probed. Generally, trace arrays retain the state of control signals for the prior 32 or 64 machine cycles. The six TCMs of the ES/3090 system controller each contained a trace array; these six arrays were controlled and accessed via four different methods. Because a simple mapping of this function into the new technology would have been inefficient, these arrays were consolidated into a single array with one access method. To further consolidate the trace function, a special reconfigurable array was developed. From prior large-system test experience we know that hardware design problems can be resolved by observing only a subset of the traceable nets. For example, one could dynamically reconfigure the arrays (via the processor–controller interface) to trace the memory sequence controls to assist in the debugging of memory-related problems. Another feature of the reconfigurable arrays is the variable depth, or cycles, of the trace. As smaller subsets of signals are selected for trace, the number of system cycles retained in the trace array increases. The consolidation of the trace array function was the fourth major element which permitted us to meet our packaging objectives.

Design enhancements

Two enhancements to the SC have already been described: the paging controls which utilize the store-back buffer and the reconfigurable trace arrays. Both were motivated by packaging constraints. Here we discuss two additional novel features of the 9121 SC design: the locality-of-reference memory controller and the storage-protect error-correcting functions.

• *Memory controller locality-of-reference feature*
The 9121 memory subsystem utilizes page-mode DRAMs to access a line of data; i.e., each column address accesses a partial line of data. Although this design increases the time required to sequence fetch or store operations (busy time), it significantly improves memory subsystem integration. (The memory design section of this paper elaborates on this point.) No attempt is made to invoke page mode between line accesses, because a large performance penalty is associated with recycling of the row address strobe (RAS) when the subsequent access is to a different row. Novel memory controller circuitry has been designed to exploit the locality of storage references while avoiding the above penalty. Fundamentally, the memory controller and memory subsystem remember the address of the last storage operation. The memory subsystem can anticipate that the next request for memory will access the same DRAM page. On subsequent fetch requests the memory controller compares the current and retained addresses. When they reference the same page, the controller can expedite the DRAM timing sequence and return the data to the requestor with less delay. In some respects this function is similar to invoking the page mode function of DRAMs across memory accesses. However, the off-page performance penalty associated with the recycling of the RAS is eliminated.

• *Storage-protect error correction*
The 9121 storage-protect key array has been implemented with the 10-ns-access 128Kb CMOS array chip designed specifically for the 9121 processor system [5]. The use of this chip has resulted in a significant decrease in the number of array chips; previously, the storage-protect array and control logic occupied an entire TCM [1]. Storage-protect array fault tolerance and improved key error detection were two important 9121 design objectives. Both objectives, which significantly reduce the occurrence of storage key failures, were achieved with the implementation of an error-correction code. **Figure 3** illustrates the storage-protect hardware.

For small data words such as keys, significantly more check bits are required to provide error correction than to provide parity protection. To minimize the number of check bits, and, thus, the quantity of CMOS chips, these bits are generated over a pair of keys. (Error-correction code words spanning more than two keys would not have reduced the CMOS chip count further.) A special error-correcting code with 14 data bits and 6 check bits has been developed for the 9121 system. This code allows correction of all single-bit errors, detection of all double-bit errors, and detection of all errors resulting from the failure of an entire CMOS array chip. In addition, knowledge of the physical failure mechanisms of the CMOS array has been incorporated into the code. Two-bit adjacent errors which may result from a chip quadrant failure are correctable. Just as in the system interconnect logic, the storage-protect function incorporates circuitry to generate ECC check bits prior to storing of key data into the arrays and to check these bits upon fetching of key data. However, the storage-protect control logic first reads a pair of keys before storing into the array because of the two-key ECC design. This design does not significantly affect performance, since key stores occur much less frequently than fetches.

Memory design

• *Memory subsystem function*
A memory subsystem must minimally fetch and store lines of data. Additional requirements have been placed upon the 9121 memory subsystem. The channel subsystem performs byte updates; thus, the memory subsystem must incorporate logic to store partial lines. Because of the 9121 error-correction code structure, the smallest entity which can be read or written into the memory array is a double word. Also, the system must be able to fetch or store from one double word to sixteen double words (one line) of data. The system may begin the store transfer at any double word within the line, or request that the fetch transfer begin at any double word within the line. This latter feature ensures that the processor receives the word required to resume program execution with minimum delay.

Cast-out operations entail simultaneous fetch and store operations and occur with store-in cache designs on cache misses when the least recently used line of data to be displaced has changed. One method to permit concurrent fetch and store operations is to provide separate fetch and store data buses to memory. However, this design was rejected (as discussed earlier) because of I/O restrictions. Bidirectional buses are used in the 9121 system between the memory support logic and SC and between the memory support logic and DRAMs. Full line fetch and store buffers have been implemented in the memory support logic to permit independent operation of the data transfer and array accessing functions.

Because of the high switching speeds of the 9121 system and the physical length of the interface wiring, all SC-to-memory-card and card-to-card nets are point-to-point to guarantee first incident switching and signal integrity. To minimize the memory interface I/O signals, each card in a memory bank receives part of the address or starting double word and repowers it to all the cards in the bank. A reduction in memory card parts is also obtained with this design, because a unique repowering card is not needed.

Reliable detection of memory support failures and identification of the failing card were other important memory subsystem design requirements. To provide

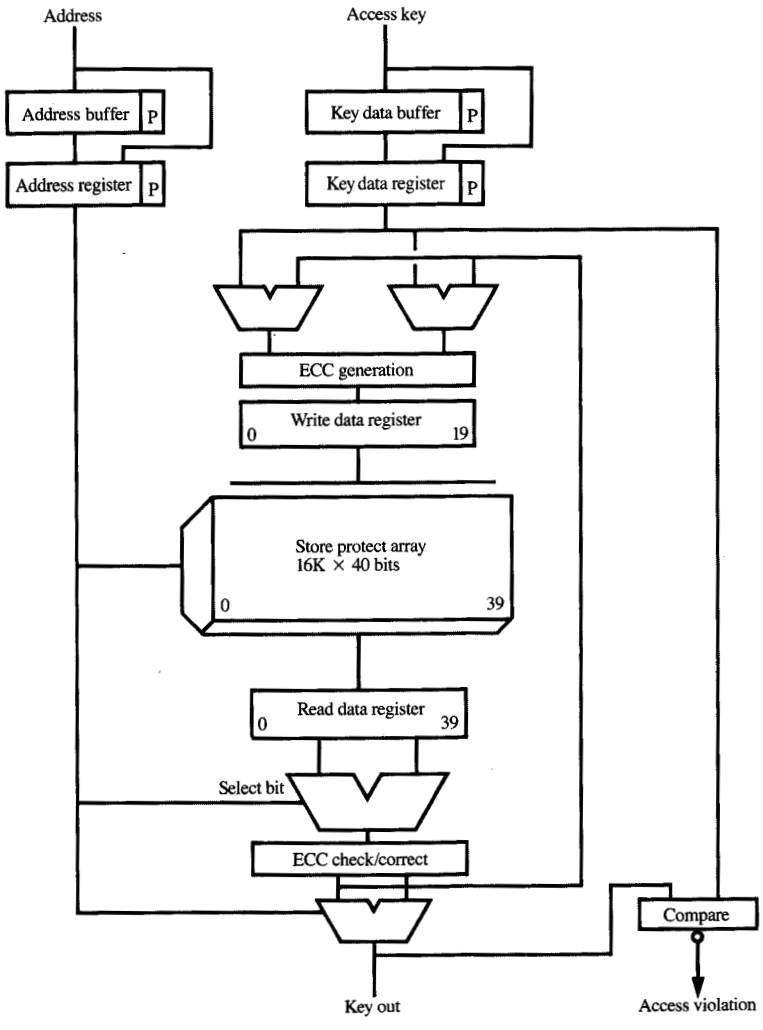

Figure 3

Storage-protect data flow, showing ECC circuitry.

maximum error detection, the memory subsystem utilizes the synchronous operation feature of the memory support modules. All modules within a card are in constant communication with one another. Similarly, the modules centrally located on each card exchange information pertaining to their present operational state. Since all modules within a memory bank should be operating synchronously, any module failure can be detected immediately and the failing component can quickly be isolated.

•*Design alternatives*

There are basically two different approaches to designing a memory subsystem to satisfy these requirements. A minimum-function set card can be developed to provide only the DRAM modules and the address, data, and control repowering logic to drive the high-fan-out nets on the card. The card interface and DRAM interface are equivalent; thus, cards designed with this approach are inexpensive and easy to manufacture and test. The system utilizing such cards must generate all of the critical control

signals required by the DRAMs. This is usually the most cost-effective solution, because the control function is centralized and need not be duplicated on all memory cards. Unfortunately, much skew is introduced in the long signal paths between the system and DRAMs; this skew may translate into increased memory access and array busy times.

Conversely, a memory card could be developed with maximum function. Current VLSI technologies allow integration of all memory support and control functions on a single chip. The major advantages of this approach are the synchronous interface with the system and reduced skew on the critical control signals. The synchronous feature is highly desirable, since it greatly simplifies both the development of a compatible interface and the interface timing analysis. However, the integration of support and controls on the memory card increases the card manufacturing costs and the complexity of the card test.

The 9121 memory subsystem is a compromise between these two alternative designs. The system controller provides the memory cards with all critical control signals, but the card latches the controls before repowering them to the DRAMs. In this way, skew is minimized at the DRAM interface. A small reduction in performance has been conceded with this design, since DRAM timing transitions are restricted to system clock edges. However, the benefits of the centralized timing function outweigh the small sacrifice in performance. Delay lines typically account for a substantial portion of card failures; thus, the elimination of the on-card timing delay lines improves the memory subsystem reliability. Other advantages of this design include the reduction of four (one per card) timing rings into the one centralized DRAM timing element in the SC. Reduction and consolidation of function are sometimes overlooked in large-system designs. The 9121 memory subsystem has been designed with the philosophy that fewer components means fewer failures.

- *Packaging*

The 9121 memory subsystem consists of two sets of four cards which plug into a single storage board. Each set of cards comprises a processor memory array or bank. The two banks are independently controllable by the memory controller. No signal communication is provided between banks; these arrays share only power distribution. The memory support function is implemented on three ECL chips mounted on multilayer ceramic modules with 180 signal I/Os. DRAMs are mounted on single in-line packages (SIPs) to achieve higher card densities (see **Figure 4**). The height of the SIPs forces the cards to occupy only every other slot in the board. Thus, the SIPs provide no volume density advantage over other DRAM packaging techniques such as double-sided-surface-mounted modules. However, the reduction in memory cards is advantageous, because it significantly reduces the memory card-to-card repowering requirements and reduces the number of system controller interface signals. Each card contains 16 or 32 SIPs which are each populated with nine 1Mb or nine 4Mb DRAMs. Memory configurations from 64 megabytes (in one memory bank) to one gigabyte (in two memory banks) are supported with these four card types.

- *Design process*

To improve memory card testability and simplify timing analysis, the memory support logic conforms to level-sensitive scan design (LSSD) [11] rules. An LSSD design permitted the internal support chip path delays to be analyzed with the same set of tools used to time TCM paths. The SC–memory-support and the memory-support–DRAM interfaces were evaluated with another timing tool called ASTAP (Advanced Statistical Analysis Program) [12]. The latter interface delays were used to create the cycle-by-cycle DRAM control timing sequences and the memory controller hardware to generate these sequences. In addition to the timing analysis, signal crosstalk noise, delta-I (or switching) noise, and signal undershoot evaluations were performed on the memory card design. Much analysis was performed to predict and then measure the amount of noise coupled into the power distribution network under worst-case conditions.

Several features of the memory subsystem design permit the memory support function to be implemented on just three chips. The first feature is the cell-efficient embedded array implementation of the line fetch and store buffers. The second is the multiple usage of the data I/O during array accesses, i.e., exploitation of the DRAM page mode feature to access a line of data. Further support chip I/O savings are achieved by wiring multiple DRAM I/O pins into a single net. The reduced number of DRAM data nets also simplified the memory card wire placement.

Conclusions

Denser chip technology and the mixing of different circuit technologies on the same chip and the same TCM (DCS, ECL, and CMOS) have culminated in a single-TCM ESA/390 system controller. Careful selection of the technologies available to implement the controller functions was required. Significant improvements have been made to the design in parallel with the reduction effort. Flexibility in the memory subsystem attachment and a more versatile main storage/expanded storage design are two of the most important improvements. Other 9121 developments include a new memory controller function which exploits locality of storage references, and an innovative error-correction code designed specifically for the 9121 storage-protect array configuration. These two

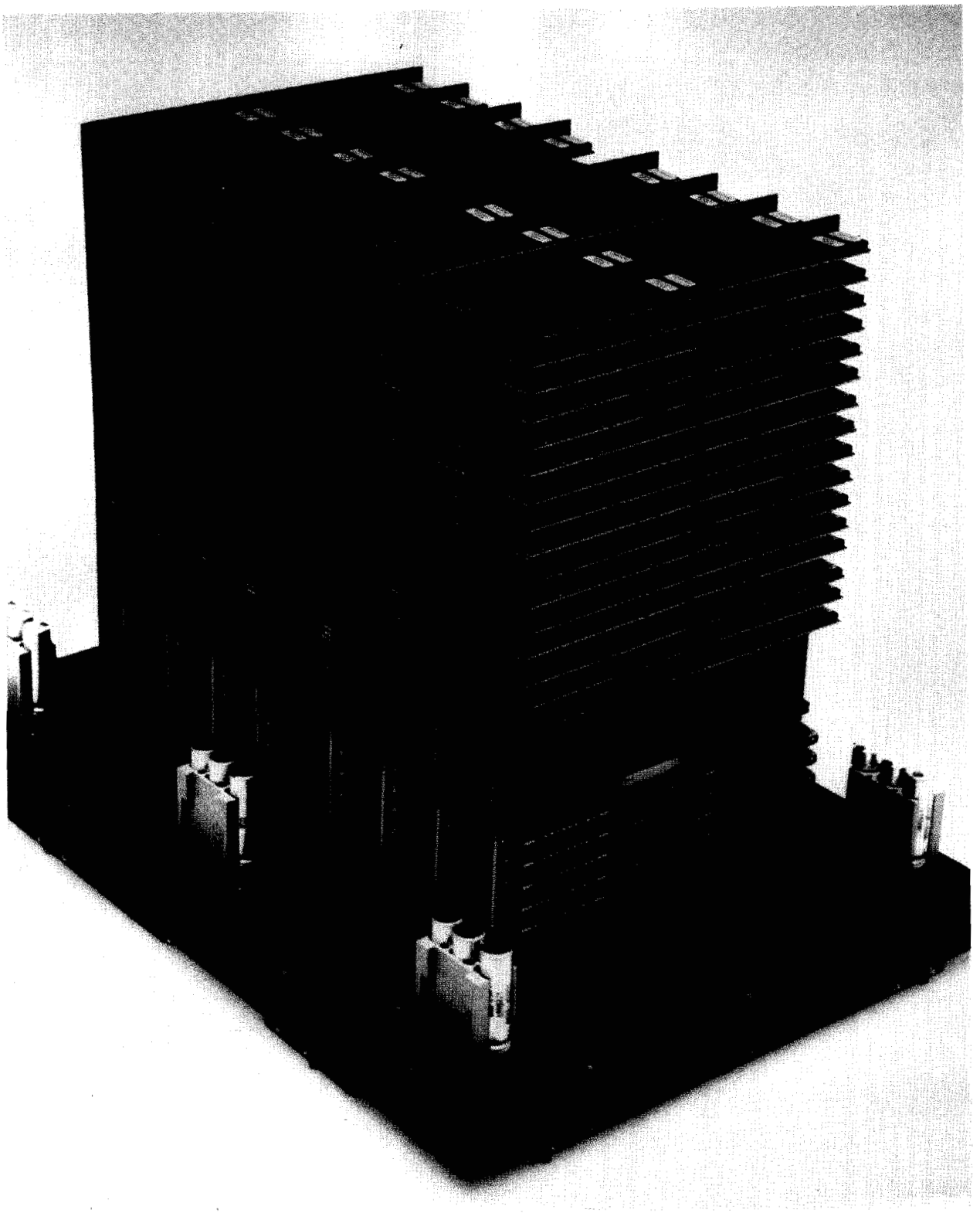

Figure 4

ES/9000 Type 9121 memory subsystem, consisting of one storage board with eight plugged memory cards. Each card accommodates 32 SIP packages; the three support chips can be seen near the base of the card.

features respectively improve system performance and system reliability.

A new memory subsystem incorporating two independent banks on the same board has been developed. This improvement in integration became feasible with the increased density of the support chip technology, the development of new data accessing methods, and the use of single in-line packages.

Acknowledgments

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