IBM System/390 air-cooled alumina thermal conduction module

by J. U. Knickerbocker

G. B. Leung

W. R. Miller

S. P. Young

S. A. Sands

R. F. Indyk

Advances in multilayer ceramic (MLC) processing, the use of thin-film metallurgy wiring, and enhancements in thermal dissipation, all described in this paper, represent significant milestones in the evolution of microelectronic packaging technology. The IBM System/390™ air-cooled alumina thermal conduction module (S/390™ alumina TCM) utilizes a 127.5 × 127.5-mm MLC substrate to interconnect as many as 121 VLSI devices and 144 substrate-mounted decoupling capacitors. The substrate provides an array of 648 pads for solder connections to each device, an array of 16 pads for solder connections to each capacitor, and an array of 2772 pins for interconnection with the next package level, and contains approximately 400 m of wiring. The reduced thermal resistance design permits up to 600 W of air-cooling capacity. This paper describes the S/390 alumina TCM fabrication processes and discusses the advances they represent in processing technology, packaging density, and performance. Comparisons to prior technology are made.

Introduction

In 1980 IBM introduced the thermal conduction module (TCM) used in the 3080 systems [1, 2] and in 1985 the TCM used in the 3090[™] systems. This paper describes the System/390™ air-cooled alumina thermal conduction module (S/390™ alumina TCM) which is used in an intermediate-performance processor in the recently announced IBM Enterprise System/9000™ (ES/9000™) processor family. The S/390 alumina TCM components are shown schematically in Figure 1. Assembled, the module measures 166 mm wide by 146 mm deep by 169 mm high; it contains up to 121 logic and array chips with 144 decoupling capacitors, all mounted using controlled collapse chip connection (C4) technology. The S/390 alumina TCM utilizes a new MLC substrate, top-surface thin-film redistribution wiring, and a new air-cooling technology which allows the package to dissipate 600 W, and uses 2772 pins to connect with the second-level package. In this module CMOS and bipolar chip technologies are packaged together on a single TCM for the first time. The evolution of the TCM in terms of physical and electrical characteristics is shown in Table 1.

In the following sections of this paper, design features and process technology advances are described. The three

[®]Copyright 1991 by International Business Machines Corporation. Copying in printed form for private use is permitted without payment of royalty provided that (1) each reproduction is done without alteration and (2) the *Journal* reference and IBM copyright notice are included on the first page. The title and abstract, but no other portions, of this paper may be copied or distributed royalty free without further permission by computer-based and other information-service systems. Permission to republish any other portion of this paper must be obtained from the Editor.

major S/390 alumina TCM fabrication process sectors are the multilayer ceramic substrate process, the thin-film process, and the module assembly and test process. The process flow for these sectors is outlined in Figure 2. Details of the MLC substrate process steps and module process steps as applied to a TCM have previously been described [1–3]. This paper focuses on the advances made in these processes, as well as the new technologies which are required in the fabrication of S/390 alumina TCMs.

Design features of the System/390 alumina substrate

Sixty-three metallized alumina layers make up the 127.5 × 127.5-mm S/390 alumina MLC substrate. Figure 3 shows the design advantages of the S/390 alumina substrate compared to the 3090 TCM substrate. These advantages are, specifically, an increase of 2.8 times the number of available C4 connections, a 4 times increase in wiring length, and a 1.5 times increase in I/O capability. The thin-film metallurgy applied directly to the surface of the planarized ceramic requires 78 500 vias in the substrate top surface for interconnection among chips, interconnection between chips and I/O pins, and interconnection between chips and pads for the bonding of engineering change wires. A total of 121 sites are available for chip joining. Additionally, 144 sites are provided for the attachment of discrete decoupling capacitors to the substrate top surface. Since the alumina/molybdenum materials set is identical to that used in previous TCMs, the electrical characteristics of the S/390 alumina MLC substrate are similar to those reported previously [1].

The addition of a single-layer thin-film metallurgy pattern provides the interconnection density required for the ES/9000 application. Detail of the thin-film pattern is shown in **Figure 4**. The pertinent thin-film design features include copper conductors as narrow as 12 μ m, as defined by the lift-off process in the chip interconnection (C4) areas, and as wide as 58 μ m, as defined by a wet-etch process in the repair and engineering change (EC) areas. MLC vias are capped with pads nominally 180 μ m in

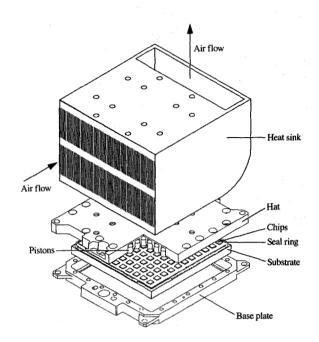


Figure 1
Assembly/cutaway view of the S/390 alumina TCM.

diameter. Additional C4 pads, which are connected to thin-film lines, are deposited on blank ceramic areas rather than directly on top of an MLC via. These pads are nominally 150 μ m in diameter. Openings to all of the C4 pads through a polyimide overcoat layer are defined by a laser ablation process [4] and are nominally 100 μ m in diameter. Through this array of 648 openings on 225- μ m centers, the VLSI devices are joined to the MLC substrate. Also ablated simultaneously with the C4 openings are 258 openings to allow the bonding of EC wires to appropriate pads. Nominal EC pad dimensions are 230 \times 258 μ m, with nominal openings in the overcoat of 250 \times 491 μ m.

Table 1 Evolution of TCM design features.

	3080 TCM	3090 TCM	System/390 air-cooled TCM
Size (mm)	90 × 90	110.5 × 117.5	127.5 × 127.5
Layers	33	36-45	63
Via count	350K	470K	2000K
Wiring (m)	130	180	400
Available C4 connections	16K	24K	80.7K
Chip sites	100-133	132	121
I/O pin connections	1800	1800	2772
Terminal metallurgy	Plating	Plating	Plating/thin film
Cooling capacity (W)	300 (water)	520 (water)	600 (air)

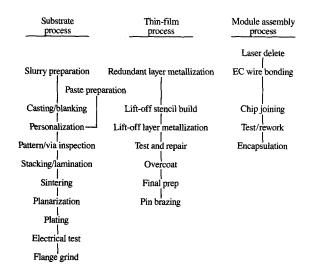


Figure 2

S/390 alumina TCM process flow.

Multilayer ceramic substrate process

• Materials processing

The S/390 alumina MLC substrate process begins with the preparation of a ceramic slurry and thick-film metal paste. The ceramic slurry, comprising alumina powder, glass

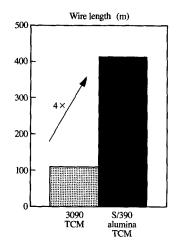
powder, organic binder, plasticizer, and solvents, is cast into 0.20- and 0.28-mm-thick greensheets. The dimensional stability of the greensheet and the absence of impurities in it are critical in the fabrication of S/390 alumina MLC substrates. Stability is critical because of the increased number of punched vias and increased metallized area which must remain stable for layer-to-layer alignment during layer stacking. Impurities must be minimized to prevent subsequent voids and other surface defects which adversely affect plating and thin-film features. Enhanced greensheet inspection ensures that the 185-mm-square sheets are free of pinholes and contamination defects.

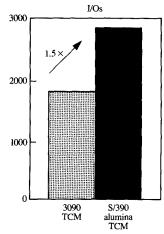
The thick-film paste used to form the three-dimensional conductive circuits in the substrate is fabricated from molybdenum powder, glass powders, organic resins, and solvents. These pastes are individually formulated for the various substrate layers and are homogenized and milled to produce the metallized paste used in the screening process. The choice of paste solvents and organics is critical in minimizing their interaction with greensheet materials and subsequent greensheet movement, especially on layers where significant screened metallization is required.

Personalization process

Personalization is the process whereby each of the 63 greensheet layers used in the substrate receives its unique circuit pattern and through-sheet via patterns. This is achieved through punching, screening, and inspection operations.

The via holes in each greensheet are mechanically punched by computer-controlled step-and-repeat





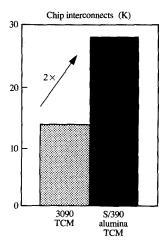


Figure 3

S/390 alumina MLC substrate design improvements

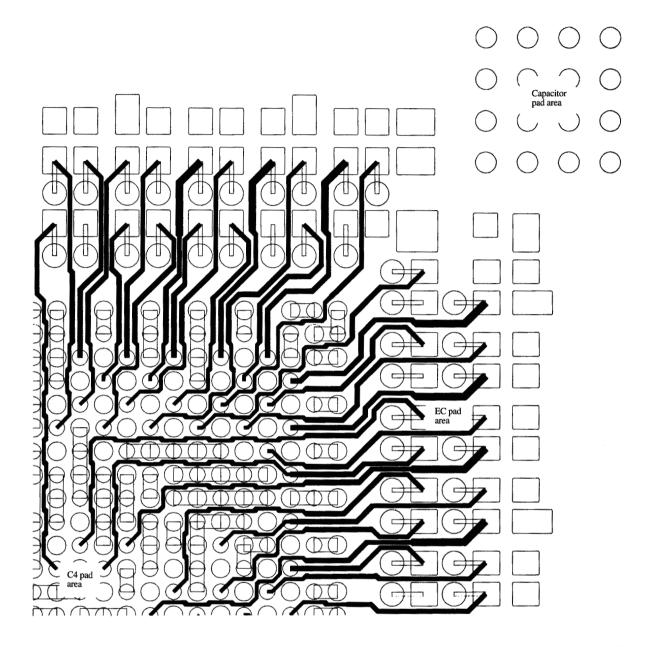


Figure 4

Thin-film pattern on typical chip site quadrant.

equipment capable of punching up to 121 holes simultaneously per stepping cycle as the greensheet is moved on a precision X-Y table. Figure 5 shows a portion of a S/390 alumina MLC substrate top-surface-layer greensheet which contains 78 500 via holes, each with a nominal diameter of 100 μ m. In comparison, a 3090 TCM MLC substrate top-surface-layer greensheet has 36 000 vias, each with a nominal diameter of 125 μ m. The four corner location holes, which are used to register and to

align each of the sheets precisely in subsequent process steps through lamination, are also shown.

In screening, the thick-film molybdenum metal paste is extruded through layer-unique metal masks to form continuous metal wiring patterns and to fill interlayer via holes. Nominal screened via diameters are 100 and 140 μ m, and nominal screened line widths are 100 μ m. After screening, the metallized greensheets are dried in forced-air-circulation ovens utilizing a time-temperature drying

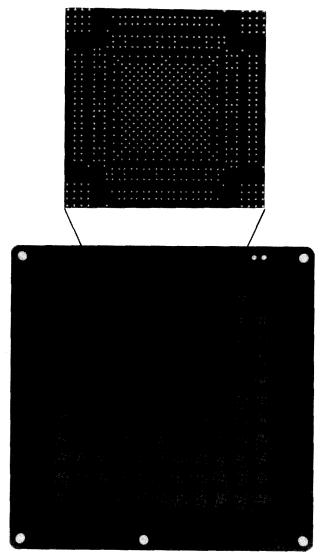


Figure 5

Detail of S/390 alumina punched top layer.

cycle designed to minimize greensheet movement. The punching, screening, and drying operations are tailored such that existing TCM MLC substrate specifications for greensheet movement are met despite the increased demands imposed by the larger number of through vias and the larger greensheet metallized area on the S/390 alumina TCM MLC substrate layers.

The automated inspection of each greensheet for pattern and via integrity is critical to the successful construction of MLC substrates. This process ensures that each layer passes the appropriate specifications and prevents the assembly of defective layers into a laminate.

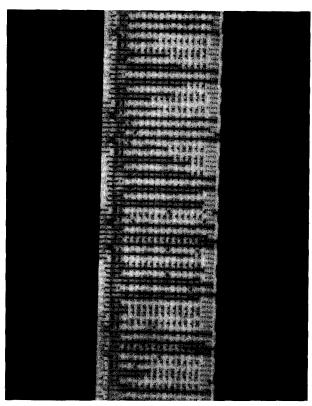


Figure 6
Cross section of S/390 alumina MLC substrates.

• Stacking, lamination, and sintering
Each of the 63 inspected personalized greensheets is
cleaned to remove foreign particulates, stacked, cut to the
lamination die cavity size, and laminated at a
predetermined temperature and pressure. The lamination
parameters are determined both by the raw-material
characteristics and by the substrate dimensions, and are
chosen to ensure the dimensional and mechanical integrity
of the substrate during the sintering process. Up to 2.0
million vias must be aligned within the substrate during
this process to ensure its electrical integrity. Figure 6
shows a cross section of a S/390 alumina TCM MLC chip
site, demonstrating the resultant alignment.

In sintering, the polymeric constituents present in the greensheets are removed, and the laminate is densified in a high-temperature furnace to form an MLC substrate. Polymer removal is accomplished through pyrolysis (decomposition) during heating to 600°C. Any residual carbon is removed by the use of wet hydrogen between 950 and 1150°C. The polymer removal process step is especially critical in the S/390 alumina MLC substrate because it contains three to five times more polymer than previous TCM substrates as a result of its increased size.

The polymer removal process is made more difficult because the diffusion resistance for the removal of the gaseous products of the pyrolysis process is more than three times greater in the S/390 alumina TCM substrate than in previous TCM substrates, again because of increased size. Adjustments to the sintering time-temperature profile, adjustments to the ambient atmosphere, and increased furnace gas exchanges are necessary to successfully decompose and remove all organic material in the S/390 alumina MLC substrate without causing layer delaminations or substrate cracks. As with other TCM substrates, final densification takes place in the range of 1250 to 1560°C under wet hydrogen. During this portion of the sintering cycle, the substrate experiences approximately 17.2% linear shrinkage.

• Precision sizing and planarization

To ensure the accurate placement of the thin-film patterns, substrates are cut after sintering to tight tolerances in the X and Y dimensions by referencing to alignment fiducials sintered into the substrate surface. Lapping and polishing techniques are used on the top surface to render the substrate flat and smooth for thin-film application and to prevent the formation of surface defects which would perturb the overlying thin-film metal features. After planarization the substrate top surface has a nominal flatness of 5 μ m and a surface finish of 300 Å average roughness (R_a).

• Finishing

All substrate metallized features are plated with nickel and gold. Electrical test is utilized to identify opens and shorts. Some substrate defects are repairable by use of discrete wiring adds for opens and line deletions for some short circuits. Prior to thin-film deposition, each substrate is ground to provide a seat for its encapsulation required later in the module assembly operation. Figure 7 shows a S/390 alumina MLC substrate ready for thin films. Finally, after thin-film processing, I/O pins are attached to the bottom surface of the substrate using the standard TCM pin attached to the substrate surface with a eutectic gold—tin braze. After the thin-film and braze processes, the finished S/390 alumina MLC substrate is ready for the module assembly processes.

Thin-film processes

A significant enhancement to the alumina TCM technology is the utilization of a thin-film metal structure on the top surface of the S/390 alumina substrate. The use of thin films in the substrate design affords simplification of the ceramic structure in that fewer ceramic layers are needed to achieve the same substrate functionality. Successful stress testing (thermal, electrical, and mechanical) has demonstrated the reliability of both the thin-film

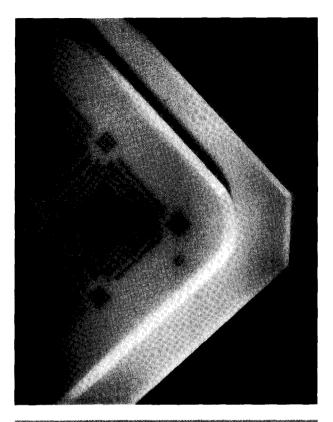


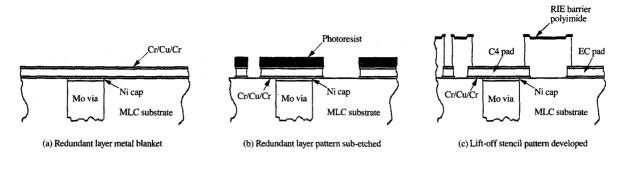
Figure 7
S/390 alumina MLC substrate ready for thin-film processing showing detail of the ground encapsulation flange.

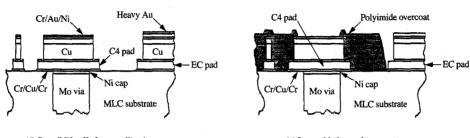
metallization and the thin-film-S/390 alumina substrate composite structure.

The major steps in the fabrication of the thin films on the substrate are shown in Figure 2. The redundant layer is defined on the alumina substrate surface by sub-etching and serves to enhance the electrical test yield for opens. The lift-off layer is placed on top of the redundant layer and serves as the major conductor pattern. It also provides device and wire connection metallurgy. Cross-sectional views at various steps in the process are shown in Figure 8 and are described more fully in the following sections of this paper. The alumina MLC substrate provides a stable base upon which thin films can be fabricated; therefore, thin-film materials and processes may be optimized without substrate limitations.

• Redundant layer metallization

The redundant metal layer is formed by a blanket metallization followed by photo expose and develop and sub-etch processes. After an initial cleaning and bake, the planarized alumina MLC substrate is mapped for feature





(d) Stencil lift-off after metallization

(e) Laser ablation and overcoat

Figure 8

Major thin-film processing steps showing the construction of the thin-film metallurgy features.

locations to provide data for subsequent thin-film feature definition. A blanket metal layer of chrome/copper/chrome is then evaporated or sputtered directly onto the MLC surface. Photoresist is spun onto this blanket metallurgy, exposed using the substrate mapping data, and then baked and reversed to give a negative-develop pattern definition process. The lines and pads required for the redundant layer are left covered by photoresist after development. A sequential chrome/copper/chrome etch is then used to produce the redundant layer pattern. After inspection and measurement of the metal pattern, the part is ready for fabrication of the lift-off layer.

◆ Lift-off stencil fabrication

The first step in the lift-off stencil fabrication involves the application of an adhesion promoter to the redundant layer followed by the application of polyimide which forms the stencil after photographic development and reactive ion etch (RIE). A RIE barrier film is plasma-deposited on top of the polyimide to protect it during RIE of the photographically developed pattern. The pattern is formed with a photoresist spin applied on top of the RIE barrier film and subsequent exposure and development of the photoresist.

• Lift-off layer metallization

Metallization of the lift-off layer is accomplished through the evaporation of a chrome/copper/nickel/gold blanket and the sequential personalization of EC pads with further gold evaporation. EC pad features require extra gold to ensure wire-bonding integrity, whereas the C4 pads require less gold to promote good solder wettability during chip joining. At the conclusion of the evaporation process, the stencil is removed in a hot, agitated solvent, leaving behind the final metal structure on the substrate. With all of the metal features defined in their final form, they are measured for dimensional requirements and sent to test for electrical assessment.

• Electrical test

The test measures opens and shorts in the alumina substrate and the thin-film structure, and determines whether the defects involve the substrate or the thin film. If the defects are thin-film related, the part is cycled through a shorts repair or an opens repair process as required, followed by retest to ensure that the desired repairs have taken place. Both repair processes are laser based. Shorts repair involves the ablation of the extraneous metal causing the short, while opens repair

336

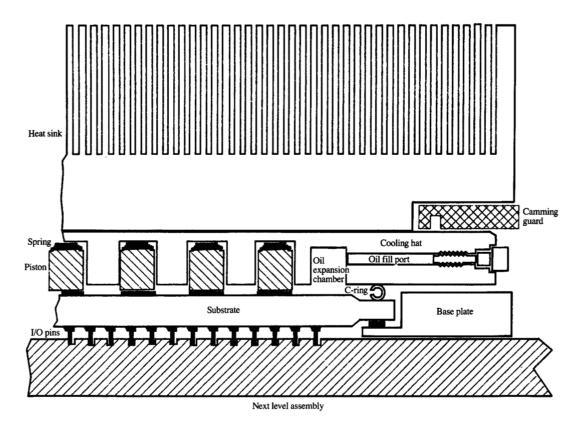


Figure 9

Cross section of the S/390 alumina TCM assembly.

deposits a metal bridge over the discontinuous feature causing the open.

• Overcoat and final preparation

The entire thin-film structure and alumina substrate top surface are now covered with a partially cured polyimide film to provide mechanical protection. Access to the C4 and EC pads is provided by laser-ablated openings in this polyimide overcoat. Ashing and etching of the ablated areas ensures the integrity of these features for the chipjoining and EC-wiring processes during module assembly. Following complete curing of the polyimide coating, an inspection ensures compliance with all final product requirements. The substrate is then shipped to the previously described I/O pin brazing process, which is the last step prior to module assembly.

Module assembly processes

After the substrate is completely metallized and the I/O pins are joined to the bottom surface, the substrate is

tested and is sent to the module assembly operations. At this stage of the assembly process, the VLSI devices and engineering change (EC) wires are joined to the substrate, and all associated module encapsulation and cooling hardware secured. The substrate is now a functional module, ready for final electrical test and subsequent joining to the board assembly. The key sectors in the module assembly area are wire bond, chip join, electrical test, and encapsulation.

The module assembly operations for the S/390 alumina TCM are similar to those used for previous TCMs; however, modifications to both fixtures and process parameters are made as required to accommodate the larger size and mass of the S/390 alumina TCM substrate.

Figure 9 shows a cross section of a fully encapsulated S/390 alumina TCM.

• Wire bond

If a wiring change is required in the module, either because of electrical design changes or because of wiring

337

Table 2 System/390 Alumina TCM thermal dissipation factors.

Maximum chip power (W)	10	
Maximum module power (W)	600	
Internal resistance (°C/W)	1.7	
External resistance (°C/W)	0.05	
Chip size (mm)	6.5×6.5	
Chip pitch (mm)	9.9	
Module size (mm)	127×127	
Heat-sink dimensions (mm)	$140.0 \times 171.3 \times 143.8$	

defects, EC pads are provided to allow surface wires to be routed from one chip site to another. A line deletion is performed by laser ablation of the appropriate thin-film wiring line, and is followed by the ultrasonic bonding of a gold-plated cadmium-copper alloy wire between the appropriate EC pads which completes the wiring change.

Chip/capacitor join

The S/390 alumina TCM is the first TCM that contains both bipolar and CMOS devices. In addition, the module contains decoupling capacitors to provide improved electrical performance. The three components use standard controlled collapse chip connection (C4) technology [5, 6] incorporating 97Pb/3Sn solder to provide the interconnection to the substrate. The use of a common solder allows for joining of all the components in a single temperature cycle.

The change in the substrate terminal metals from a Ni-Au-plated structure to the thin-film structure described previously requires a reducing gas atmosphere in the chip-joining furnace to prevent degradation of the thin-film structure and to ensure good C4 wettability and wire bondability.

The large mass of the S/390 alumina substrate stretches the capability of existing chip-joining furnaces to keep the time-temperature profile uniformly within specifications across the entire substrate. These specifications ensure the reliability of the C4 joints. Modifications to existing furnaces and fixtures manage the heat flux into and out of all sections of the substrate during the chip-join process, allowing all C4 reliability objectives to be met. The module is then electrically tested to verify the functionality of all joined devices.

If after electrical test a device requires replacement, a focused infrared process can remove an individual defective device from the substrate and remove the residual solder from the now-vacant chip site [7]. The device can subsequently be replaced with another by the standard chip-join process. Removal process parameters are tailored individually for each of the devices used in the S/390 alumina TCM because they each have very different

internal structures, physical sizes, and C4 counts, all of which affect the infrared absorptivity and heat dissipation during the removal process.

Encapsulation

After all components have been joined and EC wiring has been completed, the module is encapsulated within an aluminum enclosure, or hat. The hat provides three key functions: a thermal path from the device to the system cooling, mechanical support to the next level assembly, and a controlled environment for the substrate top surface and devices.

The hat is attached to the module by bolting it to a base plate with the seal area of the substrate contained between the base plate and the hat. A lead-coated Inconel C-ring provides a compliant, sealing interface between the substrate and the hat and maintains the hermeticity of the assembly. The dimensions of the seal area, the seal ring, and the encapsulation hardware are engineered to prevent the ring from slipping during thermal expansion or module connector actuation, which can exert forces as high as 700 pounds. Hermeticity must be preserved throughout all module assembly process steps and field thermal cycling conditions to prevent corrosion and electrical breakdown of the module.

After assembly of the hat to the substrate, the sealed S/390 alumina TCM module is backfilled with a poly-alpha olefin oil to reduce internal thermal resistance. The oil replaces the helium gas which is used in other TCM modules. The thermal benefits of this oil and the changes in the encapsulation hardware are described in the next section of the paper.

Assembly of the aluminum heat sink to the hat completes the module assembly process. The heat sink is uniformly bolted to the hat with equal force at 12 appropriately spaced locations. The completed S/390 alumina TCM is now delivered to the system assembly process sectors.

Thermal design

With the increase in circuit density on the VLSI devices, the power requirements of the S/390 alumina TCM exceed those of any previous air-cooled TCM to date by more than 100%. Increases in the chip size and chip pitch are factors in the cooling, but the improvements in materials and dimensions are the major contributors to the improvement in thermal performance (Table 2). The cooling demands are satisfied by the optimization of the existing piston technology, requiring the least change in the normal manufacturing process. The improvements in technology provide the system user with the installation flexibility and cost advantages afforded by air cooling, along with the computing capability previously available only in a water-cooled system.

The objective in designing the module thermal system is to keep the chip junction temperature T_j below a predefined temperature limit based on the device electrical performance and reliability. A simple equation to determine the junction temperature of an individual chip for a given chip power and module power is as follows:

$$T_{\rm j} = T_{\rm amb} + (P_{\rm chip}R_{\rm int}) + (P_{\rm mod}R_{\rm ext}) + T_{\rm air} + T_{\rm c-j} ,$$

where $T_{\rm amb}$ is the local air temperature, $P_{\rm chip}$ is the power of the chip, $R_{\rm int}$ is the internal thermal resistance of the module, $P_{\rm mod}$ is the total module power, $R_{\rm ext}$ is the external thermal resistance, $T_{\rm air}$ is the rise in temperature through the heat sink, and $T_{\rm c-j}$ is the difference in temperature from the front to the back of the device.

The internal thermal resistance is the sum of the individual thermal resistances from the back of the chip to the top of the hat, as shown in **Table 3**. To cool the S/390 alumina TCM, major improvements are required in each of the internal thermal resistances as well as in the external resistance.

The dimensions of the piston were changed to minimize the thermal path from the chip to the top of the hat. The tolerances between the piston and the piston wall are minimized to reduce the interface thermal resistance. Because the gaps are designed such that the motion of the piston in the hole is not impeded, contact between the piston and chip is always maintained. Piston pressure is applied to the chip via a spring behind the piston. The effect of the spring force must be considered, because there are chips with different C4 counts on the same module. The spring design chosen does not induce deformation damage to the C4s on either of the chip types, and at the same time provides sufficient contact between the piston and the chip to minimize thermal resistance.

Changing the piston material from aluminum to copper takes advantage of the excellent thermal conductivity of copper, thus reducing the overall internal thermal resistance. The material change forces a change in the way in which the chips are electrically isolated. Since there is a continuous metal contact among the chips through the hat, there is a requirement to prevent electrical contact among devices of dissimilar silicon substrate potential. On previous TCM technologies, this was prevented by electrically isolating the device through anodization of the aluminum piston. As a consequence of changing the piston material to copper, the aluminum hat must now be anodized. Piston holes are not easily anodized because of the difficulty of replenishing the anodization solution during processing; however, a new process is used which maintains anodization thicknesses to within a few μm in the holes and across the surface of the hat. The anodization requires that the surface finish of the hat be controlled tightly so that there are no burrs or scratches which would adversely affect the anodization layer. The

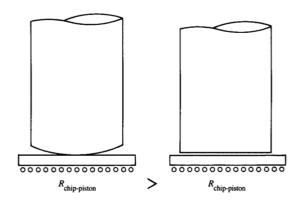


Figure 10

Effect of increasing the piston crown radius.

Table 3 System/390 Alumina TCM internal thermal resistance.

0.1
0.17
0.4
0.63
0.4
0.003

hard, tightly adherent aluminum oxide layer that is formed at the surface of the hat is an excellent electrical isolator.

The piston crown radius is increased from 200 mm to 1000 mm to provide more surface contact with the chip and thereby decrease the chip-to-piston interface resistance (Figure 10). Increasing the crown radius also raises the concern of sensitivity to contamination. Particles greater than a few microns in size could act as spacers and prevent the piston from making good contact with the chip. To eliminate this concern, the back surface of the device is cleaned of contamination before the assembly process, which is performed in a class 100 environment. All surfaces of the piston must be kept free of burrs and defects. The substrate surface planarization operation provides a flat surface to join the chip, keeping the amount of chip tilt after joining well within the limits required for good thermal contact between the chip and the piston.

The replacement of the helium atmosphere inside the hat with synthetic oil provides a 20% improvement in thermal conductivity. A poly-alpha olefin oil is used as the cooling oil because of its thermal conductivity and chemical stability. A slot is machined in the side of the piston to

relieve pressure as the piston moves in the hole during normal machine cycling. The amount of oil added to the hat is controlled, to allow for thermal expansion during temperature cycling.

Another area where the two chip technologies, bipolar and CMOS, are considered is the temperature requirements of each device. Since CMOS technology devices are most efficient at temperatures lower than those typically experienced in TCM modules, these devices are placed on the leading edge of the substrate where the air temperature through the heat sink would be the lowest. The highest-power bipolar devices are spread out over the module to take advantage of the maximum spreading of heat and the most efficient use of the cooling technology.

With the optimized piston design, chip temperatures for a given chip power layout can be estimated by an ASTAP finite-difference model with considerable accuracy [8]. The model is verified by running a module at various power levels and measuring the chip temperatures. Close agreement of the actual data with the model prediction confirms the validity of the model. The module designer can then use the model to confirm that chip temperatures are still within acceptable limits without having to power up a module and generate chip temperature maps for each different design.

Of equal importance to the hat in cooling the S/390 alumina TCM is the air-cooled heat sink. In calculations of the module thermal performance, the heat-sink resistance and the resistance at the hat/heat-sink interface constitute the external thermal resistance. Three important factors are considered in the heat-sink design: thermal performance, cost, and acoustics. The design for the S/390 alumina TCM heat sink is a high-density straight-fin design with air flowing in the transverse direction. The fin density and gap spacing are selected to provide a small pressure drop across the heat sink. The small drop in pressure permits the use of lower blower speeds, allowing low system noise levels. The thermal resistance between the hat and the heat sink is dependent on the amount of contact between the two mating surfaces. The contact area is maximized by finishing these surfaces extremely flat and fine, typically 0.013 mm and N/5, respectively.

Conclusion

The IBM System/390 alumina thermal conduction module is the result of extending existing alumina substrate manufacturing processes and combining them with the use of thin-film metal wiring and the greatly improved thermal dissipation capacity of the air-cooled TCM hardware.

The more significant elements of the module fabrication discussed in this paper include the following:

• Larger mass and metallized area on the substrate drive improvements in the punching, screening, lamination,

- and sintering processes to maintain the dimensional and electrical integrity of the substrate.
- The use of thin-film metallurgy on the top surface provides the interconnection density required for the System/390 application and simplifies the underlying substrate structure. Integral to the use of thin-film wiring is the lapping and polishing of the substrate to provide a flat, smooth surface for thin-film processing.
- Encapsulation hardware improvements, an oil cooling medium, and chip layout design significantly improve the thermal dissipation capability of this air-cooled TCM.

Acknowledgment

The authors wish to express their appreciation to all those individuals in the East Fishkill Packaging Laboratory and in the East Fishkill, Sindelfingen, Poughkeepsie, and Montpellier manufacturing lines whose work contributed to the development and manufacture of the air-cooled alumina TCM utilized in the IBM System/390 processor.

System/390, S/390, 3090, Enterprise System/9000, and ES/9000 are trademarks of International Business Machines Corporation.

References

- 1. A. J. Blodgett and D. R. Barbour, "Thermal Conduction Module: A High-Performance Ceramic Package," IBM J. Res. Develop. 26, 30-36 (1982).
- 2. A. J. Blodgett, "Microelectronic Packaging," Sci. Amer. 249, 86-96 (1983)
- 3. W. G. Burger and C. W. Weigel, "Multi-Layer Ceramics Manufacturing," IBM J. Res. Develop. 27, 11-19 (1983).
- 4. J. H. Brannon, J. R. Lankard, A. I. Baise, F. Burns, and J. Kaufman, "Excimer Laser Etching of Polyimide," J. Appl. Phys. 58, 2036-2043 (1985).
- 5. L. F. Miller, "Controlled Collapse Reflow Chip Joining,"
- IBM J. Res. Develop. 13, 239-250 (1969).
 6. P. A. Totta and R. P. Sopher, "SLT Device Metallurgy and Its Monolithic Extension," IBM J. Res. Develop. 13, 226-238 (1969)
- 7. K. Puttlitz, K. Schink, H. Wenskus, and R. Meyen, "Individual Chip Joining Machine," U.S. Patent No. 4,160,893, July 10, 1979.
- 8. S. Oktay and H. C. Kammerer, "A Conduction-Cooled Module for High-Performance LSI Devices," IBM J. Res. Develop. 26, 55-66 (1982).

Received October 17, 1990

John U. Knickerbocker IBM General Technology Division, East Fishkill facility, Hopewell Junction, New York 12533. Dr. Knickerbocker is a Senior Engineering Manager responsible for Advanced Substrate Development in the Packaging Development Laboratory at the IBM East Fishkill facility. He received his B.S. and M.S. degrees in ceramic engineering from Alfred University and his Ph.D. in ceramic engineering from the University of Illinois in 1983. Upon joining IBM in 1983, Dr. Knickerbocker worked in the Advanced Packaging Technology group in the area of substrate sintering development. He is a member of the American Ceramic Society.

George B. Leung IBM General Technology Division, East Fishkill facility, Hopewell Junction, New York 12533. Mr. Leung is a Senior Engineering Manager in Advanced Process Technology, a thin-film packaging group at the IBM East Fishkill facility. Mr. Leung holds a B.S. in mechanical engineering and an M.S. in industrial administration. His previous work includes the development of multilayer ceramic packaging, multilevel thin-film packaging, thermal electron-beam personalization, gas panel displays, and vacuum process and equipment.

William R. Miller IBM General Technology Division, East Fishkill facility, Hopewell Junction, New York 12533. Mr. Miller is a Development Engineer in the Packaging Laboratory at the IBM East Fishkill facility. He received his B.S. (1979) and M.S. (1984) in materials science from Stevens Institute of Technology. Since joining IBM in 1979, Mr. Miller has worked in the packaging interconnections development area and has managed the Thermal Design and Analysis and the Interconnection Development departments. He is currently manager of the Packaging Product Development Department.

Steven P. Young IBM General Technology Division, East Fishkill facility, Hopewell Junction, New York 12533. Mr. Young is a Senior Engineering Manager in the Advanced Module Development and Technology group at the IBM East Fishkill facility. He received his B.S. (1974) and M.S. (1976) from Lehigh University. After joining IBM in 1976, he was involved with various MLC substrate technologies in both engineering and managerial capacities. Since 1986, Mr. Young has managed various MLC module technologies including module cooling and encapsulation and device interconnection. He is a member of the American Society for Metals International and the International Society for Hybrid Microelectronics.

Scott A. Sands IBM General Technology Division, East Fishkill facility, Hopewell Junction, New York 12533. Mr. Sands is a Senior Engineer in the Thin Film Metallization group at the IBM East Fishkill facility. He holds a B.A. (1962) in physics from the University of Minnesota and an M.S. (1981) in industrial administration from Union College. Mr. Sands joined IBM in 1967 and has engineering and management experience in both the packaging and semiconductor organizations at East Fishkill.

Richard F. Indyk IBM General Technology Division, East Fishkill facility, Hopewell Junction, New York 12533. Mr. Indyk is a Staff Engineer in the Packaging Laboratory at the East Fishkill facility. He received his B.S. (1979) and M.S. (1981) degrees in ceramic engineering from Rutgers University. Mr. Indyk has held various engineering positions in both substrate and module process development since joining IBM in 1981. Specific areas of process involvement include substrate raw materials, chip joining and chip rework, and, currently, substrate planarization.