Preface

IBM recently announced the IBM System/390™ processors known as the Enterprise System/9000™ (ES/9000™)—a single family of air- and water-cooled processors. ES/9000 is upward compatible with System/370™ systems, and offers additional function and new architecture support through the Enterprise Systems Architecture/390.™

This issue of the *IBM Journal of Research and Development* describes many of the technical innovations embodied in the four uniprocessor models (190, 210, 260, and 320) and two dyadic models (440 and 480) comprising the ES/9000 Type 9121 family of single-frame, air-cooled processors. Written by system designers and technologists, these papers detail significant advances made in system architecture, circuit and device technology, machine organization, hardware design, storage subsystem, and self-test methods.

The goal in the design of the Type 9121 processors was to provide the functional performance of a multiframe, water-cooled mainframe computer at the cost of a single-frame, air-cooled mainframe. This challenge was met by development teams from IBM Kingston, East Fishkill, Burlington, Endicott, Poughkeepsie, and Boeblingen. The result, as described in the overview paper by Hajek, was a 15-ns-cycle-time, air-cooled processor which advanced the state of the art in several areas:

- CMOS technology and a newly developed low-power bipolar differential current switch (DCS) circuit family were used to meet power and performance (15-ns cycle time) requirements. Increased circuit density reduced the number of thermal conduction modules (TCMs) from 21 to four (a sevenfold reduction of logic hardware) for the uniprocessors, and to six for the dyadic processors. Decreased power dissipation permitted the TCMs to be cooled by air.
- Central and expanded storage were combined into a single physical storage to conserve circuits and physical volume within the frame. Innovative machine design compensated for the performance loss associated with combined storage.
- Self-test technology was implemented to meet manufacturing test requirements due to increased circuit densities within a TCM.
- A compatible vector function was designed and implemented for the first time within an air-cooled intermediate mainframe processor.
- Advanced fault-tolerant designs were incorporated for all arrays within the machine design.

Two groups of papers are presented, addressing technology issues and design challenges. Technology innovations are described in the first four papers, as follows.

Eichelberger and Bello describe the DCS circuit family, which provides enhanced logic function and improved speed–power capability. Chu et al. discuss the design of a 128Kb CMOS static RAM that provides seven different system applications with an eightfold improvement in packaging density. An innovative multilayer ceramic package with thin-film wiring is presented by Knickerbocker et al., and Gani et al. describe the TCM cooling design techniques.

The design team faced the dual challenge of implementing a working design in a limited space while progressively enhancing system function and performance as the ES/9000 objectives evolved with time. Important aspects of the system design are described in the last five papers, as follows.

Weinberger discusses an adder design optimized for DCS logic, presenting the design of a carry-lookahead adder to illustrate its versatility. Curran and Walz discuss the system controller and memory subsystem design, with emphasis on the improvements and innovations required to implement it within a single air-cooled TCM. Slegel and Veracca describe the design of the air-cooled Vector Facility and evaluate its performance, presenting specific performance results, while Turgeon et al. present two differing approaches to CMOS array fault tolerance. Finally, the application of new self-test techniques to the 9121 TCMs during manufacturing is discussed by Sarma.

These papers do not present every aspect of design and development of the air-cooled ES/9000 processors, but they describe many of the most important ones. We would like to express appreciation to the authors for the time and effort they spent to enable the *Journal* to publish their contributions to this significant product accomplishment.

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