A 3072 × 32-stage TDI imaging device

by E. S. Schlig

A 3072 × 32-stage TDI charge-coupled imaging device is described. It is believed to be the first reported TDI imager suitable for 300-pel-per-inch document scanning. Its large photocharge capacity gives it the noise performance and dynamic range required for high-quality gray-scale and color imaging in publishing and museum applications. Design options for high-resolution TDI imagers and the uniformity enhancement provided by the TDI mode of operation are discussed.

Introduction

A TDI (time-delay and integration) charge-coupled imager for 300-pel-per-inch document imaging has been designed and prototyped. Its scan width is 3072 pels (picture elements), which is believed to be the widest reported for a TDI imaging chip. The scanned image is integrated over 32 stages, providing a sensitivity advantage of about 10 times over a hypothetical linear imager with the same photosite size. Its large photocharge capacity, which results from the large surface-channel photosites and four-phase double clocking, makes the device suitable for large dynamic range gray-scale and color applications. The imager is in use in a prototype color image scanning camera for high-quality publishing and museum applications [1].

In an earlier paper the advantages of the TDI mode in document imaging were outlined in connection with a 2048 × 32-stage TDI device [2]. The traditional application area of TDI has been aerospace reconnaissance; some examples are referenced [3–7]. That application is characterized by relative insensitivity to cost. The present application to high-quality and high-resolution color imaging, together with the appearance on the commercial market of a number of TDI devices up to 2048 stages wide, suggests that TDI is coming of age, and will compete with linear imagers on the basis of cost per performance for application in new document-imaging products.

For scan widths larger than 2048 pels, TDI imaging chips tend to become uncomfortably long and narrow in physical format, leading to higher manufacturing costs and to problems in chip handling and packaging, and in the design of the optical systems of scanners. The use of bilinear and quadrilinear CCD (charge-coupled-device) structures, and of time-multiplexed serial CCD registers, which permit pel sizes as small as one-quarter the length of a CCD stage in linear photodiode imagers, are not complete solutions to the chip size problem in two-dimensional CCD arrays such as TDI arrays. Such techniques do nothing for the pel size in the vertical dimension, which remains at the CCD stage size. One solution to this problem employs ripple-clocking to approximately double the vertical density of photosites at a given CCD electrode pitch [8]. This solution, while proven viable, creates new problems related to the nature of ripple-clocking.

One problem with ripple clocking is that one photocharge integrating site in each sequence of n is absent, where n is the number of phases used, commonly eight or more. In TDI, because the optical image scans

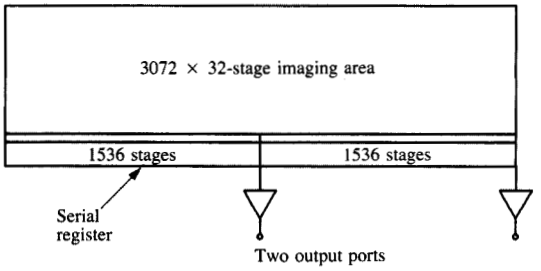


Figure 1

Schematic layout of 3072 × 32 TDI charge-coupled imager.

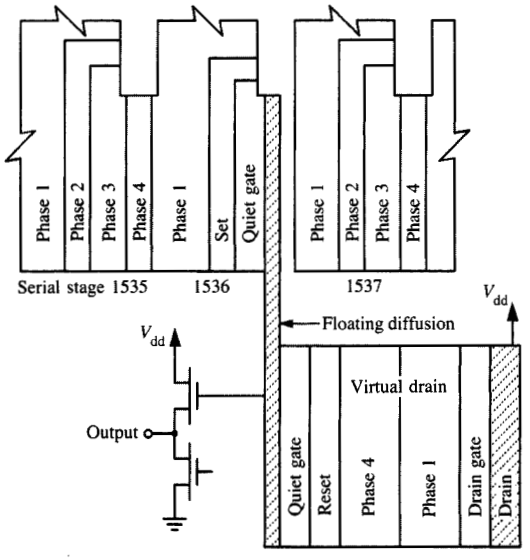


Figure 2

Schematic layout of the central output port and reset channel. Clear regions represent the footprint of the named gate in the buried channel. Crosshatched regions represent diffusions.

vertically across the device, each pel is affected equally by the missing sites. The result is a small reduction in the modulation transfer function.

A second problem is that the photocharge packets are not moved simultaneously in ripple clocking, as they are in normal CCD clocking, but sequentially in ripple fashion. All pels of the optical image move simultaneously. To avoid significant loss of resolution due to periodic loss of coincidence between the optical and photocharge images, the eight or more ripple-clock phase pulses should be generated within a small fraction of the line time [6]. However, the pulse rate is limited by the charging time of the resistive and capacitive polysilicon phase electrodes that are used. Serious scanning speed limitations would result unless the polysilicon electrodes were driven at multiple points within the array by means of diagonal metal lines and metal-to-polysilicon contacts [8] to reduce the charging time. However, the space needed for such contacts would prevent us from designing to minimum layout rules, defeating our purpose of reducing the chip size.

Lacking a clean and complete solution to the long-chip problem, and wishing to retain the large dynamic range resulting from a high photocharge capacity, we chose to retain a single simplex serial register and four-phase clocking in both dimensions, using the same 2-μm, double-polysilicon, double-metal NMOS process used in earlier devices [2]. The result was a 48 × 2-mm chip, by no means the longest imaging chip made today.

Device architecture and design features

The layout of the device chip is shown schematically in **Figure 1**. The imaging area, referred to as the parallel array, comprises 3074 parallel columns of 32-stage four-phase CCD registers, clocked by two-layer polysilicon electrodes; 3072 are true imaging columns, while the first and last column are partially occluded by the metal light shield and deposit their photocharge into a drain diffusion rather than into the serial register. This helps to screen the device from charge diffusing from the sides of the array and to keep the photoresponse uniform at the ends of the true imaging array. The parallel array is surface-channel to maximize the photocharge capacity, which is approximately 0.6 pC per stage. This is equivalent to 3.75 million electrons, providing a signal-to-shot-noise ratio of 1936 at saturation.

The technology provides for an optional upper protective layer of polyimide for the chip surface. We have designed TDI devices both with and without such a layer. Both function well and exhibit similar electrical performance characteristics, but differ somewhat in spectral response. With polyimide, the quantum efficiency is greater at longer visible wavelengths but lower in the blue. The devices described here, intended for color applications, were fabricated without the polyimide layer.

The serial register is a buried-channel four-phase CCD to maximize the speed and transfer efficiency. The parallel-to-serial interface is designed to avoid necking-down of the width of the channel in the interface [2]. The buried

channel is formed selectively by replacing the usual arsenic depletion channel implant of the NMOS process by a phosphorus buried-channel implant.

To take advantage of the speed potential of the device without excessively high serial clock rates, two output ports are provided, at the center and the end of the register, so that only 1536 clock cycles are required per line. The design maximum serial clock rate is 12 MHz, so the maximum composite pel rate is 24 MHz. At that speed a B4-size document (10.1 × 14.3 inches) could be imaged at 300 pels per inch in 0.6 seconds. The serial clock distribution electrodes are split at the center of the device so that the two halves can be driven by separate clock driver circuits. This is helpful at the highest clock rates because the capacitive load on each clock driver circuit is reduced.

The output stages each use a floating diffusion which is reset into a virtual drain consisting of two CCD stages followed by the true drain [2, 9]. A single source follower stage biased by an integral NMOS current source drives each output pad. The floating diffusion itself provides the conductive connection between the final stage of each section of the register and the associated virtual drain channel, which is placed parallel to the serial channel as illustrated schematically in **Figure 2**. This arrangement avoids the deterioration of speed and charge-transfer efficiency which would result from right-angle bends in the channel at the output port, and permits the length of the stages of the serial register which incorporate the floating diffusion to be the same as the normal stages, as governed by minimum design rules. Quiet gates, internally connected to the drain supply voltage, are placed on either side of the floating diffusion to minimize coupling of clock pulses to the output. A 2-V set pulse is applied to the set gate which couples the signal charge to the floating diffusion, instead of the more commonly used barrier potential [2, 9]. The same set pulse is internally connected to the drain gate which couples the charge from the virtual drain to the drain. The output signal at saturation is approximately 0.8 V.

The TDI imaging chip is mounted in a custom 40-pin ceramic dual-in-line package with a crown glass window; 32 pins are used. Although only 24 pins are needed to operate the device at moderate speed, redundant connections are provided because of the length of the chip. A photograph of a packaged chip without the glass window is shown in **Figure 3**.

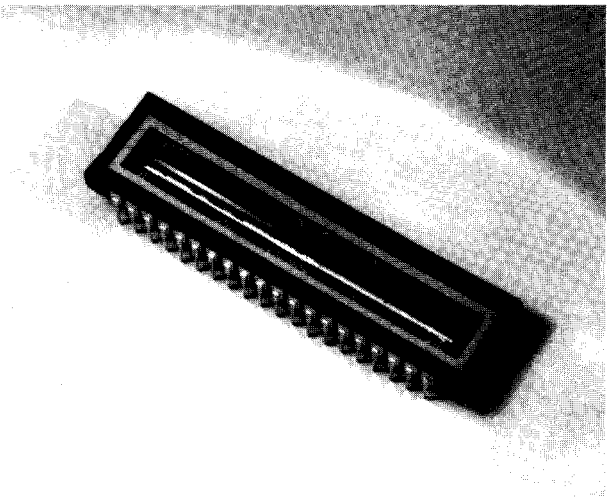


Figure 3

Photograph of TDI imager.

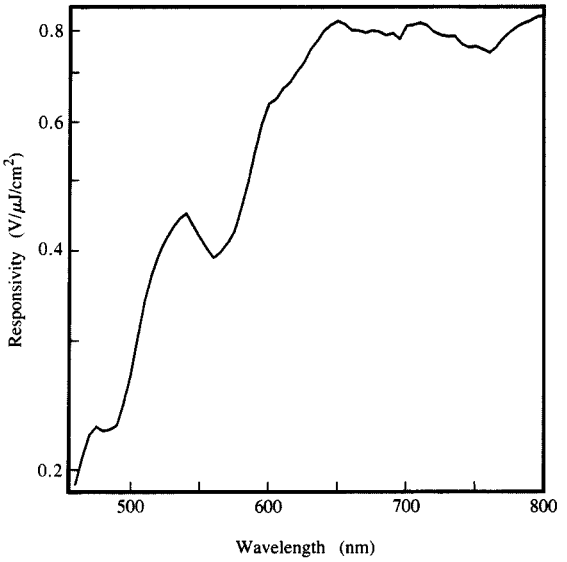
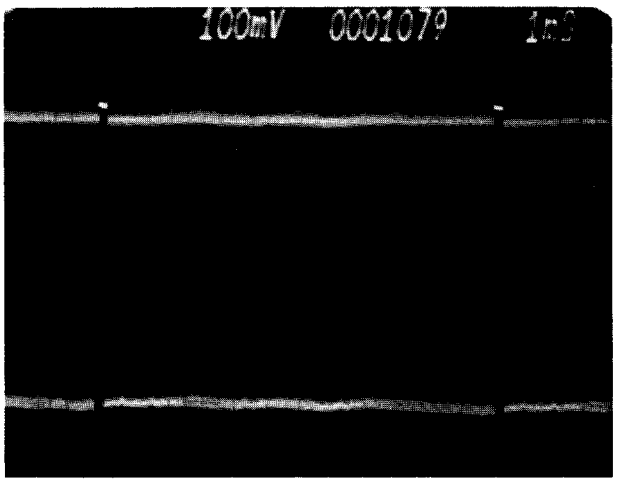


Figure 4

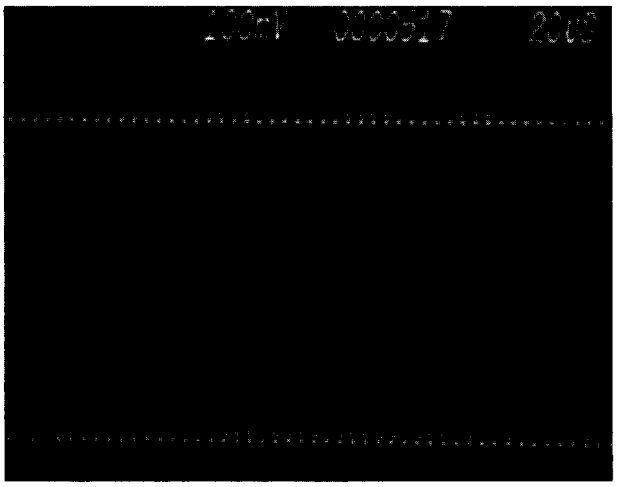
Measured spectral responsivity. Spectral slit width was 10 nm.

Performance

The charge-transfer inefficiencies of the serial register and of the combination of the parallel registers and parallel-to-serial interface are too small to measure precisely. They were estimated by general illumination of the array with the parallel clocks stopped, followed by normal clocking with the array dark to shift the photocharge, one pel at a time, to the output ports. The buried-channel serial register has an inefficiency of about 10^{-6} per phase at moderate frequencies and photocharge packet amplitudes. The combined inefficiency of the surface-channel parallel registers and the interface is about 10^{-4} per phase.



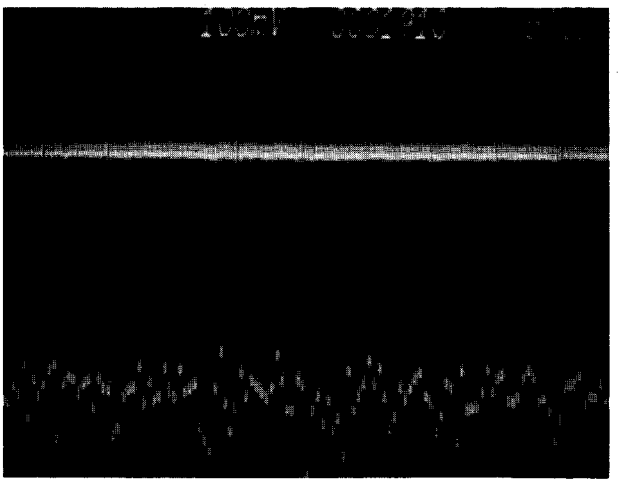
(a)



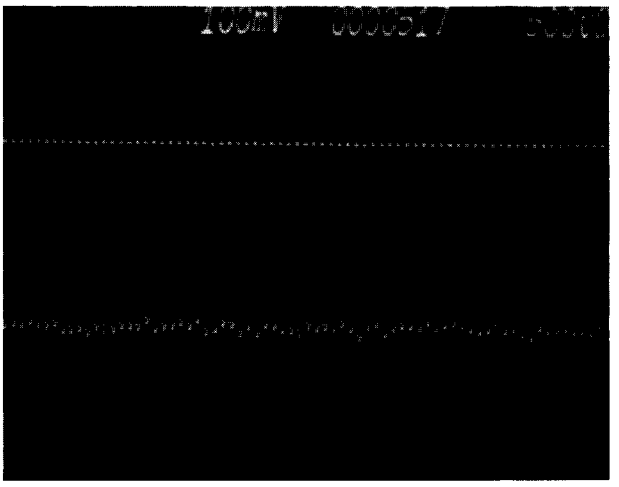
(b)

Figure 5

Oscillographs of output with diffuse uniform illumination, illustrating photoresponse uniformity: (a) Full scan line. (b) Detail of about 50 cycles of the scan.



(a)



(b)

Figure 6

Oscillographs of dark output, illustrating the improved uniformity obtained in the TDI mode: (a) Frame transfer mode. (b) TDI mode. In each case, integration time was 209 s.

The spectral responsivity in the visible is shown in **Figure 4**. Its general shape is characteristic of imaging devices with polysilicon thin-film electrodes over the imaging cells [2]. This responsivity is derived using the total integration time. In these TDI devices the integration time is 32 times the line time, so the responsivity is not a proper basis for comparison with linear devices or other TDI devices. For such comparisons, the use of a scanning responsivity which is the product of the responsivity and the number of integrating stages is more appropriate.

The dark-current density at 25°C is typically less than 1 nA/cm^2, yielding a dark output of less than 3 mV per second of integration time. The devices exhibit the enhancement of the uniformity of dark current and photoresponse which is a feature of the TDI mode, in which local nonuniformities are averaged down by the summation of photocharge due to imaging of each pel in 32 successive photosites. That feature is an important advantage of the TDI mode that has been generally neglected in the literature, which tends to focus on the sensitivity advantage.

Figure 5 shows oscillographs of the unprocessed output obtained with diffuse, approximately uniform ambient illumination, illustrating the photoresponse uniformity. In part (a) a full line scan from one of the two ports, 1536 cycles, appears between the second and eighth division of the time axis. The serial clock frequency is 250 kHz and the line time is 6.3 ms. The upper trace is the reset or

reference level, and the lower trace is the output level representing the incident light. In part (b), about 50 cycles of the output are shown on an expanded time scale.

Figure 6 shows the dark output for a much longer integration time, 209 seconds. The output shown in part (a) was obtained for operation in the frame-transfer mode, so that each output pulse represents the dark charge collected in a single photosite. For part (b), operation was in the TDI mode, so that each output pulse represents the sum of contributions from 32 photosites. The effect of TDI operation on dark-signal uniformity is apparent.

Given the large saturation photocharge and low dark charge, the dark noise imbedded in the output should be negligible with 12-bit resolution at normal integration times. The term "imbedded" implies immunity to filtration and correlated double sampling. With the 250-kHz serial clock rate and 6.2-ms line time of the scanning camera, the dark-noise voltage at the device output in the frequency range of 10 to 300 kHz was not measurable over the 0.5-mV noise level of our equipment; hence, the noise dynamic range is better than 1600. In the scanning camera, after voltage amplification of ten, low-pass filtration to 1 MHz, and correlated double sampling, the system noise dynamic range is 1400.

Conclusions

The 3072 × 32-stage imaging device described here demonstrates that TDI imaging is extendable to high-resolution application areas, such as publishing and artwork image archiving. In color imaging applications, its high sensitivity compensates for the optical density of the color filters used, potentially improving productivity while avoiding the hot incandescent illuminators typically used. The high degree of photoresponse and dark-current uniformity afforded by TDI operation helps to maintain high image quality with a minimum of processing. The large photocharge capability and low dark current lead to a system dynamic range large enough to justify digitization to a level of at least 11 bits.

Acknowledgment

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