On-chip wiring for VLSI: Status and directions

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The thirty-year history of silicon integrated circuits has resulted in dramatic increases in both the number of devices per chip and circuit speed. A consequence of scaling to submicron dimensions is that the major component of propagation delay will transfer from the devices to the interconnecting "wires." Additionally, increased integration, together with scaling, leads to a need for more numerous interconnections on a chip and higher current densities. Accommodation to these changes will necessitate the use of new materials arranged in three-dimensional wiring structures which have the ability to make the most effective use of the area of the chip. Generic processing routes to achieve the desired structures are reviewed and examples are presented of two experimental structures with layers of planar wiring and vertical vias between planes. One of these integrates aluminum-alloy wiring with tungsten vias in a silicon dioxide dielectric; the other integrates copper wiring and vias in polyimide dielectric with the goal of minimizing delay due to on-chip wiring.

Introduction

Very large scale integration (VLSI) is key to the continuing development of the computer industry. Its realization depends upon fabricating and interconnecting ever-increasing numbers of components on silicon chips. The numbers of devices contained in the most densely packed chips have quadrupled with each new generation, every three to four years. At each step, chip size has been increased (by a factor as large as 1.3), and minimum linear feature size has been reduced (by a factor of approximately 0.7) to make this possible. Shrinking the sizes of components has allowed ever greater numbers of them to be fabricated on each wafer, increasing efficiency and reducing cost. A recent review by Lu [1] of developments in dynamic random access memory (DRAM) chips, which use complementary metal oxide semiconductor (CMOS) devices, illustrates the rate of development in this field. Ning and Tang [2] have provided a similar review of advances in the area of bipolar devices.

As VLSI structures are scaled to smaller dimensions, fabrication becomes more complex, but the relative burdens of speed of operation, processing costs, and reliability are increasingly transferred from the active devices to the on-chip interconnections. Simple scaling arguments are used to demonstrate the increasing role of wiring in chip delay. Increasing integration leads to the need for greater numbers of wiring levels for logic chips, with ready access between "wires" at different levels. The use of more wiring levels requires an increased number of processing operations. Greater complexity and reduced dimensions lead to increased concern with both yield and cost. Increased current densities in the finer dimensions lead to increased concern for reliability. In combination,

these requirements result in a need to apply the most effective materials for high-speed performance in structures which provide the greatest freedom in interconnecting devices. The need for multilevel wiring structures fabricated from materials with both good electrical performance and reliability leads to consideration of alternative processes for the deposition of both new metals and dielectrics and for their patterning.

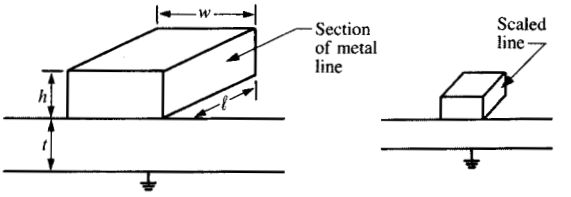
Functions of on-chip interconnections

The functions served by the interconnections can be divided into four parts. The first of these, so-called local interconnections, are used to wire a cluster of adjacent elements, both active devices and passive elements, into a circuit element. These circuit elements may be the storage node of a static random access memory (SRAM) chip or a logic element of a logic chip. A second type of wiring, referred to as global wiring, is used to connect circuit elements. The most demanding use of such lines occurs in logic arrays, where such connections may span the full extent of the chip. It is these longest lines on a chip which limit its overall speed. Third, there are interconnections which carry power to the active devices on the chip. Finally, it is necessary to have a level which acts as an interface with the packaging element on which a number of chips are mounted and interconnected. This interface may either be bonding pads or an area array of solder bumps, which can be joined to a similar array on the packaging element. The final level of wiring usually combines this latter function with a primary distribution of power. As dimensions are reduced, the relative importance of each of these different wiring functions to chip performance, to processing cost, and to overall reliability increases.

VLSI scaling effects

Scaling theory for MOS devices has been developed and applied by Dennard [3]. A scaling factor $K > 1$ is used to reduce linear dimensions by a factor of $1/K$. Ideal scaling of the devices maintains constant electric fields by increasing doping levels as dimensions shrink. A simplified scaling table with emphasis on interconnections is shown in **Table 1**. The upper section of the table records that, as the dimensions of the devices are reduced by a factor of $1/K$, their speed increases by a factor of K. The lower section of the table gives scaling factors for the resistance and capacitance of the interconnections; a subdivision is based on length. Short lines are defined as those which were contained on a chip prior to scaling. The length of such lines scales with the general scaling. **Figure 1** illustrates how line resistance R and capacitance C change upon scaling. Following the work of Bakoglu and Meindl [4], we write for the interconnection delay

$$T \simeq (2.3R_{tr} + R)C,$$



$$C \propto \frac{\varepsilon\varepsilon_0 w\ell}{t} \qquad C_s = \frac{C}{K}$$

$$R = \frac{\rho\ell}{hw} \qquad R_s = RK$$

Figure 1

Illustrative scaling rules for the capacitance and resistance of a metal line. Capacitance is indicated by a proportionality, to allow for a multiplicative factor due to parasitic capacitances.

Table 1 Ideal scaling for CMOS devices and wiring.

Property	*Factor*
Devices	
Dimension	$1/K$
Doping concentration	K
Voltage	$1/K$
Current	$1/K$
Device delay	$1/K$
*Short lines**	
Capacitance	$1/K$
Resistance	K
RC time constant	1
Voltage drop	1
Current density	K
Long lines†	
Capacitance	1
Resistance	K^2
RC time constant	K^2
Voltage drop	K
Current density	K

*length scales as $1/K$
†constant ratio of chip size to line length

where R_{tr} is the device resistance. Because the capacitance of the metal line occurs in two terms, it has a more significant contribution than the line's resistance, and the delay is larger than the simple RC of the line alone. Table 1 shows that the RC time constant for short lines remains constant with scaling. For long lines, the RC time constant increases by a factor of K^2, as indicated in the table. Such lines were formerly used to interconnect chips at the

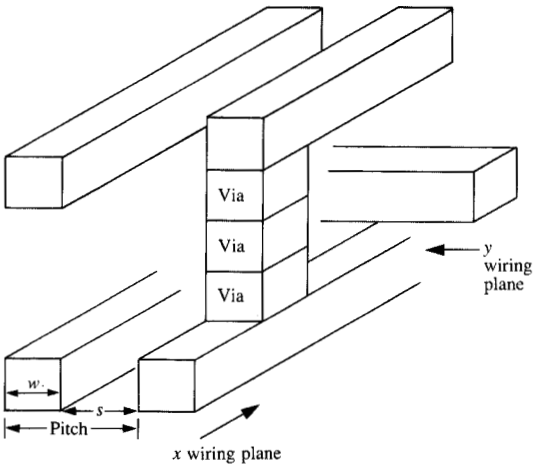


Figure 2

Idealized wiring structure. The metal lines are planar, alternating between the x and y directions on successive planes. The same pitch at successive levels allows easy access between levels.

packaging level, so are not truly scaled. To overcome the delay in long lines, it is usual to use unscaled driver devices; this increases current densities.

Simple scaling of both the devices and the wiring on a chip is not generally followed. In the case of the wiring, there is an incentive to increase the aspect ratio (ratio of height to width) of the metal lines to achieve a finer pitch, while retaining cross-sectional area. As a consequence, the scaling factors in Table 1 are made less unfavorable. Despite an increase in intraline capacitance, overall chip performance, which also depends on chip size, is optimal for cross-sectional aspect ratios in the range 1.0 to 1.5*.

Scaling of MOS devices has been selected as an example because it can be more simply modeled, although such simple scaling is not practiced. Scaling for bipolar devices has been developed by Solomon and Tang [5], while a more general approach to interconnection scaling has also been carried out by Solomon [6]. Major differences in the bipolar case are the use of higher current densities and the need to minimize voltage drops along the lines. Thus, for bipolar devices, the resistive component of the wiring is more important than simple RC delay estimates indicate.

Table 1 also indicates the effect of scaling on current density. Increasing current density leads to reliability concerns due to the phenomenon of electromigration. Momentum transfer between conduction electrons and metal ions results in their transport primarily along grain boundaries. Line failure is believed to occur when a mass flux divergence at grain-boundary triple points initiates formation of a metal void (and ultimately an open line) or when the transported metal extrudes from some point in the structure and causes shorting to an adjacent line.

Over the past twenty years significant improvements in the electromigration strength of fine Al wires have been made. One level of improvement has been made by alloying Al with small amounts of other metals such as Cu. A second method of improvement is to form layered structures between Al and thin layers of a transition metal such as Ti. When annealed, part of the Al adjacent to the Ti is consumed to form an intermetallic compound, $TiAl_3$; such compounds have high electromigration strength. The layers so formed can maintain current continuity even though voids may form and heal again in the main conductor. Both methods of improvement result in an increase in the sheet resistance of the resulting structure; it is unlikely that additional improvements can be made without further compromising this property. The subject of electromigration has been discussed in greater detail by Kwok and Ho [7].

Materials for advanced wiring structures

Improvement of the performance of chip wiring structures requires substitution of new materials with lower dielectric constant and resistivity without compromising the increasing demands for reliability and yield. The materials commonly used today are SiO_2- and Al-based alloys. SiO_2 has a dielectric constant of about 3.9; this is among the lowest among common inorganic materials. Polyimides can be prepared with a range of dielectric constants (the lowest being about 2.9), with the possibility of further reductions. Potential concerns with polymeric materials are their absorption of water or processing chemicals and their mechanical properties. Polymers are more readily deformed by stress than inorganic dielectrics; however, they need not be brittle. It can be beneficial to the mechanical stability of a composite structure of metal and dielectric if the dielectric matrix has a small elastic modulus, thus exerting small stress, and is capable of large extension. Polyimides can play such a role.

There are only three metals with conductivities higher than that of Al: Au, Cu, and Ag. These metals form deep levels in the bandgap of Si, and reliable barrier structures are required to prevent their penetration. It is also important that their electromigration performance be as good as that of the layered Al-based alloys used today. Since these metals all have melting points substantially higher than that of pure Al, their atomic diffusivities are substantially less at device operating temperatures. For this reason either pure metals or simple alloys are expected to be equivalent to the best Al-based systems.

*J. McCabe, IBM General Technology Division, East Fishkill facility, private communication.

Wiring structure requirements

Custom logic is the application which requires the greatest complexity of wiring. There is a well-accepted algorithm, Rent's rule, which relates the number of logic gates to the number of connections, from which may be inferred the number and length distribution of global wires necessary to interconnect the gates [8]. When the level of integration is low, a total of only two or three levels of wiring are required for all wiring functions; global wires are usually mixed with local wires and power wires to provide access to both x and y directions. The required via interconnections between wires running in the two directions are easily made. As the number of levels largely dedicated to global wiring exceeds two, as driven by higher integration, access between pairs of x or y wires at different levels can most readily be ensured if they can be fabricated to lie one above the other. That is, it must be possible to make lines with the same pitch at successive levels. Additionally, to make the best use of space at any level it is preferable that vias connecting between levels be vertical and exact minimal penalty from the pitch. To achieve constant, fine pitch at successive levels requires a high degree of planarization for lithographic processing. **Figure 2** illustrates a section through idealized x and y wiring planes and a via from one x plane to another. The via consists of a stack of two pure vias with a short section (also labeled as a via) of a y-plane line sandwiched between them.

In the figure, it is assumed that the via sections are perfectly aligned between the upper and lower lines. In practice each level is aligned with one of the previous levels. Each such alignment is a member of a Gaussian distribution. In its design, a process must guarantee that chips exhibiting "worst-case" misalignments (defined as six standard deviations) will operate to specification. A simple way to achieve this for a via is to enlarge the wires at via locations so that a worst-case alignment is just contained, as illustrated in **Figure 3**. However, the use of such "bordered" vias increases the wired pitch, which in highly integrated chips would result in decreased circuit density.

Figure 4 illustrates interconnection without the use of borders. A process is assumed in which a via hole is formed by etching down through the dielectric to intersect the underlying metal line, followed by filling of the hole with metal. Since there is also variability in the etching process, the depth of the hole must encompass worst-case variations in both dielectric thickness and etch rate. The resulting shape can be as illustrated. Thus, a further requirement is that the metal deposition process used to fill the via hole must fill the over-etched region.

An additional factor to be considered with borderless vias is that the effective conduction area of the contact may be reduced, while, in common with vertical vias in general, higher current densities occur at the inner corners of even perfectly aligned lines and vias. Both of these effects must be examined for their reliability due to enhancement of electromigration stress.

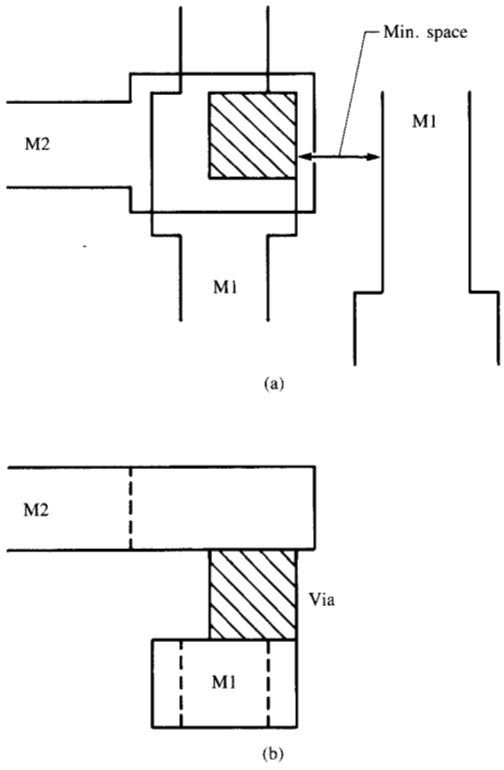


Figure 3

Wiring structures which use bordered vias between their levels to ensure that vias are fully "landed" on wires at the level below: (a) plan view; (b) side view.

Processing routes

Figures 5, **6**, and **7** are simplified illustrations of processing schemes which may be used to achieve the desired structures. Figure 5 shows a sequence in which metal lines are defined, followed by vias on the lines in order to connect to the next metal level. The structure must then be filled with dielectric and planarized before repeating the process. One concern with this scheme lies in the fragility of the free-standing vias prior to deposition of the dielectric; another is development of a process by which a dielectric can be deposited to fill the spaces between the metal structures. This scheme has been described, at relatively large dimensions, by Bartush [9].

Figure 6 illustrates a reverse process, in which first the line pattern, then the via pattern is etched into a planar

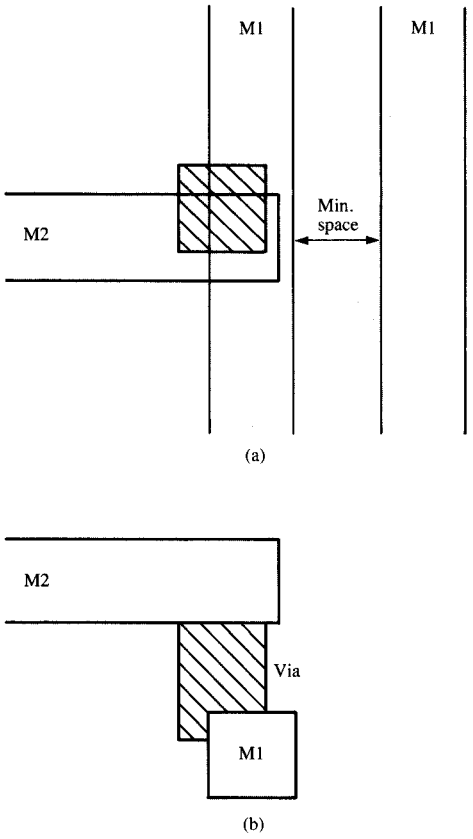


Figure 4

Illustrative vias without borders: (a) plan view; (b) side view.

dielectric. The structure is then filled by metal and excess metal on the upper surface of the dielectric etched away. Here, the difficult process element is filling the spaces in the dielectric with metal. Broadbent [10] and others have used chemical vapor deposition (CVD) of tungsten to fill both defined slots (for lines) and via holes; subsequently excess tungsten was etched from the topmost surface.

A hybrid process is illustrated in Figure 7. In this case, covering the lines with dielectric prior to via formation reduces the potential for damage to free-standing studs. First the lines are defined, then the dielectric is deposited and planarized at a level one via height above the lines. Subsequently a via hole is etched and filled with metal. The aspect ratio for the metal filling is reduced compared to that of Figure 6.

From a consideration of these schemes, critical processes can be identified which are necessary to achieve the desired end result. Such processes must also be compatible with the underlying structure.

Individual processes

Reactive ion etching (RIE) processes are readily available for etching trenches and via holes in both SiO_2 and polyimide dielectrics. Similarly, Al(Cu) conductors can be etched [11] to both the dimensions and the high aspect ratios required. Processes for etching better conductors than Al (Ag, Cu, and Au) are not readily available because these metals do not form volatile species at normal processing temperatures, although a process has recently been reported for etching Cu films [12] at 250°C. One may anticipate similar developments for the other two metals.

Processes which are fundamentally more difficult than etching are those for the deposition of either dielectric or metal into the etched structures. A short review of the options available is presented because of the critical role of these processes in the realization of the desired structures. In general, CVD processes are better able than physical processes to provide depositions which are conformal to the structure of a substrate. It is possible to realize CVD deposition conditions in which the reaction rate is determined by surface kinetics and is thus the same for all points on a contoured surface, rather than being limited by mass transport of the species through a fluid phase. (Mass transport is slower into fine recesses in a surface than to its planar areas.) In the case of SiO_2, a pure CVD process

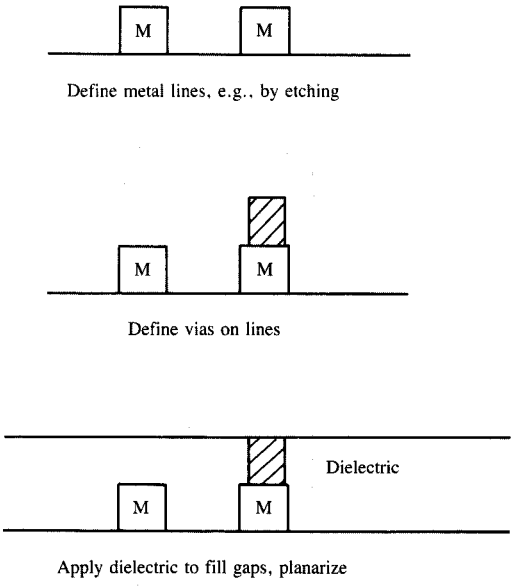


Figure 5

Process sequence which first defines metal lines and vias, followed by a dielectric deposition and planarization.

is not available at the low temperatures dictated by the materials and structure of the substrates. Very substantial efforts have been made to develop physical processes for sputter deposition both to fill spaces [13] and to planarize the resulting surface [14]. Planarization is achieved by simultaneous resputtering from the substrate which, because of the angular dependence of sputtering yield, prevents the formation of surfaces with large angles to the mean plane. The resputtering concept has also been combined with deposition by plasma-enhanced CVD [15]. Similar physical approaches have also been taken to develop processes for metal filling and planarization. Both sputter removal of metal [16] and planarization by radio-frequency bias sputtering [17] have been modeled and studied experimentally. Those processes which rely on sputtering and resputtering ultimately depend on ions with trajectories which are large compared to the dimensions of the holes to be filled, hence limiting the ability to fill such holes. More recently, collimated sputtering has been developed [18] to control the trajectories of the metal ions to be normal to the substrate's surface. These ions have the ability to fill a recess, provided its shape does not present an undercut profile.

In contrast to physical deposition methods, CVD of metals can provide either conformal coatings over blanket coating of a suitable initiation, adhesion layer (normally also a conductor), or even selective deposition onto a patterned layer in a matrix of a dielectric. To date such processes have been extensively developed only for CVD of tungsten [19–21]. The use of this material to fill vertical via holes is described later in this paper. A major disadvantage of tungsten is its high resistivity; for this reason, it is generally used simply for vias to connect between lines etched from Al alloy using a hybrid processing route. The use of different metals for the vias and lines can have deleterious consequences with regard to electromigration. There is necessarily a divergence in the fluxes of material driven by electromigration forces where two dissimilar materials join. In the case of aluminum-alloy lines connected to tungsten vias, voids can be formed in the aluminum at the point of contact with the via material. To avoid such problems in the future, while at the same

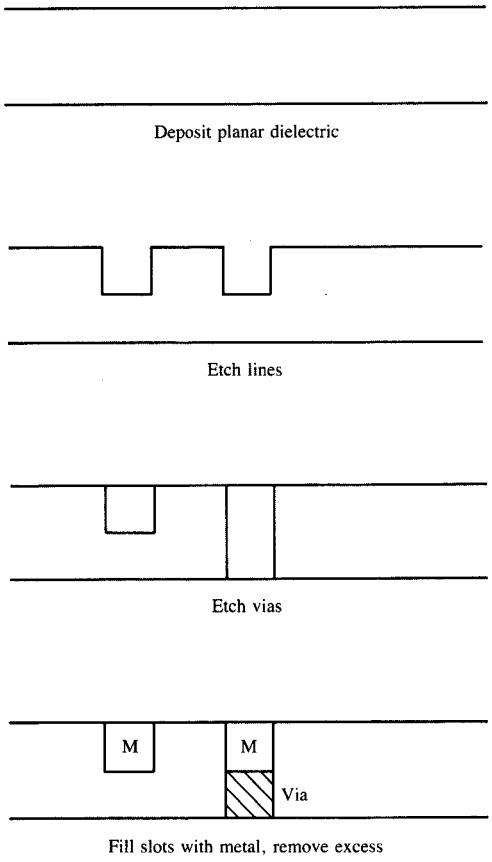


Figure 6

Process sequence which first defines a pattern of lines and vias in a dielectric, followed by metal deposition to fill the pattern.

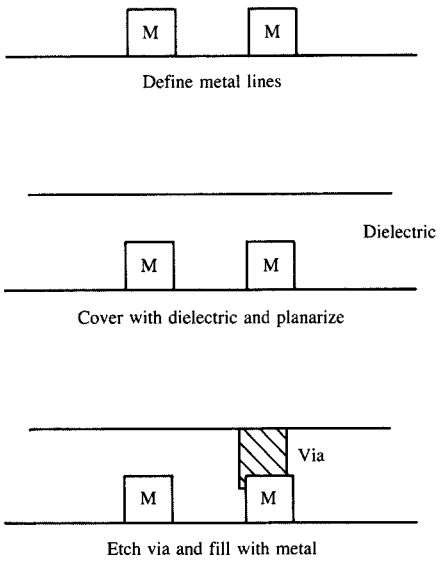


Figure 7

Hybrid process sequence. Metal lines are formed and covered with dielectric, followed by etching of via holes and filling with metal.

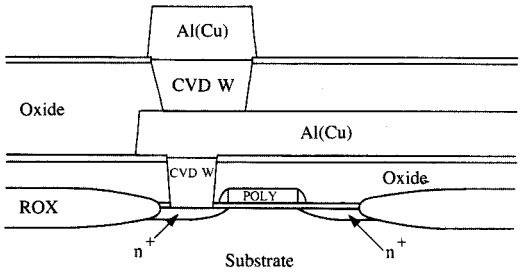


Figure 8

Schematic diagram of experimental wiring structure formed using planarized dielectric, W vias, and Al(Cu) lines.

time obtaining improved performance and the greatest flexibility of processing routes, it is highly desirable to have well-developed CVD processes for the better conductors. There are publications that demonstrate the feasibility of such processes for Al [22], Cu [23–26], and Au [27, 28]. It is anticipated that these processes will develop rapidly in the future.

Process examples

The preceding review has described potential structures and materials for future wiring structures. Associated processing routes and the critical elements of each of these routes have been described in largely generic terms. In what follows, results are presented for experimental structures, fabricated at the IBM Thomas J. Watson Research Center, which were aimed at achieving the indicated goals. Many associated process details are currently confidential. Nevertheless, it is hoped that the material presented will stimulate similar efforts in other laboratories and among the manufacturers of process tools, with whom we share a common goal to develop associated tools and processes.

Before the experimental structures were used on actual circuit chips, several were fabricated using a test site consisting primarily of comb/serpentine structures for determining continuity and shorting in long lines, and via chains for determining interlevel continuity and contact resistance. These test structures were fabricated over a range of horizontal ground rules, with critical dimensions ranging from 0.7–1.3 μm.

After the processes were exercised on test sites, they were applied to experimental chips containing a selectively scaled 64Kb CMOS static RAM design. The circuits on the chip were designed using 1.35-μm ground rules [29] with gate level selectively scaled to 0.7 μm [30] to yield an effective device channel length of 0.5 μm. Minimum dimensions for the wiring were as follows: 1.2 μm for contacts, 1.4-μm line width and spacing for the first metal level, 1.4 × 1.9-μm interlevel vias, and 1.9-μm linewidth and 5.7-μm line spacing for the second metal level. Accompanying the SRAM design were parametric test sites for obtaining FET characteristics, sheet resistance, contact resistance, and yield measurements at a variety of horizontal ground rules.

- *Aluminum-alloy wiring with tungsten vias in silicon dioxide*

In this process, wiring fabrication begins following formation of titanium silicide contacts to the silicon devices and passivation by a SiO_2 film. Additional SiO_2 is then deposited by plasma-enhanced CVD (PECVD) and planarized by chemical mechanical polishing [31] to provide global thickness uniformity of ±10% over the wafer (**Figure 8**). PECVD silicon nitride is deposited as a barrier against mobile ion diffusion and as the second component of a dual dielectric. Contact-hole lithography is followed by RIE of the nitride/oxide dielectric to form vertical contact hole openings to the silicide contact layer on both diffusions into the silicon, and to polycrystalline silicon lines. The RIE process is designed to produce wall angles of approximately 85° to eliminate void formation during CVD of tungsten.

Sputtered Ti/TiN is deposited as a contact and adhesion metallurgy followed by CVD of tungsten at 430°C to produce a 1.0-μm-thick film. An etchback process is performed after W deposition to remove both W and Ti/TiN from the field and leave the contact vias.

A layered structure based on Ti/Al(Cu) is deposited by room-temperature dc magnetron sputtering and is patterned by RIE. Following patterning of the first level of metallization and resist removal, a PECVD oxide interlevel dielectric is deposited and planarized as before, and coated with Si_3N_4. Subsequent via formation and second-level metal patterning is performed by repeating the processes described previously to yield the final structures shown in **Figures 9** and **10**.

- *Copper wiring and vias in polyimide*

In this process, planar copper–polyimide wiring is fabricated to produce the structure shown in **Figure 11**. The tungsten contact level via for this structure is the same as that used in the previously described Al(Cu)/SiO_2 process. The W via structure provides an additional barrier against Cu diffusion into the silicon.

The insulator structure used is a trilayer structure of PECVD Si_3N_4/polyimide/PECVD Si_3N_4. The dielectric constant of the spin-cast polyimide has been measured between 2.8 and 3.1, with the variability in the measurement due primarily to varying solvent and water content. The thin Si_3N_4 in these layers serves several functions:

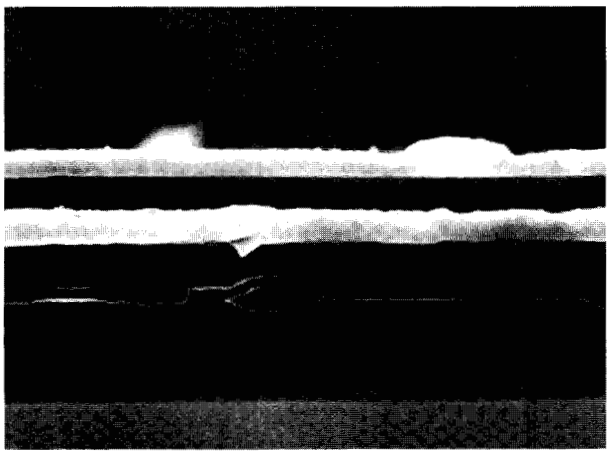


Figure 9

Scanning electron micrograph of a cross section of the structure of Figure 8. Ragged edges of the metal lines are due to tearing during sample preparation.

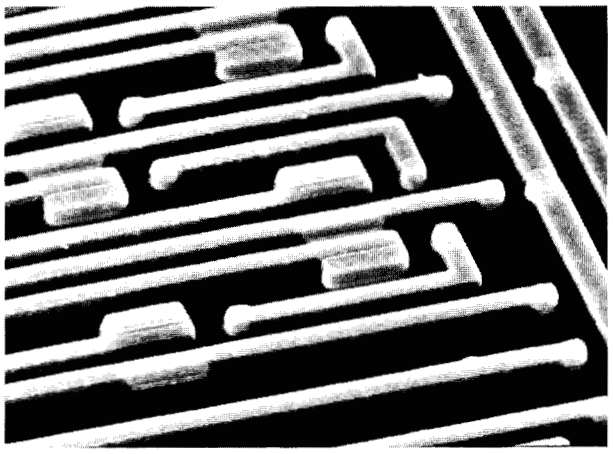


Figure 10

Angled scanning electron micrograph of a wiring plane on an experimental 64Kb SRAM chip. Minimum line width is 1.3 μm. The enhanced backscatter from the W vias highlights them.

- It is a Cu diffusion barrier.
- It forms an adhesion layer between polyimide layers.
- It suppresses Cu hillock formation.
- It prevents solvent adsorption by a completed polyimide layer during subsequent processing.

The metallization is a bilayer consisting of a thin ($\simeq$50 nm) tantalum layer and a greater thickness of Cu. The Ta acts as both an adhesion layer and a diffusion barrier for Cu [32]. It is important to note here that the Cu lines are nominally encased in a combination of Ta and silicon nitride regardless of process variations such as level-to-level overlay or RIE overetch. Also important is the fact that the polyimide is completely passivated at all times; any process step which exposes polyimide to the environment is followed by a low-pressure bake-out cycle and application of a barrier layer. While no system of barrier layers is defect-free, this combination of barriers and process steps is designed to minimize the exposure of Cu and polyimide to the external environment.

Contact resistance and device characteristics were virtually the same as those obtained with the Al/SiO_2 structure, as would be expected using the same contact level structure. For via chains between Cu conductor levels, the total resistance of a line segment plus via was not measurably different from the value calculated using the bulk resistivity of Cu (2.0 $\mu\Omega$-cm). That is, the contact resistance was not measurable by such a structure.

Functional testing of this structure on the 64Kb SRAM design gave bit yields of more than 90% on some chips. The internal access time of the chip was the same, within

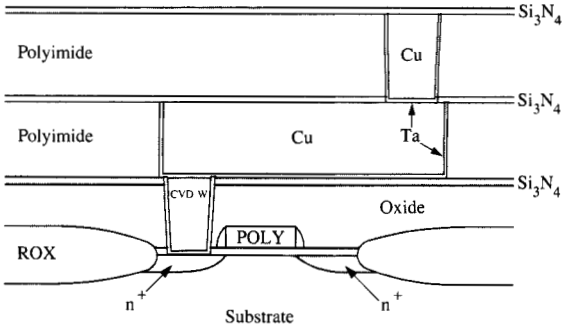


Figure 11

Schematic diagram of experimental Cu–polyimide wiring structure.

experimental error, as previously. One would not anticipate a significant improvement because of the relatively large horizontal dimensions used. Also degrading the performance was the PECVD Si_3N_4 used as part of the dielectric. This is an excellent material from a process standpoint, but its higher dielectric constant compromises electrical performance, and a replacement material is being sought. **Figure 12** shows a view of the wiring structure, while **Figure 13** contains a more highly magnified view of the array area.

Figure 12

Micrograph of a single level of Cu wiring in polyimide on an experimental 64Kb SRAM chip.

Figure 13

Micrograph of portion of array area of chip shown in Figure 12.

As qualitative evidence for the stability of the Cu–polyimide wiring structure, several test sites were subjected to 12 thermal cycles (30 min at 400°C) to simulate further processing and 100 cycles to 77 K as a first-pass test of structural and electrical stability. There was no evidence of notching, voiding, or distortion of the Cu lines due to excessive mechanical stress. Furthermore, no significant change in overall line or via chain resistance was observed following these thermal cycles. The structure was also tested for Cu penetration into underlying devices. Diode reverse leakage measurements at 77 K both before and after annealing at 400°C for 16 hours revealed no evidence of any metal contamination.

Conclusions

The case has been made that as VLSI is scaled to increasingly small dimensions, the signal delay due to the wiring on a chip will become dominant compared to that due to the active silicon devices. At the same time, the increasing level of integration will require a greater number of wiring levels. To satisfy these demands will require, first, the ability to fabricate planar structures with the same wiring pitch at a number of levels; and second, the ability to fabricate such structures with a combination of new materials for use in this application. An experimental structure is reported that satisfies the first of these goals. The structure contains Al(Cu) lines with tungsten-filled vias in a SiO_2 dielectric. Also reported is the first realization of a Cu–polyimide structure en route to the second goal. It is clear that an expanded menu of process options, such as low-temperature CVD of the better-conducting metals, or alternate processes for their conformal deposition into dielectric structures, is highly desirable to reach the goals outlined. Although the complexity of the process options and their possible interactions make it difficult to predict future directions, our opinion is that future chip wiring will likely contain structures similar to those described here.

Acknowledgments

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