Selective epitaxial growth of silicon and some potential applications

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In the selective epitaxial growth (SEG) of silicon, growth occurs only on exposed silicon areas of a silicon substrate. Substrate regions on which silicon growth is not desired are masked by a dielectric film, typically silicon dioxide or silicon nitride. Use of the process permits the fabrication of novel silicon devices and integrated-circuit structures. In this paper, an overview is presented of our studies on the SEG process at the IBM Thomas J. Watson Research Center. Aspects covered are the kinetics of the process using a $SiCl_4$ and H_2 gaseous mixture, the associated suppression of deposition on silicon dioxide and silicon nitride, and some potential applications of the process to the fabrication of bipolar devices and dynamic random access memory (DRAM) cells.

Introduction

The SEG of silicon on silicon surfaces is a process in which the nucleation and growth of the material on silicon dioxide and silicon nitride is avoided, thus permitting the fabrication of novel silicon device structures. Recent efforts on the SEG process have led to the production of high-quality silicon films at moderate growth temperatures (850–950°C) with excellent selectivity.

An overview of the evolution of the process has been presented by Borland [1]. We mention only a few key aspects of that evolution. In 1962, Joyce and Baldrey [2] first reported selective epitaxial growth of silicon at atmospheric pressure and 1200°C using $SiCl_4$ and a silicon dioxide mask. In 1965 Jackson [3] added HCl to the $SiCl_4$ to inhibit spurious nucleation of silicon on the oxide mask. HCl presumably etches away every small nucleus of silicon before it can grow and coalesce with another nucleus. This technique, along with the alternation of HCl etching and silicon growth in a grow/etch series of cycles, was used for some years as a means for achieving SEG [4–6]. However, relatively high growth temperatures were required, and good reproducibility was difficult to achieve.

A major advance in the SEG process occurred in 1982 when Tanno et al. [7] first reported on the use of $SiCl_2H_2$ at a reduced pressure (80 torr) in a commercial epitaxy

reactor. The use of deposition temperatures below 1000°C was shown to produce smooth films. The addition of HCl continued to be necessary to control selectivity, maintain planarity, and reduce stacking fault density. In 1984 McGinn et al. [8] showed the importance of pattern orientation on defects in SEG-grown material. Defects which appear along the interface between the dielectric mask edges and the SEG area could be eliminated by orienting the mask edges in a ⟨100⟩ direction. By 1985 Borland and Drowley [9] had reported SEG deposition at temperatures as low as 826°C at a pressure of 26 torr. In 1987 Ginsberg et al. [10] showed that high-quality SEG-grown material could be deposited at a reduced pressure (40 torr) using $SiCl_4$ without the addition of HCl. More recently SEG has been reported at temperatures as low as 600°C using experimental chemical vapor deposition (CVD) systems. The systems employ ultra-clean environments [11], ultra-low pressures [12], or limited reaction processing [13]. Berkenblit et al. [14] have shown that SEG using $SiCl_4$ is feasible at atmospheric pressure.

Device fabrication using silicon films produced by the SEG process began in the late 1960s, shortly after the first reports on the process. Although the process has not yet been used in manufacturing, a number of novel device and integrated-circuit structures have been formed through its use, exploiting the above-mentioned improvements in selectivity, material quality, and reduced growth temperatures.

Potential applications of the process in the formation of silicon devices and integrated circuit structures can be broadly divided into the categories described below, although most fall into more than one category.

1. Applications that require the ability to selectively deposit silicon onto exposed silicon regions within openings on a silicon wafer. The primary requirement here is that it be possible to dope the deposited silicon to make it electrically conductive; the need for the deposited material to be defect-free is of secondary importance. It can be in the form of a single-crystal silicon or polycrystalline silicon ("polysilicon"). The following are examples of such applications:

   - Replacement of local silicon oxidation [15] and filling of deep trench structures [16, 17] in order to achieve device and circuit isolation.
   - Refilling and planarization of contact holes [18].
   - Formation of elevated source/drain structures [19, 20].
   - Formation of silicon gates in CMOS circuits [21].
   - Formation of an epitaxial emitter window of a bipolar transistor (described later).

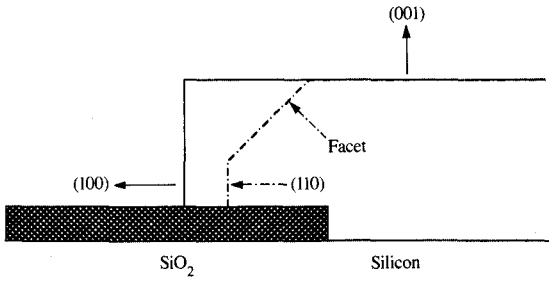


Figure 1

Epitaxial lateral overgrowth. Solid line represents overgrowth with crystallographically identical horizontal and vertical planes. Broken line represents growth along a <110> direction. Note formation of facet in the latter case.

2. Applications that require the ability to selectively deposit defect-free, device-quality silicon. Examples are

   - Formation of a retrograde well in a CMOS structure and an intrinsic base in a bipolar transistor, as an alternative to their formation by means of ion implantation [22–25].
   - Formation of a very compact DRAM cell (described later).

3. Applications that are based on an extension of the SEG process, designated as the epitaxial lateral overgrowth (ELO) process, in which an opening in a dielectric layer can be used as a "seed" area for the selective growth of silicon. Growth occurs in the seeded area and is continued until it spreads laterally over the dielectric layer. If the edges of the insulation layer are oriented so that the horizontal and vertical planes are crystallographically identical, e.g., (100) horizontally and (001) vertically, equal growth rates can result for both directions. This is depicted in **Figure 1** for an oxidized silicon wafer containing an opening in its oxide layer. (Although it is also possible for facets to form as the result of differing growth rates for other crystallographic planes, such as the {111} planes [26], their formation can be minimized by varying deposition conditions.) If the overgrowth is continued for a sufficient time, it is possible for the epitaxial silicon from adjacent seed regions to meet and coalesce, in effect forming single-crystal material over a buried oxide layer. This then is an alternative means for forming SOI (silicon-on-insulator) structures. A number of papers have reviewed the merits and problems of the ELO process as applied to such structures [27–29].

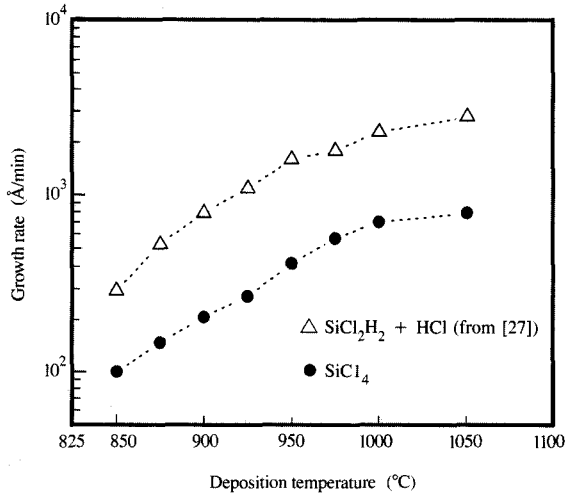


Figure 2

Silicon growth rate vs. temperature for $SiCl_4$ and $SiCl_2H_2$ processes.

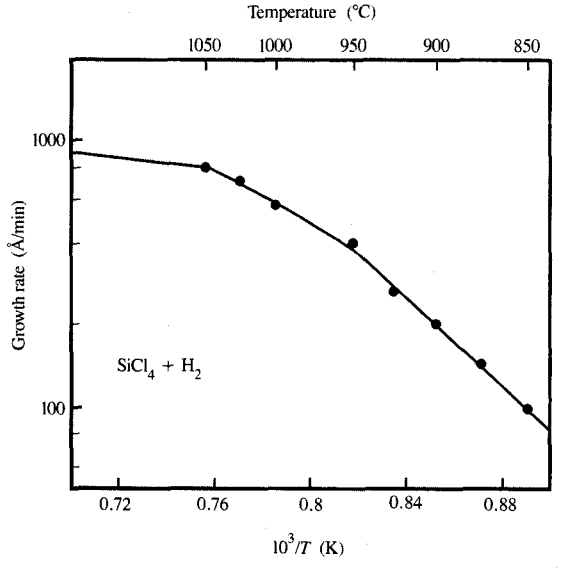


Figure 3

Arrhenius plot of $SiCl_4$ process at 40 torr.

This paper contains an overview of our studies of the SEG process at the IBM Thomas J. Watson Research Center, including studies of its materials aspects and its potential applicability to the fabrication of several types of silicon devices and integrated-circuit structures.

The selective epitaxial growth process

• *Process parameters and tooling*

A conventional reduced-pressure epitaxial reactor of "barrel" design, consisting mainly of a large quartz bell jar, was used to fabricate the device and circuit structures described in this paper. Wafers (12 in the case of 125-mm-diameter wafers) rest on a silicon-carbide-coated graphite susceptor. The susceptor is in the form of a six-sided truncated pyramid. Two wafers rest in shallow pockets on each face of the susceptor, held in place by the taper of each side. The bell jar is surrounded by quartz halogen lamps, which heat the susceptor and wafers by infrared radiation. Gases are introduced at the top of the bell jar and exit below to a pumping system. Temperature, pressure, and gas flows are computer-controlled.

We have chosen to use the $SiCl_4 + H_2$ reactant system in our SEG work. Although it is one of the earliest combinations used in epitaxial deposition, it lost favor to less chlorinated silicon sources, such as dichlorosilane ($SiCl_2H_2$), because of their higher deposition rates at any given temperature. This became a factor as the temperature of epitaxial depositions fell to the 1050–1100°C range and relatively thick films were required. Two factors argue for the reconsideration of $SiCl_4$ as a silicon source. First, the scaling down of silicon device dimensions, both horizontally and vertically, calls for thinner epitaxial films, to micron and submicron thicknesses. The lower deposition rates which result with $SiCl_4$ improve thickness control when the thinner films are being grown. Second, in the case of selective epitaxy, processes which use less chlorinated silanes require the addition of HCl to ensure selectivity, although this depresses the deposition rate. The $SiCl_4$ process does not require the addition of HCl to achieve selectivity. The result is that the deposition rates of selective epitaxy, under similar conditions of temperature and pressure, are not very different for $SiCl_4$ and other chlorinated silanes, especially at the lower temperatures typically used in SEG. This is illustrated by the growth-rate curves in **Figure 2**.

The elimination of the HCl has certain advantages. It is a difficult gas to purify and is a potential carrier of metallic contamination. It can also damage pumping systems and scrubbers. To ensure selectivity and reasonable uniformity, a sufficient amount of HCl must be added to saturate the reactor during deposition. The resulting high level of HCl exacerbates the problems inherent in its use. In the $SiCl_4$ process, four HCl molecules are produced for each deposited silicon atom. This self-generated HCl is sufficient to ensure selectivity over a wide range of process parameters.

The overall stoichiometry of the reaction is

$$SiCl_4 + 2H_2 \leftrightarrow Si + 4HCl,$$

with the formation of many intermediate silanes both chlorinated and unchlorinated. Note that this reaction can proceed in both directions; the etching created in the back-reaction is important in providing selectivity. **Figure 3** contains an Arrhenius plot of the $SiCl_4$ growth process at 40 torr using 1.88 g/min of $SiCl_4$ flow, typical conditions for the work described in this paper. The change in slope which occurs between 925°C and 950°C is the result of the transition from a reaction-rate-limited to a mass-transport-limited regime. **Figure 4** contains plots of growth rate vs. $SiCl_4$ flow rate at several temperatures and at a pressure of 40 torr. Hydrogen background flow rates were the same for all conditions, viz., 120 L/min. Note the increase in growth rate with $SiCl_4$ flow rate; the magnitude of the increase is a strong function of temperature. Growth rates increase by a factor of two at 850°C and a factor of three at 950°C over the range of our $SiCl_4$ flow controller. The process remains selective for all of these conditions.

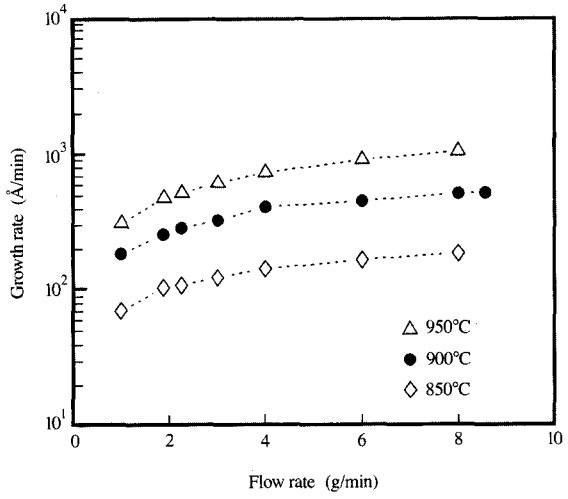


Figure 4

Growth rate vs. $SiCl_4$ flow rate at several temperatures, at a pressure of 40 torr.

- *Pre-clean and pre-bake*

Since the $SiCl_4$ process is selective, it is essential that all traces of oxide be removed from areas where good-quality silicon is to be grown. Residual traces of native oxide will prevent the growth of silicon. If the native oxide is discontinuous, in the form of small islands of oxide, these islands can become embedded in the film and lead to the generation of extended defects such as stacking faults. Removal of residual oxide is ensured as follows: First, the wafers are dipped in a dilute $HF:H_2O$ bath followed by a DI water rinse and spin dry. Second, a bake is performed in the epitaxial reactor in a hydrogen ambient. This bake volatilizes the oxide by forming SiO [30]. Its temperature and duration depend on the pressure and the cleanliness of the reactor as well as the level of residual water vapor which may be present in the hydrogen. We have found that a 950°C five-minute bake is sufficient in our system to ensure the growth of device-quality epitaxial silicon.

Some potential applications of the process

- *Formation of epitaxial emitter window*

A critical step in the fabrication of bipolar transistors is the formation of an emitter window. It must be opened in a layer of polysilicon which serves as contact to the base of the transistor (extrinsic base). Future transistors will require very narrow, submicron emitter openings and sub-100-nm basewidths. Emitter widths down to 0.1 μm have been achieved using electron-beam lithography [31]; however, the low throughput of electron-beam lithography systems makes conventional optical lithography more attractive for practical manufacturability. By using a version of the SEG process, designated as the selective-epitaxy emitter-window (SEEW) process, deep submicron emitter openings have been formed using optical lithography [32]. The process makes use of two aspects of the SEG process, namely the absence of nucleation and growth on Si_3N_4, and the equal rates of epitaxial overgrowth in the vertical and horizontal directions when the emitter window is aligned along the ⟨100⟩ directions of the wafer surface. The midtemperature range of 800–900°C that is used is low enough to allow prior formation of intrinsic base profiles that broaden only slightly during growth.

Figure 5 illustrates the key steps in the SEEW process. Starting with a (001) wafer surface, the collector area is defined by a recessed oxide (ROX) or similar isolation scheme. The intrinsic base is then formed by *in situ* boron-doped, low-temperature epitaxy (LTE) [33]. Since the epitaxial silicon is nonselective, it nucleates as polysilicon on the ROX, as shown in Figure 5(a). A stripe of thin nitride on a thin pad oxide is defined by optical lithography (aligned along a ⟨100⟩ direction) and a short dry-etching step [Figure 5(b)]. Next, selective epitaxial silicon with a high boron concentration is deposited at a temperature of 850°C. To minimize the heat cycle, which might broaden the profile of the intrinsic base, no pre-bake is used prior to deposition. The deposited material is used to define the geometry of the emitter window opening and to provide

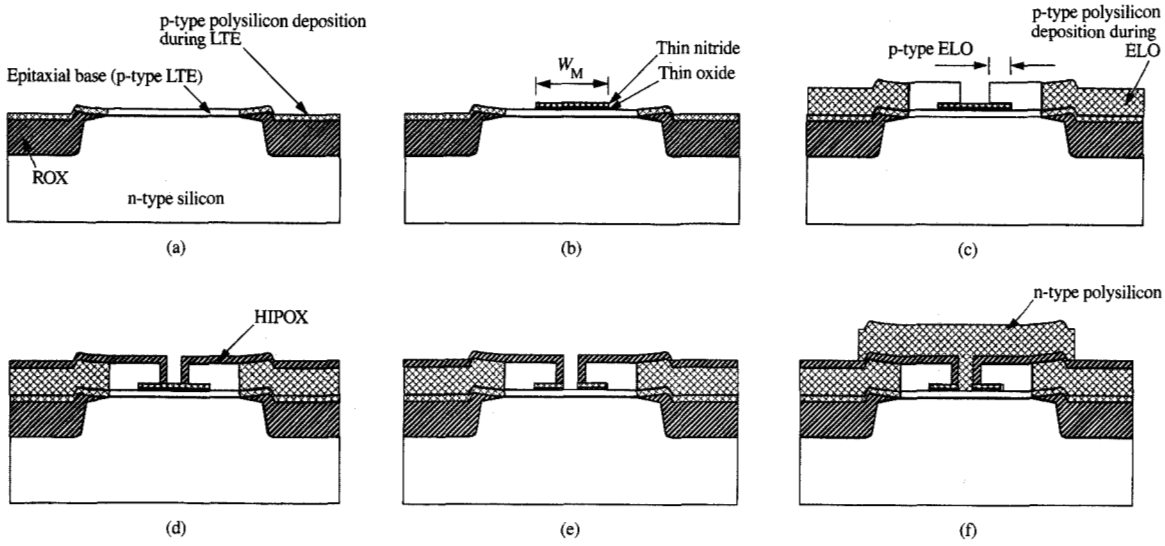


Figure 5

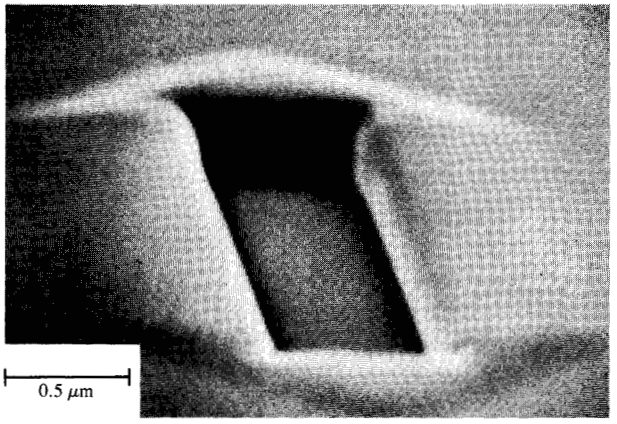
Key steps in SEEW process: (a) concurrent formation of epitaxial base and polysilicon layer; the latter on ROX (recessed oxide) regions; (b) formation of oxide/nitride pad which defines active device region; (c) selective epitaxial overgrowth: (d) formation of HIPOX (high-pressure oxidation) layer; (e) formation of emitter window by dry etching; (f) formation of n-polysilicon emitter. From [34], reproduced with permission. © 1991 IEEE.

electrical contact to the base of the transistor (extrinsic base). Thus, a pre-bake for suppression of crystal defects is not required.

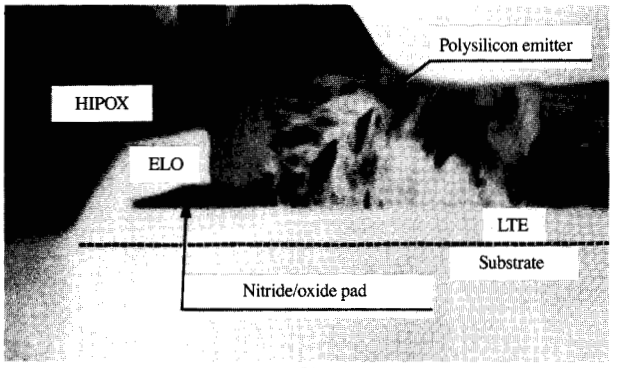
As described previously, the orientation of the emitter stripe in a ⟨100⟩ direction results in lateral growth dominated by {100} planes that grow at the same rate as the (001) planes parallel to the wafer surface. This results in equal lateral and vertical growth rates and an emitter opening having vertical sidewalls [Figure 5(c)]. Since the growth rate in ⟨110⟩ directions is low, no facets appear at the corners, and a controlled rectangular overgrowth is obtained. The nitride/oxide stripe which defines the emitter opening has a thickness of 34 nm and a typical width [W_M in Figure 5(b)] of 0.6 μm to 1.0 μm. The thickness of the selective epitaxial silicon film is typically 180 nm; this reduces the emitter opening by about 0.3 μm. The selective epitaxial silicon is *in situ* doped with boron to a level of 2×10^{19} cm^{-3} to form a self-aligned extrinsic base contact.

The selective-epitaxial extrinsic base is isolated from layers which are to be deposited above and into the emitter window by a 120-nm-thick oxide grown by high-pressure oxidation (HIPOX), as shown in Figure 5(d). This oxidation further reduces the emitter width by about 0.1 μm. Oxidation of the intrinsic base is prevented by the presence of the partially overgrown nitride pad. The emitter window itself is then opened by selective dry etching of the nitride, followed by a brief wet etch of the thin oxide pad [Figure 5(e)]. This is followed by a polysilicon deposition that forms the emitter after arsenic ion implantation and activation [Figure 5(f)].

Figures 6(a) and **6(b)** contain scanning electron microscopy (SEM) and transmission electron microscopy (TEM) images of an emitter window opening produced by selective epitaxy. They illustrate the vertical sidewalls and rectangular overgrowth that is obtainable. The emitter window size of an SEEW transistor can be estimated by electrical measurement if the collector current density is uniform: The collector currents I_C of transistors that have the same emitter pedestal length L_M but different widths are proportional to the emitter width W_E. Therefore, the extrapolation to $I_C = 0$ in **Figure 7(a)** indicates the effective emitter-width reduction ΔW_E, the reduction from the width W_M on the mask used to define the emitter to the width W_E. The dominant growth in the (100) direction at the four sides of the emitter window [Figure 6(a)] requires that the same reduction ΔW_E apply to the emitter length $L_E = L_M - \Delta W_E$. Variations in the collector current of a particular transistor can be due to variations in the ELO, lithography, HIPOX layer, dry etching process, or its vertical doping profile. The calculated maximum emitter-width tolerance is shown in **Figure 7(b)** [34]. The measurements represent a worst-case tolerance of 0.07 μm (σ), which indicates that emitter formation down to 0.2 μm is possible using the SEEW process.



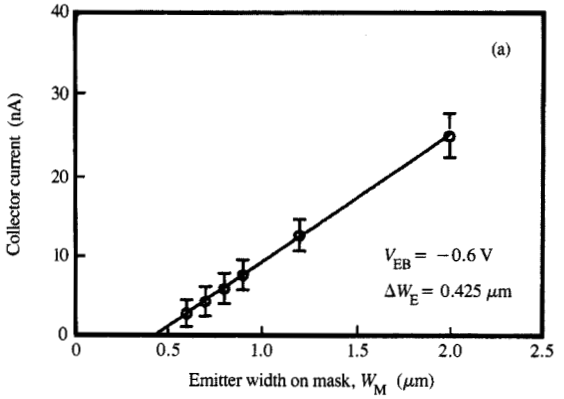
(a)



(b)

Figure 6

(a) SEM image of emitter window opening formed by selective-epitaxy emitter-window (SEEW) process; (b) TEM image of cross section of window. From [34], reproduced with permission. © 1991 IEEE.



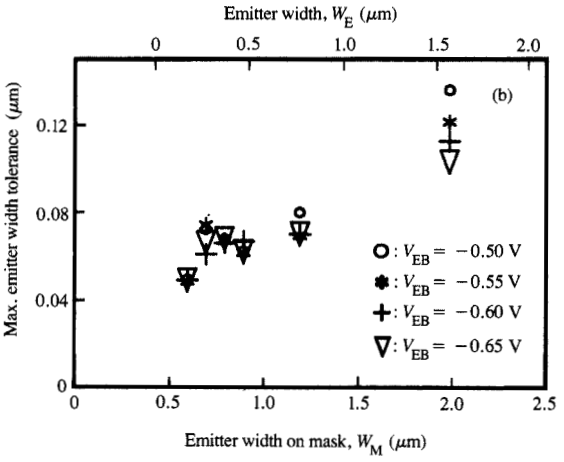


Figure 7

(a) Electrical determination of effective emitter width; (b) estimate of a worst-case tolerance of emitter width. From [34], reproduced with permission. © 1991 IEEE.

• *Formation of epitaxial base*

A key requirement for continued scaling of bipolar devices is the ability to produce narrow base widths. To lower base transit times while avoiding collector-emitter punchthrough, a sufficient doping level in the intrinsic base, with an abrupt profile, is desired. If ion implantation is used to form the intrinsic base, the base width is broadened by channeling and defect-enhanced diffusion [35]. Such broadening does not occur for an *in situ* doped epitaxial base. However, it is difficult to introduce a nonselectively grown epitaxial base into a conventional double-poly self-aligned transistor structure because of problems associated with emitter sidewall formation. Although the use of a selective-epitaxy process to form the base can provide advantages, facets and defects along the edges of selective-epitaxial material grown in insulator-defined openings and wells can form [36]. These perimeter-related difficulties have discouraged the use of selective epitaxy for base formation. An experimental bipolar transistor, designated as the SEBT (selective-epitaxy base transistor) [37] avoids these problems by excluding the defective perimeter area of the base from the active device area. In addition, in the SEBT, faceting is minimized by forming the selective-epitaxy base in a well bounded by the polysilicon extrinsic base, rather than by a dielectric sidewall. The disadvantage of the process is an uneven growth of some silicon crystallites at the epitaxial silicon/polysilicon interface. If the ensuing surface roughness becomes too large, it is difficult to form the sidewall that is necessary to isolate the extrinsic base from the emitter. If the epitaxial film is thin enough, the surface roughness is small and can be reduced by subsequent sidewall formation.

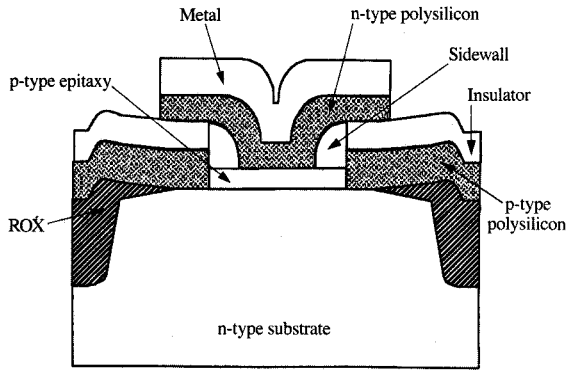


Figure 8

Cross section of experimental selective-epitaxy-base transistor. From [37], reproduced with permission. © 1988 IEEE.

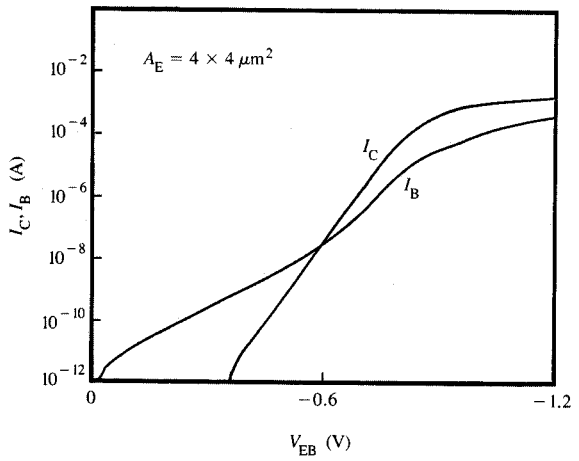


Figure 9

I–V characteristics of experimental selective-epitaxy-base transistor with a 110-nm base width.

SEBTs were fabricated in n-type 0.3–0.7-Ω-cm (100) substrates. After formation of a recessed oxide (ROX), a structure was formed that consisted of polysilicon followed by an insulating film. Boron doping of the polysilicon was achieved by ion implantation. The emitter window was defined by conventional lithography and etched to the substrate using reactive ion etching. A sacrificial oxide was grown and removed prior to the selective epitaxial base deposition at 900°C. After base definition, the sidewall spacer was formed. It had to be thick enough to cover defects and rough spots along the perimeter and exclude them from the active device region. Conventional polysilicon-emitter methods were subsequently used. A cross section of the resulting SEBT is shown in **Figure 8**.

Figure 9 shows the *I–V* characteristics of an SEBT with a 110-nm base width. The collector current was ideal throughout the current range, but leakage current degraded the base-current characteristics. Two effects could be identified as being responsible for this base-current degradation: First, it was found [37] that the formation of the emitter sidewall spacer was difficult to achieve if the epitaxial layer thickness (and thus the roughness at the poly sidewall) was large, resulting in severe emitter-base leakage. Secondly, cross-sectional TEM studies showed that the transition regions between polysilicon and epitaxial silicon regions contained a high density of stacking faults [38]. Enhanced boron diffusion from the highly doped extrinsic base polysilicon through this defective region beneath the emitter sidewall results in an encroachment of boron into the emitter diffusion, which could be another reason for base-current degradation. It has been shown in [37] that sidewall-spacer formation can be controlled well if the epitaxial layer is thin enough. We believe that dopant encroachment beneath the emitter sidewall can be eliminated if the thickness of the epitaxial layer is further reduced. This will require epitaxy at temperatures below 900°C for lower growth rate and, therefore, improved process control. The SEBT is a logical extension of the conventional double-polysilicon self-aligned method to achieve epitaxial-base integration. It is attractive because it requires only that the base implantation be replaced by selective epitaxial growth in a conventional reduced-pressure reactor. It should be noted, however, that despite the good quality of the epitaxial film, care is needed to ensure proper linkup between the intrinsic and extrinsic bases.

• *Epitaxial growth over a trench capacitor*

Dynamic random access memory (DRAM) technology is rapidly moving toward the use of three-dimensional structures to achieve high density. In the 4Mb DRAM chip generation, use is made of trench storage capacitors to decrease cell size [39]. An epitaxy-over-trench (EOT) process has been devised as a potential means of achieving the combination of cell size and capacitance needed for future DRAMs [40, 41]. Selective epitaxy is used to bury the trench storage capacitor of a cell below single-crystal material, permitting the transfer transistor of the cell to be fabricated above the storage capacitor.

An experimental DRAM cell [41] which makes use of the EOT is shown in **Figure 10**. Clearly, a capability is

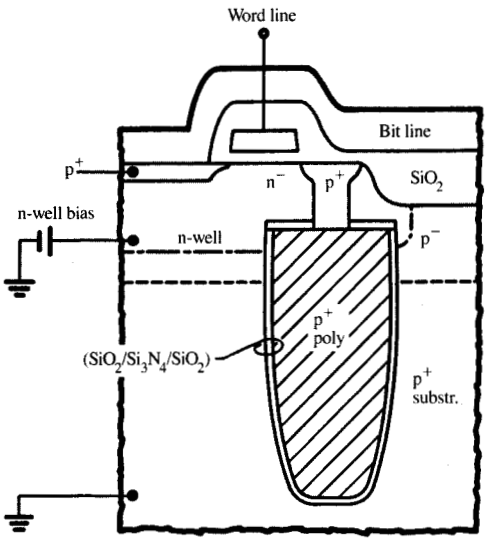


Figure 10

Cross section of experimental buried-trench DRAM cell.

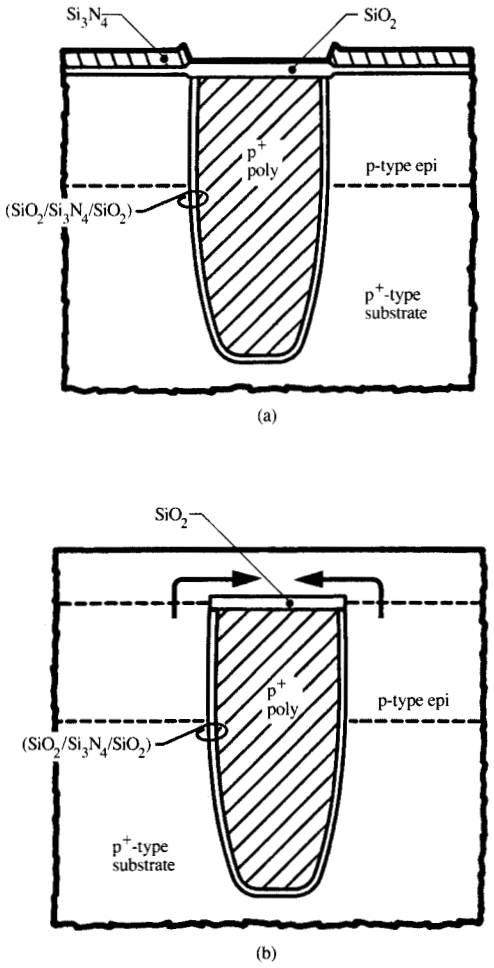


Figure 11

Key steps in epitaxy-over-trench (EOT) process: (a) formation of trench with self-aligned cap; (b) lateral overgrowth of silicon, covering trench capacitor.

required to form high-quality silicon over the trench storage capacitor. In **Figure 11**, the key steps used to fabricate the cell are shown. A Si_3N_4 film is deposited over a thin SiO_2 layer and is patterned to define the storage capacitor trench. This film is an etch stop for removing the polysilicon used to fill the trench. After the polysilicon is etched back, the Si_3N_4 nitride film is used to provide a self-aligned cap oxide above the trench. This structure is shown in part (a). The nitride and pad oxide are then removed, leaving the trench with its cap oxide, surrounded by bare silicon. This large area of silicon surrounding the trench is the seed for the selective epitaxial growth, which is used to deposit silicon laterally over the trench. In time the laterally growing silicon covers the trench, as shown in part (b). Selective epitaxy is achieved by using the $SiCl_4 + H_2$ process. Growth occurs at 900°C at a pressure of 40 torr, following a 950°C H_2 pre-bake for five minutes. The pre-bake and deposition temperatures ensure that device-quality silicon is produced. It is essential that native oxide be removed prior to selective epitaxial growth so that no oxide inclusions are present to nucleate defects during growth. Unlike the SEEW process described above, the EOT process involves the unrestrained growth of silicon over a planar pad of oxide. Because the growth is dominated by {100} planes and the trenches are oriented in ⟨110⟩ directions, growth proceeds from the corners of the trenches, resulting in the formation of a diamond-shaped hole. **Figure 12** is an illustrative plan-view TEM image showing the growth of {100} planes in the corner of a {110} oriented oxide pad. The hole, which is self-aligned to the trench, is rotated at an angle of 45° from the starting trench orientation. Its size can be calculated from the original trench size and the thickness of the epitaxial film. **Figure 13** contains an SEM image of the self-aligned holes remaining after partial trench overgrowth. Note the uniformity of the sizes and shapes of the holes. Next, the self-aligned hole is used to form the via to the trench capacitor by opening the oxide covering the polysilicon-filled trench and carrying out a second epitaxial deposition.

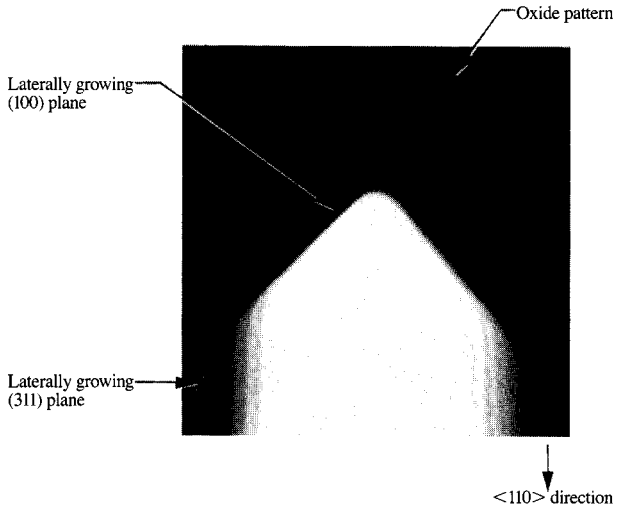


Figure 12

Plan-view TEM image showing laterally growing {100} planes.

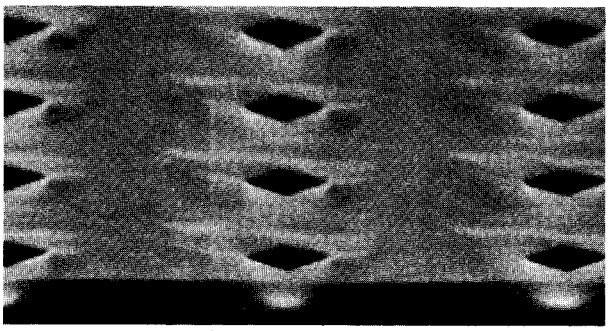


Figure 13

SEM image of self-aligned holes remaining after partial trench overgrowth. Buried oxide over the trenches is visible at the bottom of the image.

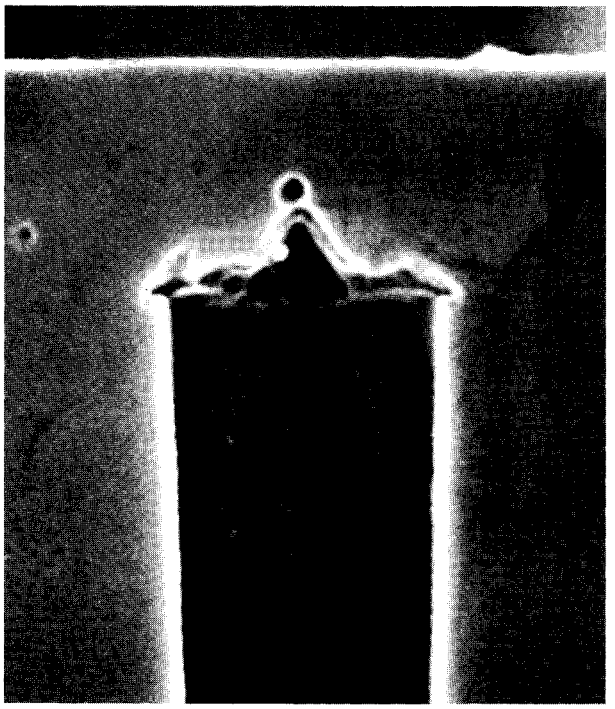


Figure 14

SEM image of cross section of etched sample after two-step epitaxy. Note pyramid-shaped "neck."

Table 1 Charge-carrier lifetimes (in μs) epitaxial silicon grown over unpatterned silicon vs. those in epitaxial silicon grown over oxide pads.

Sample no.	*Unpatterned silicon*	*Oxide pads*
1	135	53
2	90	48
3	81	131
4	73	117
5	71	123

During the second epitaxial deposition, single-crystal silicon grows on the first epitaxial layer and polysilicon nucleates on the exposed trench material, thus forming a self-aligned via or "neck." To complete the cell, an MOS transfer transistor is fabricated in the epitaxial silicon above the trench; contact to the trench storage capacitor is achieved through the neck.

Figure 14 contains an SEM image of a cross section of an etched sample after completion of the epitaxial depositions. The pyramid-shaped neck connection is visible. Note also the absence of defects in the single-crystal material; if present, they would have been decorated by the etchant. TEM analysis confirmed the presence of good-quality silicon. MOS capacitors were used to measure carrier lifetimes in silicon grown over an array of 5000 thin oxide pads that were patterned with the mask used to define the storage trenches. Typical data are presented in **Table 1**. As can be seen, carrier lifetimes over the array of oxide pads were found to be comparable to that of material grown over unpatterned silicon, and were uniformly high. Relatively large diodes were fabricated over a similar array of 5000 storage trenches. Ion implantation was used to produce an n-well, and p^+–n junctions were formed in the well directly over the trenches. Leakage current measurements in diodes formed over areas with and without buried trenches showed no

effect due to the presence of the trenches. In both cases, the leakage current was found to be about 0.2 fA/μm^2.

To examine the applicability of the EOT process to the DRAM technology, cells and associated test sites were designed and fabricated. The *I–V* characteristics obtained for NMOS and PMOS transistors on the test sites are shown in **Figure 15**. The characteristics were equivalent to those of submicron MOS transistors fabricated in a conventional substrate. The apparent electron and hole mobilities measured from long-channel transistors were found to be about 405 and 120 cm^2/V-s, respectively.

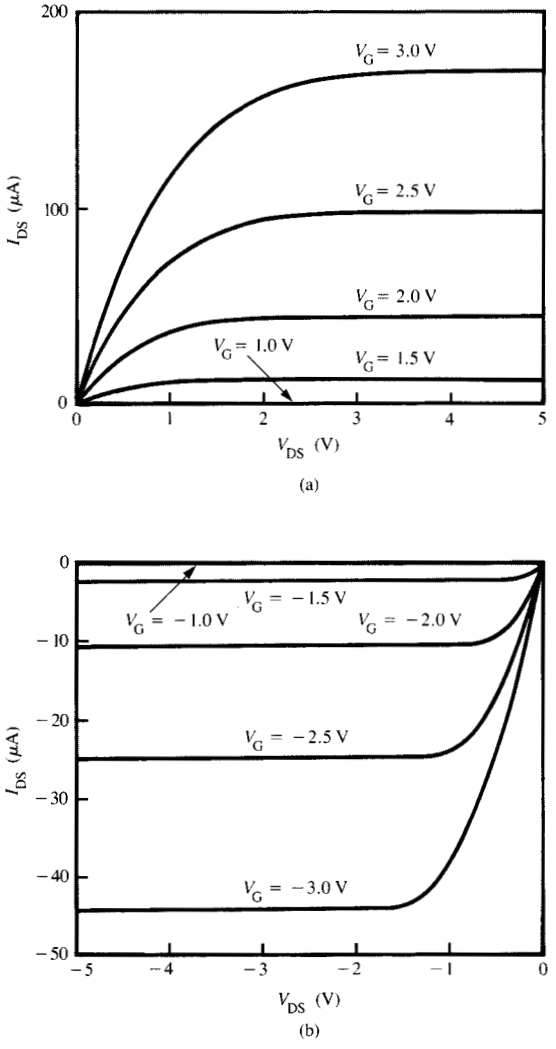


Figure 15

I–V characteristics on DRAM test site: (a) of NMOS transistors; (b) of PMOS transistors.

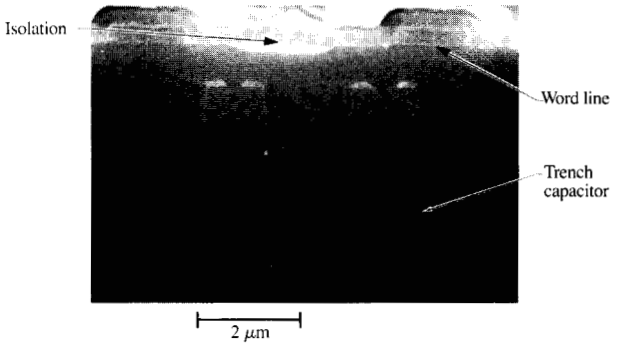


Figure 16

SEM image of cross section of experimental DRAM cell.

Transconductances for the NMOS and PMOS transistors, ranging from 103 mS/mm and 53 mS/mm, respectively, were obtained for effective channel lengths of 1.0 μm, with a drain bias of 3.5 V and a gate bias of 3.0 V above threshold.

Figure 16 shows an SEM image of a cross section of a completed DRAM cell. The cell, which was designed using 0.85-μm ground rules, occupied an area of 7.8 μm^2 (corresponding to less than 10.8 lithographic squares), and was found to be capable of functioning in a write "1"/read "1"/write "0"/read "0" sequence.

Summary

The selective epitaxial growth (SEG) of silicon at lower temperatures than are conventionally used in the epitaxial growth of silicon has made it possible to explore the formation of novel silicon devices and integrated-circuit structures. Although the use of $SiCl_4$ has fallen out of favor for the conventional epitaxial growth of silicon, we have found that it has certain advantages when applied to the SEG of silicon. Because HCl does not have to be added for selectivity, the use of $SiCl_4$ results in a clean and repeatable growth process with very good uniformity.

The following potential applications of the process have been described:

- The use of SEG-grown non-device-quality silicon to form the emitter of a SEEW (selective-epitaxial emitter-window) transistor. Formation of the emitter relies on the correct choice of crystallographic planes such that an opening with vertical sidewalls results from the selective epitaxial growth. This self-aligned opening defines the active device region of the transistor. The emitter opening thus formed permits the use of optical lithography for forming deep submicron devices. It avoids the problems of linkup of the intrinsic and

extrinsic base regions, and reactive-ion-etch damage in the active device region.

- The use of SEG-grown device-quality silicon to form the base of an SEBT (selective-epitaxial-base transistor). Because the silicon is grown only on the base of the transistor, the fabrication of the transistor is simplified. Because of the capability to form a very narrow base by depositing a thin *in situ* doped epitaxial layer of silicon, difficulties in achieving thin-base formation by the conventional ion-implantation approach are avoided. Furthermore, that capability ensures linkup of the intrinsic and extrinsic base regions. The SEBT is the first self-aligned epitaxial-base transistor that has been reported.
- The use of an extension of the SEG process, designated as the EOT (epitaxy-over-trench) process, for depositing device-quality silicon over a trench storage capacitor in a DRAM cell, leading to the formation of a very compact cell. Because of the crystallographic morphology of the epitaxial overgrowth, a self-aligned connection is formed between the buried-trench storage capacitor and the transfer device of the cell.

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References

1. J. O. Borland, *Proceedings of the 10th International Conference on Chemical Vapor Deposition*, PV 87-8, Electrochemical Society, 1987, p. 307.
2. B. D. Joyce and J. P. Baldrey, *Nature* **195,** 485 (1962).
3. D. M. Jackson, *Trans. Met. Soc. AIME* **233,** 596 (1965).
4. D. D. Rathman, D. J. Silversmith, and I. A. Burns, *J. Electrochem. Soc.* **129,** 2303 (1982).
5. L. Jastrzebski, J. F. Corboy, and R. Pagliaro, *J. Electrochem. Soc.* **129,** 2645 (1982).
6. B. J. Ginsberg, M. Arienzo, S. R. Mader, and M. D'Agostino, *Ext. Abst. Electrochem. Soc.* **84-2,** 749 (1984).
7. K. Tanno, N. Endo, H. Kitajima, Y. Kurogi, and H. Tsuya, *Jpn. J. Appl. Phys.* **21,** L564 (1982).
8. J. T. McGinn, L. Jastrzebski, and J. F. Corboy, *J. Electrochem. Soc.* **136,** 398 (1984).
9. J. O. Borland and C. I. Drowley, *Solid State Technol.* **28,** 141 (1985).
10. B. Ginsberg, G. Bronner, and S. Mader, *Ext. Abst. Electrochem. Soc.* **87-2,** 991 (1987).
11. J. Murota, N. Nakamura, M. Kato, N. Mikoshiba, and T. Ohmi, *Appl. Phys. Lett.* **54,** 1007 (1989).
12. T. R. Yew and R. Reif, *J. Appl. Phys.* **65,** 2500 (1989).
13. R. Regolini, D. Bensahel, E. Scheid, and J. Mercier, *Appl. Phys. Lett.* **54,** 658 (1989).
14. M. Berkenblit, T. O. Sedgwick, and C. Wong, *Proceedings of the 10th International Conference on Chemical Vapor Deposition*, PV87-8, Electrochemical Society, 1987, p. 406.
15. Y. S. Yu and A. Witkowski, *J. Electrochem. Soc.* **135,** 2562 (1988).
16. V. J. Silvestri, *Ext. Abst. Electrochem. Soc.* **86-2,** 402 (1986).
17. J. L. Mauer, B. J. Ginsberg, D. A. Danner, and G. P. Li, *Ext. Abst. Electrochem. Soc.* **86-2,** 404 (1986).
18. H. Shibata, S. Samata, M. Saitoh, T. Matsuno, H. Sasaki, Y. Matsunaga, K. Hashimoto, and J. Matsunaga, *Technical Digest, IEEE Symposium on VLSI Technology*, 1987, p. 75.
19. H. Inokawa, T. Kobayashi, and K. Kiuchi, *Extended Abstracts, 18th Conference on Solid State Devices and Materials*, Jpn. Soc. Appl. Phys., Tokyo, 1986, Sec. B-2-2, p. 73.
20. L. Karapiperis, G. Garry, and D. Dieumegard, *Extended Abstracts, 18th Conference on Solid State Devices and Materials*, Jpn. Soc. Appl. Phys., Tokyo, 1986, Sec. A-3-7LN, p. 713.
21. N. Kasai, N. Endo, and A. Ishitani, *Technical Digest, IEEE International Electron Devices Meeting*, 1988, p. 242.
22. N. Endo, K. Tanno, A. Ishitani, Y. Kurogi, and H. Tsuya, *Technical Digest, IEEE International Electron Devices Meeting*, 1982, p. 241.
23. L. Jastrzebski, A. Ipri, J. F. Corboy, and R. Metzel, *Technical Digest, IEEE Symposium on VLSI Technology*, 1983, p. 50.
24. J. N. Burghartz, J. D. Warnock, S. R. Mader, and B. J. Ginsberg, *Electron Lett.* **25,** 1337 (1989).
25. D. Harame, B. Ginsberg, M. Arienzo, S. Mader, and M. D'Agostino, *Solid State Electron.* **30,** 907 (1987).
26. C. I. Drowley, G. A. Reid, and R. Hull, *Appl. Phys. Lett.* **52,** 546 (1988).
27. L. Jastrzebski, J. F. Corboy, and R. Soydan, *J. Electrochem. Soc.* **136,** 3506 (1989).
28. R. Pagliaro, J. F. Corboy, L. Jastrzebski, and R. Soydan, *J. Electrochem. Soc.* **134,** 1235 (1987).
29. N. Kasai, M. Kimura, N. Endo, A. Ishitani, and H. Kitajima, *Jpn. J. Appl. Phys.* **25,** 671 (1987).
30. F. W. Smith and G. Ghidini, *J. Electrochem. Soc.* **129,** 1300 (1982).
31. Y. Tamaki, F. Murai, K. Sagara, and A. Anzai, *Technical Digest, IEEE Symposium on VLSI Technology*, 1987, p. 31.
32. J. N. Burghartz, B. J. Ginsberg, and S. R. Mader, *Technical Digest, IEEE Symposium on VLSI Technology*, 1989, p. 57.
33. J. N. Burghartz, S. R. Mader, B. S. Meyerson, B. J. Ginsberg, J. N. Stork, C. S. Stanis, and Y. C. Sun, *Technical Digest, IEEE International Electron Devices Meeting*, 1989, p. 229.
34. J. N. Burghartz, S. R. Mader, B. J. Ginsberg, B. S. Meyerson, J. M. C. Stork, C. L. Stanis, Y.-C. Sun, and M. R. Polcari, *IEEE Trans. Electron Devices*, in press (1991).
35. A. E. Michel, M. Numan, and W. K. Chu, *Appl. Phys. Lett.* **53,** 851 (1988).
36. A. Ishitani, H. Kitajima, K. Tanno, H. Tsuya, N. Endo, N. Kasai, and Y. Kurogi, *Microelectron. Eng.* **4,** 3 (1986).
37. J. N. Burghartz, B. J. Ginsberg, S. R. Mader, T. C. Chen, and D. L. Harame, *Electron Device Lett.* **29,** 259 (1988).
38. J. N. Burghartz, B. J. Ginsberg, S. R. Mader, T. C. Chen, and D. L. Harame, *J. Phys. C4* **9,** 367 (1988).
39. H. Sunami, *Technical Digest, IEEE International Electron Devices Meeting*, 1985, p. 694.
40. G. B. Bronner, N. C. C. Lu, T. V. Rajeevakumar, B. Ginsberg, and B. Machesney, *Technical Digest, IEEE Symposium on VLSI Technology*, 1988, p. 21.
41. N. C. C. Lu, T. V. Rajeevakumar, G. B. Bronner, B. Ginsberg, B. J. Machesney, and E. J. Sporgis, *Technical Digest, IEEE International Electron Devices Meeting*, 1988, p. 588.

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