Heterojunction FETs in III–V compounds

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We review work on heterojunction FETs (HFETs) fabricated from III–V compounds, with emphasis on the unique properties of such devices and their applicability to high-speed logic circuits. After discussing their general properties, including their uniquely high carrier mobility and fast switching speed, we discuss HFETs investigated at the IBM Thomas J. Watson Research Center, i.e., the semiconductor–insulator–semiconductor FET (SISFET) and quantum-well metal–insulator–semiconductor FET (QW-MISFET)—and their possible circuit applications. Finally, the opportunities for achieving a circuit performance level beyond that offered by the GaAs–(Al,Ga)As materials system are explored.

Introduction

When compared with silicon, which forms the basis of all current large-scale integrated circuits, direct-gap III–V compound semiconductors have superior electron transport properties. The electron mobility in these materials is higher because of the smaller effective mass of their conduction electrons, and lower associated scattering rates. The scattering rates are also reduced because low-field transport occurs within a single valley. These superior transport properties result in higher-speed electronic devices. In fact, the highest-speed semiconductor devices, useful especially for microwave amplifiers, are fabricated using semiconductors from the III–V group, i.e., compounds of Ga, Al, or In with As, P, or Sb. The GaAs MESFET (metal semiconductor field-effect transistor) as discussed by Jackson et al. [1] is the most widely used III–V transistor and now dominates the microwave arena. While permitting much higher frequency performance than silicon, the MESFET configuration does not take full advantage of the higher mobilities offered by GaAs and the other III–V compounds. Electron transport in a MESFET occurs in a doped channel of GaAs, and the dopant ions themselves reduce the mobility of the electrons. This effect is exacerbated at smaller gate lengths, where more heavily doped channels must be used to comply with requirements of vertical scaling of the channel. A further disadvantage of the MESFET, especially for digital applications, is that the forward gate voltage is restricted to less than 0.7 V because of the turn-on of its forward-biased-gate Schottky barrier.

This paper pertains to III–V HFETs in which use is made of layered structures of different III–V materials instead of the doped GaAs layer of the MESFET. The layers are all epitaxial and are grown by a crystal-growth technique such as molecular beam epitaxy (MBE). The GaAs/$Al_xGa_{1-x}As$ materials system is the most widely used for this purpose because of the availability of high-quality GaAs wafers (as used for MESFETs) and because the lattice constant of $Al_xGa_{1-x}As$ is almost the same as for GaAs for all values of the AlAs mole fraction x. At

the boundary between two adjacent layers, which generally have different bandgaps, discontinuities exist between the conduction bands (ΔE_C) and valence bands (ΔE_V). These band discontinuities are of considerable importance in HFET design, since they act as barriers to spatially confine electrons and holes. A band diagram of such a heterojunction is shown in **Figure 1(a)** for $Al_xGa_{1-x}As$ sandwiched between GaAs layers.

In the modulation doping technique, first demonstrated by Dingle et al. [2] in 1978, the larger-bandgap material is doped and electrons spill over from the wide- to the narrow-bandgap material and form an electron channel, as shown in **Figure 1(b)** for n-type doping. The momentum of the electrons in the channel perpendicular to the interface is quantized, and the electrons have freedom of motion in the other two dimensions, forming a two-dimensional electron gas (2DEG). Because the donors are thus separated from the electrons, their scattering power is much reduced, and consequently the electrons in a 2DEG generally have a much higher mobility than those in the doped-channel MESFET. At room temperature the difference in electron mobility is roughly a factor of two (8000 cm^2/V-s vs. 4000 cm^2/V-s). The difference is even larger at lower temperatures, since the next most important scattering mechanism, that due to polar optical phonons, is greatly reduced. Mobilities for a 2DEG of $\simeq 2 \times 10^5$ cm^2/V-s can be obtained at liquid nitrogen temperature, and mobilities greater than 1×10^7 cm^2/V-s at liquid helium temperature. Not only the mobility, but also the peak velocity in the velocity vs. field curve for bulk GaAs, is affected by the removal of the dopants, although here the effect is much more modest, <2× at 77 K [3]. For small FETs (<1-μm gate length), Monte Carlo simulations [4] show large peak velocities in FETs, limited by the maximum group velocity in GaAs rather than by details of doping, geometry, and temperature; nevertheless, the velocity is higher over a larger portion of the channel in a FET with a high channel mobility.

Using modulation doping, FETs were fabricated with a 2DEG channel, first in Japan [5] and shortly afterward in the USA and France as well. These FETs exhibited record-breaking speeds, which were attributed to the higher mobility of their carriers. Thus, one of the major limitations of MESFETs had been overcome, namely the degradation of their carrier mobility with doping. Different acronyms were given to these FETs by the different groups, each reflecting a different attribute of the basic structure. Thus we have the HEMT (high electron mobility transistor) from Fujitsu, the MODFET (modulation doped FET) from the University of Illinois, the SDHT (selectively doped heterojunction transistor) from AT&T, and the TEGFET (two-dimensional electron gas FET) from Thomson–CSF. In this paper, we use the MODFET acronym to designate such a device. For more details on MODFETs, including their design and performance, see Solomon and Morkoç [6], Drummond et al. [7], Abe et al. [8], and Sugeta et al. [9]. **Figure 2(a)** shows a band diagram for a typical MODFET under a positive gate bias. The possible use of different AlAs mole fraction and doping combinations results in a considerable design freedom, and, accordingly, many variations on the basic structure of Figure 2(a) have been tested [10, 11]. For instance, using a technique called "delta doping," the uniform doping in the $Al_xGa_{1-x}As$ has been replaced by a single plane of dopants $\simeq$5 nm from the 2DEG channel, permitting a higher concentration of electrons in the 2DEG before spill-over of carriers into the $Al_xGa_{1-x}As$.

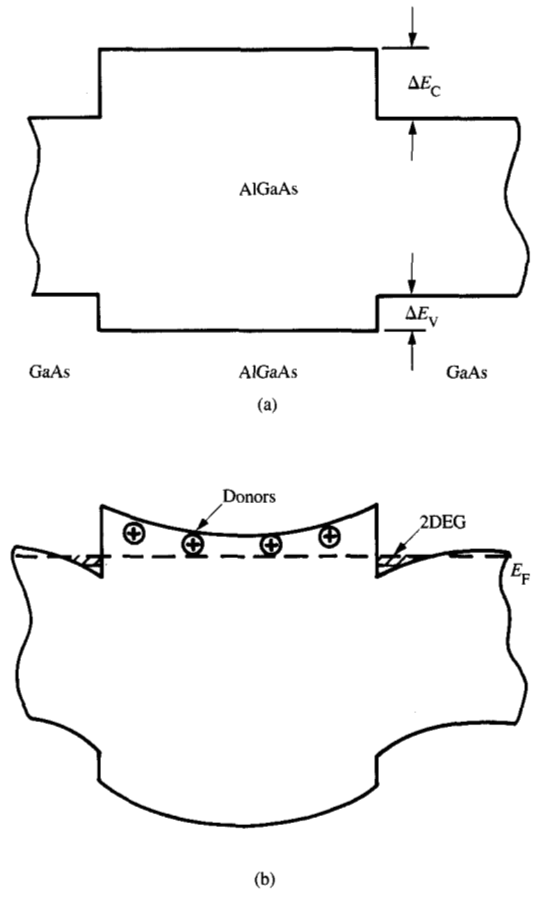

Figure 1

Band diagram for an $Al_xGa_{1-x}As$–GaAs heterojunction: (a) for an undoped structure, showing conduction and valence-band discontinuities; (b) for a modulation-doped structure, showing 2DEG channels.

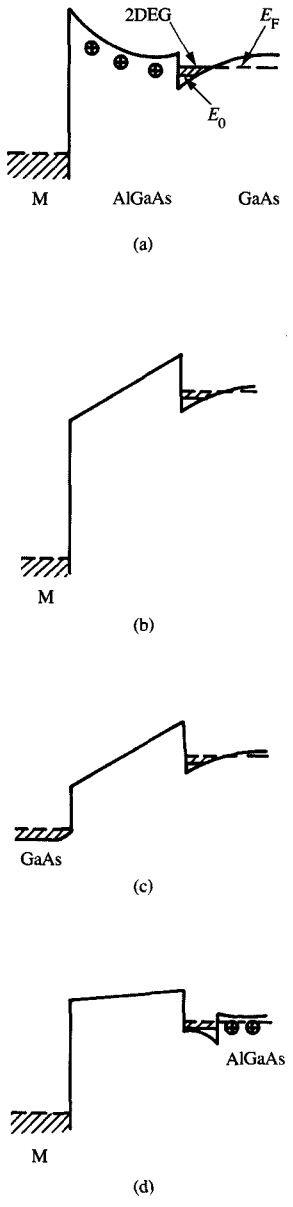

Figure 2

Band diagrams for different types of HFETs: (a) for a MODFET; (b) for a MISFET in which the $Al_xGa_{1-x}As$ is undoped and the 2DEG channel is induced by a voltage on the gate; (c) for a SISFET in which the metal gate is replaced with n^+ GaAs; (d) for a quantum-well MISFET in which doping in the bottom $Al_xGa_{1-x}As$ layer is used to reduce the threshold voltage.

The main drawback of modulation doping is the problem of the DX center, a deep trap associated with every donor in $Al_xGa_{1-x}As$ [12]. This trapping causes bias-induced instabilities in the MODFET characteristics, and threshold voltage shifts, especially at low temperatures [13]. The trapping can be reduced to acceptable levels by using $x \lesssim 0.2$ with the penalty of reduced electron confinement. Other solutions are discussed in the following sections.

On examination of the band diagram for the MODFET shown in Figure 2(a), it may be appreciated that the 2DEG channel is no different qualitatively from the inversion channel of a conventional Si MOSFET, the electrons terminating electric field lines induced in the $Al_xGa_{1-x}As$. It is irrelevant, from the device point of view, whether this field is induced by doping the AlGaAs or, as shown in **Figure 2(b)** for a MISFET (metal insulator semiconductor), merely created by a gate bias. The metal gate of the MISFET may be replaced by an n^+ GaAs gate to make a SISFET [**Figure 2(c)**]. In the MODFET, the channel field is the sum of the field due to the donors and that due to the gate. In the SISFET and MISFET, the insulator is undoped AlGaAs, and the field is due only to the gate. In the quantum-well MISFET [**Figure 2(d)**], the $Al_xGa_{1-x}As$ behind the channel is modulation-doped, so that charge is introduced into the channel from both interfaces.

Another advantage of HFETs is their higher gate-current turn-on voltage compared with that for MESFETs. For one thing, Schottky barrier heights at metallic contacts to $Al_xGa_{1-x}As$ are larger than those to GaAs; for another, the 2DEG is confined to the vicinity of the AlGaAs barrier, and this barrier continues to exist even when a forward voltage is applied which is larger than the Schottky barrier height. This barrier, which is designated as the conduction-band discontinuity ΔE_C for electrons and valence-band discontinuity ΔE_V for holes, is a very important parameter in the design of HFETs. Estimates of these parameters from the band lineup of GaAs and $Al_xGa_{1-x}As$, along with experimental barrier heights obtained from measurements of thermionic emission currents, are given in **Figure 3**. Because $Al_xGa_{1-x}As$ changes from a direct to an indirect band lineup at $x = 0.4$ as shown in the figure, ΔE_C has a maximum in this range of x. In contrast to this, the variation of ΔE_V with x is linear [14] and has its maximum value of 0.55 eV at $x = 1$. It was found [15] for electrons that the magnitude of the effective Richardson's constant (scaling factor for the current) is reduced in the indirect regime; this partially offsets the reduction in barrier height in that regime.

Until now we have considered n-channel devices only. The same principles apply to p-channel devices, for which much higher hole mobilities are achieved in a two-dimensional hole gas (2DHG) than in a doped channel, especially at low temperatures. Störmer et al. [16] have measured mobilities in p-modulation-doped layers of 400 $cm^2/V\text{-}s$ at 300 K and 6000 $cm^2/V\text{-}s$ at 77 K. This is to

be contrasted to the silicon CMOS [17] case, where interface roughness scattering limits the hole mobility at high gate fields $>1 \times 10^5$ V/cm (typical of FETs) to <150 and 600 cm^2/V-s at 300 K and 77 K, respectively. As we discuss next, the mobility improvement at low temperatures is much more important in p- than in n-channel devices, because circuit speed is very sensitive to mobility in this mobility range. The improvement in Schottky barrier height for the p-HFET is also very significant, since the p-Schottky of the MESFET is too small for reliable circuit operation. As seen in Figure 3, the maximum ΔE_V occurs at $x = 1$ for holes in $Al_xGa_{1-x}As$ and, hence, even higher mole fractions are desirable for p-HFETs than for n-HFETs. Investigations of p-HFETs have been pioneered both at IBM [18] and at AT&T [19, 20].

We see from basic principles that the HFET is faster than the MESFET, especially at low temperatures, and can work over a larger voltage range. The high-speed capability was apparent from the early MODFET work of Fujitsu. **Figure 4** shows the trend in ring oscillator delays with gate length for MESFETs at 300 K and for MODFETs at 300 K and 77 K. Data for this figure were taken from reports published over the years 1981 to 1989 [7, 21–32]. In most cases the power was in the 1–5-mW range, except for the 0.1-μm-gate-length MESFET (for brevity, 0.1-μm MESFET), for which it was 31 mW. Proportionality trend lines were fitted to the data passing through the geometric mean of the respective data points. There is a large scatter in the data because of varying and uncontrolled design factors; nevertheless, there is a clear trend showing an approximately 50% advantage of MODFETs over MESFETs at 300 K, with another factor of about 2 accruing at 77 K. The present speed record for HFETs is 5.8 ps at 1.8 mW for a 0.35-μm-gate-length ring oscillator from AT&T [21] at 77 K; for MESFETs [32] it is 5.9 ps at 30 mW for a 0.1-μm gate length and at 300 K. For comparison, 0.1-μm Si NMOS [33] devices operating at 77 K have achieved delays of 14 ps.

The rest of this paper consists of four major sections. In the first we further discuss the factors which affect the performance of HFETs and relate this to the field of applications for those devices. The next two sections deal with HFET device technologies under active investigation at the IBM Thomas J. Watson Research Center, the first being an n-channel SISFET enhance-deplete technology, and the next a complementary HFET technology based on quantum-well MISFET devices. Finally, we discuss the use of III–V materials systems other than the (Al,Ga)As system and their performance advantages.

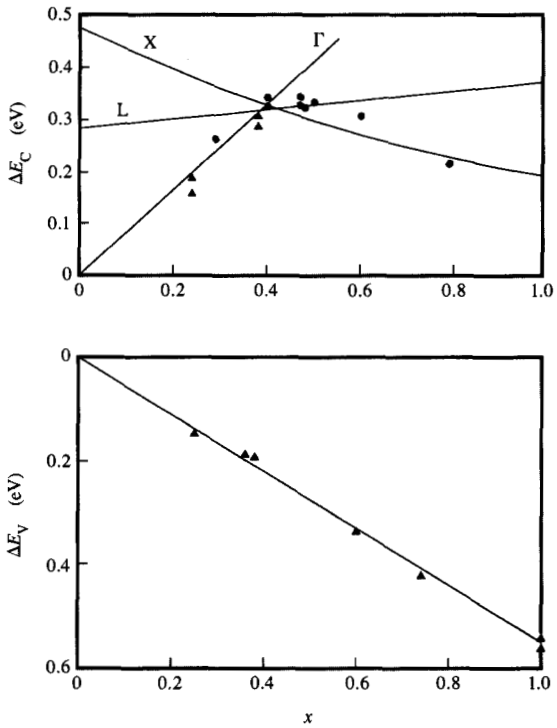

Figure 3

Conduction band and valence band discontinuities for the GaAs/$Al_xGa_{1-x}As$ system. After Solomon et al. [15] (circles), and Batey and Wright [14] (triangles).

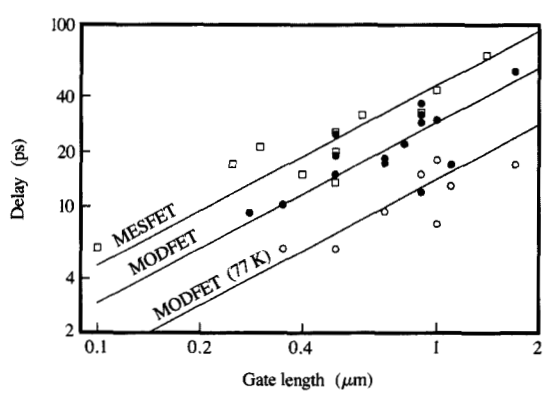

Figure 4

Delay vs. gate length for MESFET (squares) ring oscillators measured at 300 K, and HFET ring oscillators measured at 300 K (solid circles) and at 77 K (open circles). Data compiled from [7] and [21–32].

HFET performance and applications

For a detailed appreciation of carrier transport through the channel of a FET, the reader is referred to the paper

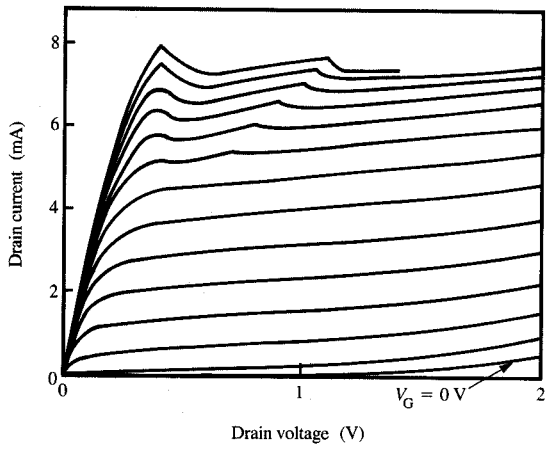

Figure 5

Drain characteristics of an experimental ohmic self-aligned SISFET at 77 K having a 1.7-μm gate length and 20-μm gate width. Gate voltage steps are 0.1 V. The characteristics are not corrected for probe resistance (~10 Ω). The negative resistance regions are attributed to hot-electron current and the discontinuities to RF oscillations.

by Laux, Fischetti, and Frank [4]. The approach we present below is phenomenological and emphasizes how material transport parameters, FET geometry, and choice of circuit affect performance in high-speed digital applications.

Extremely high mobilities can be obtained in n-channel HFETs at low temperatures. This is not a direct measure of the high-speed performance of the HFET. A measure of the fastest switching speed a FET is capable of is given by the transit time τ_t of electrons (or holes) from source to drain, which can be expressed as $\tau_t = L/\bar{v}$, where L is the channel length and $\bar{v}$ is the "average" velocity of the electrons (or holes) along the channel. For sufficiently long gate-length devices, in saturation, $\bar{v}$ is proportional to the mobility, μ, times the average field in the non-pinched-off part of the channel $[(V_G - V_T)/L]$. This implies a decrease in τ_t with $1/\mu L^2$. As seen in Figure 4, the experimental ring oscillator results decrease much less strongly, more like $1/L$. This is due to 1) velocity saturation, which would give a $1/L$ dependence, and 2) the effects of parasitic capacitances. First, the extremely high mobilities possible in 2DEG channels are seen only at low electric fields (<1 kV/cm) and at channel lengths much longer than the electron mean free path (≃0.5 μm). Thus, the improved mobility contributes less and less to improving device-switching speeds at small gate lengths. Monte Carlo simulations[1] suggest that the main contribution of the higher mobility to FET performance is to increase the velocity near the source-end where it is most effective in determining the total current [34]. Use is usually made of the ratio of transconductance to gate capacitance as a measure of effective carrier velocity. These numbers range from about $1.1–1.4 \times 10^7$ cm/s for MESFETs and MODFETs, respectively, at room temperature, to about 2.2×10^7 for SISFETs at 77 K. When used in device models, these velocities suggest that the performance of a switching circuit, employing 0.5-μm devices and with a 1-V power supply, becomes independent of mobility when the mobility is greater than $\simeq 1 \times 10^4$ cm^2/V-s [35]. Second, as we see below, failure to scale vertical with horizontal dimensions leads to an increasing dominance of the device parasitic capacitance in determining the delay.

Another figure of merit for the HFET is its transconductance per unit width (g_{me}). For the digital HFET the large-signal transconductance G_m (g_{me} averaged over the logic swing) is the relevant quantity [34]. This is a direct measure of the ability of the FET to drive an external capacitive load C_L, since a major component of the delay on a heavily loaded node is $C_L/G_m W$, and the device width W is restricted by space requirements. The intrinsic transconductance can be approximated by $g_{mi} = \bar{v}\epsilon_1/(d + \Delta d)$, where Δd is the equivalent thickness of the 2DEG (≃ 5 nm [34]), which must be added to the thickness of the $Al_xGa_{1-x}As$. The extrinsic transconductance g_{me} is related to the intrinsic transconductance by $g_{me} = g_{mi}/(1 + g_{mi}R_s)$, where R_s is the source resistance. A typical 0.5-μm MODFET with $d = 30$ nm would thus have a g_{me} of ≃300 mS/mm at 300 K and 400 mS/mm at 77 K.

The formulae developed above (which are well known) apply to the parasitic capacitances as well. The fringing capacitances C_p at the edges of the gate depend mainly on the gate width and are typically 0.1–0.2 fF/μm. These cause an extra component of delay $\propto C_p/g_{me}$ which is independent of gate width and can only be reduced by increasing g_{me} by proper scaling of the vertical dimension and reducing R_s.

In addition to the benefits of increased magnitude of g_{me}, a low overall resistance from source to drain is very important when driving low-impedance loads. The intrinsic HFET at 77 K has a low resistance because of its high channel mobility. This is apparent in **Figure 5**, which shows the characteristics of an experimental ohmic self-aligned SISFET device that is 20 μm in width and has a source–drain resistance (including that of the probes) of only 32 Ω. Although the fabrication process for this device is not practical for VLSI, this demonstrates that HFETs of small width should have a resistance low enough to drive transmission lines which typically have impedances of about 50 Ω.

[1] D. J. Frank, IBM Research Division, Thomas J. Watson Research Center, Yorktown Heights, NY, unpublished work.

For FETs with very short gate lengths the transconductance increases, suggesting an increase in $\bar{v}$. Recently Chao et al. [36] have reported a significantly enhanced transconductance of up to 920 mS/mm for their 80-nm "delta-doped" pseudomorphic MODFET compared to about 500 mS/mm for a 0.25-μm device. They interpret this as being due to velocity overshoot, although some caution should be exercised, since devices of different gate lengths also had different $Al_xGa_{1-x}As$ thicknesses ($\simeq$25 nm vs. 32 nm) [37].

Power and power–delay product are important considerations for VLSI logic and are strongly influenced by the choice of circuit. In this paper we consider three types of circuits: DCFL (direct-coupled FET logic), SBL (super-buffer logic) and C-HFET (complementary-heterostructure FET) logic. For these circuits the power P can be approximated by

$$P = CV^2\left(\frac{\gamma}{2\tau_D} + f\right), \tag{1}$$

where f is the switching frequency, τ_D the gate delay, and γ a parameter which depends on the circuit type. The first component of Equation (1) is the static power and the second the dynamic power. An extra term, neglected in Equation (1), but which should be small, is the power dissipation caused when both push-pull transistors are on simultaneously. For a DCFL circuit, a static circuit, $\gamma \simeq 1$; for an SBL circuit, a partially dynamic push-pull-type circuit, γ can be $\ll 1$, and for a C-HFET circuit (ignoring gate leakage), $\gamma \simeq 0$. For a DCFL circuit, $f\tau_D < 1$, so that for such a circuit the power dissipation per circuit is much larger than for a C-HFET circuit, even at the highest switching frequencies. The higher n-type mobilities permit DCFL and SBL circuits to operate at high speeds at considerably lower voltages than C-HFET circuits, thus reducing the power penalty. Indeed, for SBL circuits, a regime can be found at very high switching rates (but not typical of most computer applications) where such circuits consume less power than their C-HFET counterparts.

Because of the many factors involved, especially the CV^2 product, quoting power–delay products is not very meaningful unless strictly qualified. Unloaded (low-C) HFET ring oscillators operating at low voltages ($\simeq$0.5 V) can achieve power–delay products of $<$1 fJ.

The chief proponents of the HFET technology for digital logic are Fujitsu, AT&T, and Hewlett-Packard. Fujitsu [38] has reported on a 4K gate array using 0.5-μm MODFETs having a basic delay of 40 ps and a loaded delay (fan-out of 3 and typical wiring length) of 110 ps. A 16 × 16 parallel multiplier was implemented with a record-breaking multiplication time of 4.1 ns. Comparing the delay numbers with those in Figure 4, we see the effect of realistic design for adequate noise margin, and the effect of loading. A 4K static RAM [39] was also implemented with this technology and an access time of 500 ps was achieved.

While able to operate well at room temperature, as shown above, the HFETs are really at their best at low (liquid nitrogen) temperatures. This is so both because of higher carrier mobilities and reduced leakage currents at such temperatures. Silicon CMOS circuits also benefit from improved mobilities at low temperature; investigations of low-temperature CMOS circuits have been carried out at IBM for several years [40]. In addition, the use of a low-temperature environment may bring important benefits to a high-speed computer from the wiring and packaging points of view [41]. Wire resistance is greatly reduced, and failure mechanisms such as electromigration should be of less concern.

Temperature plays a rather different role, whether we are considering the SISFET or the C-HFET. For the SISFET, the improvement in speed is not as important as the improvement in leakage and the ability to function at low voltages which result in low power–delay products at low temperatures. For the C-HFET, the improvement in leakage and transport, especially hole transport, results in much higher circuit speeds.

GaAs gate FET (SISFET)

• *Background*

The GaAs gate FET (SISFET) was conceived independently by Rosenberg [42] and Solomon et al. [43], all at IBM at the time. Its first realization was in 1984, almost simultaneously by the investigators at IBM and at the Electrotechnical Laboratory, Japan [44].

In the SISFET, the metal gate and Schottky barrier of the MODFET (see Figure 2) are replaced by a GaAs gate and heterojunction barrier. A comparison of the band diagrams for the two devices is shown in Figure 2. Note how the GaAs gate band diagram resembles that of a Si MOSFET with the $Al_xGa_{1-x}As$ replacing SiO_2, except that the barrier height for the $Al_xGa_{1-x}As$ is about an order of magnitude smaller; the polysilicon and amorphous SiO_2 of the MOSFET have been replaced by single-crystal epitaxial $Al_xGa_{1-x}As$ and n^+ GaAs. Use of an all-single-crystal structure of the GaAs gate FET, fabricated in the high-vacuum MBE environment, avoids potential problems due to uncontrolled metal–semiconductor and polysilicon–SiO_2 interfaces, which hamper the MOSFET and the MODFET. The fact that the critical $Al_xGa_{1-x}As$ layer is buried under the GaAs gate endows the structure with excellent thermal stability under high-temperature processing.

The symmetry of the GaAs gate-band diagram implies that the threshold voltage V_T of this device is near zero and does not depend critically on the $Al_xGa_{1-x}As$ mole

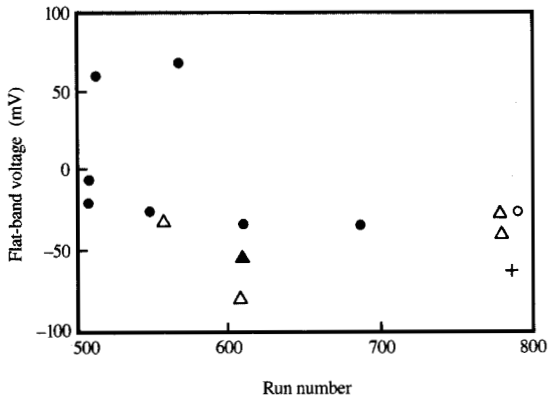

Figure 6

Run-to-run variation of the flat-band voltage for SIS (n^+GaAs–i$Al_xGa_{1-x}As$–n^-GaAs) capacitors. The capacitors ranged in thickness from 30–50 nm and the AlAs mole fractions were 0.3 (open circle), 0.4 (solid circles), 0.5 (open triangles), 0.6 (solid triangle), and 0.8 (plus sign). The run number refers to the cumulative number of runs in a multi-purpose MBE system.

fraction or thickness. The threshold voltage may be approximated by the following equation [43]:

$$V_T = \phi_1 - \phi_2 - eNd^2/2\varepsilon_1 + F_B d\varepsilon_S/\varepsilon_1, \quad (2)$$

where ϕ_1 and ϕ_2 are the barrier heights at the two interfaces, as measured from the Fermi levels when biased at threshold, N and d are the doping and thickness of the barrier, respectively, and $\varepsilon_S/\varepsilon_1$ is the ratio of the dielectric constant in the semiconductor (GaAs) to that in the insulator ($Al_xGa_{1-x}As$).

This equation has an extra term compared to Equation (1) of [43] to account for the effect of a back-field F_B originating in the substrate. It has been verified by repeated experiments on GaAs gate capacitors on n-type substrates. The run-to-run variation of the flat-band voltage of capacitors grown at different times is shown in **Figure 6**. The theoretical flat-band voltage is negative in this case because of the larger work function of the channel region at flat band due to the lighter doping there. Note that, in agreement with Equation (1), the flat-band voltage does not depend on the AlAs mole fraction. By using epitaxially grown semiconductors with a larger work function in the gate, such as Ge [45] or (In,Ga)As, the threshold voltage can be shifted to a suitable positive value for normally-off logic (≃0.1 V). Alternatively V_T can be shifted by p-doping the $Al_xGa_{1-x}As$. Depletion-mode devices can be made by selective n-type ion implantation [46]. The sensitivity to the doping is proportional to the shift from the canonical position ($\phi_1 - \phi_2 + F_B d\varepsilon_S/\varepsilon_1$) according to

$$\Delta V_T = (V_T - \phi_1 + \phi_2 + F_B d\varepsilon_S/\varepsilon_1)\frac{\Delta N}{N}, \quad (3)$$

so that there is only a small sensitivity to doping for low-voltage logic circuits (<1 V), which requires V_T to be less than about 0.2 times the logic swing. It should be emphasized that Equations (2) and (3) address only part of the V_T control problem. There remain short-channel-induced variations in V_T (controllable by proper vertical scaling), as well as those caused by uncontrolled charge in the substrate. For our ion-implanted depletion-mode FET (see next section), a larger shift from canonical position (≃0.4 V) is required, and there is additional sensitivity to epitaxial layer thickness because the tail of the implantation is used.

For the n-SISFET there is no Si doping in the $Al_xGa_{1-x}As$ beneath the gate, so that the problem of DX-center-related threshold shifts does not arise. While some bias-induced change in source–drain resistance can still occur at low temperatures due to DX centers in the Si-implanted $Al_xGa_{1-x}As$ regions outside the gate, these effects are much smaller than those in early MODFETs. The AlAs mole fraction can therefore be much larger than in the MODFET, and is chosen to be 50% to minimize leakage. The larger value of x also leads to an improvement in electron confinement.

The SISFET structure introduces a new degree of freedom into the art of FET design, since the entire structure is a single crystal, and the parameters of all of the layers may be changed at will. One such concept is the saturable-charge FET (SATFET) [47], in which the n-type gate is nonuniformly doped in a heavy–light–heavy configuration. The heavily doped layer nearest the channel is depleted as the 2DEG concentration in the channel is increased. Beyond a critical 2DEG concentration (gate voltage), the depletion layer spreads into the lightly doped layer. The charge in the 2DEG saturates, and with it the gate leakage current; the gate capacitance decreases. Although such a design does not increase the maximum current drive of the device, it allows the gate voltage to swing over a wide voltage range without affecting the low-voltage performance of the FET.

• *SISFET fabrication*

Cross sections of the SISFET are shown in **Figure 7**. The fabrication sequence for the device is as described in [48, 49]. Apart from the MBE growth step and the selective RIE of the top GaAs layer outside the gate, the sequence is very similar to that used for an ion-implanted self-aligned MESFET [1] and a conventional polysilicon gate MOSFET.

The layers grown by MBE (in order of the growth sequence) consist of a 0.6-μm lightly doped buffer layer of GaAs, with a 1×10^{11}-cm^{-2} beryllium-doped central p-layer, followed by a 30-nm $Al_{0.5}Ga_{0.5}As$ layer with a 4×10^{11}-cm^{-2} central p-layer. The gate consists of a 2-nm GaAs spacer followed by $\simeq$100 nm of 2×10^{18}-cm^{-3} n^+ GaAs and by contact layers consisting of 20 nm 6×10^{18}-cm^{-3} n^+ GaAs and 20 nm graded (Ga,In)As, with an additional 20 nm of InAs on the surface. Note in the above the use of the p-layer in the buffer to reduce parasitic electron flow in that layer, the use of the p-layer in the $Al_{0.5}Ga_{0.5}As$ to shift the threshold voltage about 0.1 V positive, and the use of the graded-bandgap (In,Ga)As contact to the gate [50].

The process sequence is as follows. First, silicon is implanted through the (In,Ga)As and GaAs gate layers and the $Al_xGa_{1-x}As$ layer into the channel to form the depletion-mode implantation as practiced by Baratte et al. in [49]. Next, $\simeq$150 nm of refractory metal such as WSi_x is deposited to form the gate contact. The metal is then reactive-ion etched to the InAs, which acts as an etch stop. The In-rich layers are chemically etched, followed by RIE of GaAs, which stops at the $Al_xGa_{1-x}As$ layer, using a method introduced by Fujitsu [51] and further developed at IBM by Knoedler and Kuech [52].

The source/drain regions are now ion-implanted and self-aligned to the gate stack. The ion implantation is angled to minimize channeling, yet is parallel to the gate to maintain symmetry with respect to source and drain. Silicon nitride sidewalls are then formed to protect the InAs contacts (following Tiwari et al. [53]), and the devices are then subjected to rapid thermal annealing at 900°C in an arsine atmosphere, as described by Jackson, DeGelormo, and Pepper [54]. A conventional GaAs process sequence can then be used to complete fabrication of an associated circuit, typically including Au–Ge alloyed contacts, CVD SiO_2 dielectric, and Ti–Pt–Au interconnections, as evidenced in the scanning electron micrograph in Figure 7.

While this process is satisfactory for our experimental circuits, the D-FET load device is unduly sensitive to the epitaxial-layer thickness control. Simulations show that the sensitivity to thickness, for a 100-keV $^{29}Si^+$ implant, is 150 meV for a 10-nm change in total thickness of the top layers. Using a deeper implantation alleviates this problem, but has the undesirable effect of making the characteristics of the D-FET more resistor-like and more sensitive to substrate doping. Work is in progress to develop a more suitable load device.

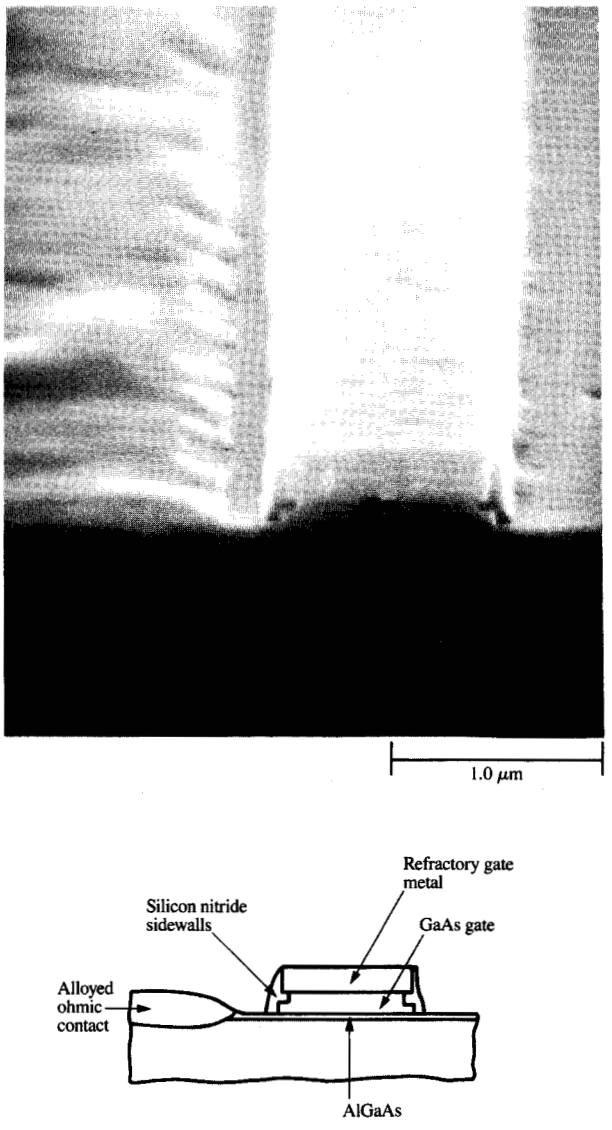

Figure 7

Cross-section views (SEM and schematic) of completed SISFET structure.

• *dc characteristics of the SISFET*

At 77 K SISFETs typically exhibit dc characteristics of the type shown in **Figure 8**. The transconductance vs. gate voltage curves, at 77 K and 300 K, are shown in **Figure 9**. Note how much more rapidly the transconductance turns on at the lower temperature. The sharper turn-on in the knee region is due to the well-known exp $[q(V_G - V_T)/nkT]$ dependence in the subthreshold region (the factor n is typically 1.2–1.5 for most FETs). The higher slope in the linear region is due to the higher channel mobility. The benefit of high mobility to the drain characteristics can best be judged from Figure 5, which shows characteristics at 77 K for an ohmic-self-aligned FET—an experimental device, in

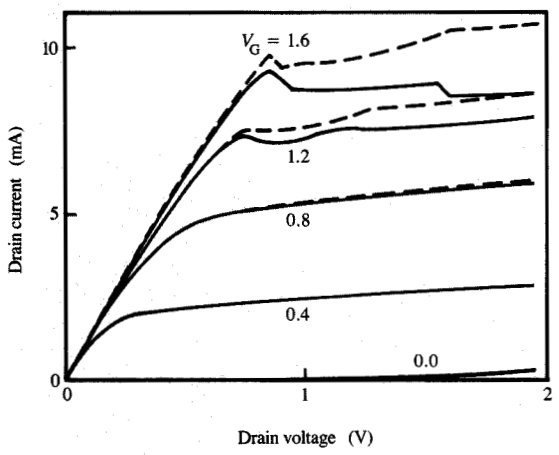

Figure 8

Drain-current (solid) and source-current (dotted) characteristics of a $1 \times 20\text{-}\mu m^2$ SISFET at 77 K. Differences between the curves reflect the influence of hot-electron gate current. The presence of jogs is attributed to parasitic RF oscillations.

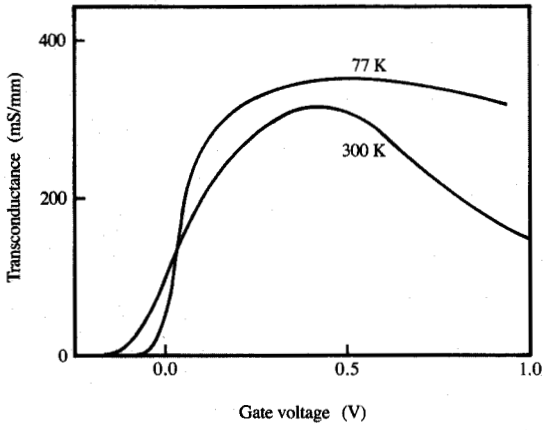

Figure 9

Transconductance vs. gate voltage for a 1-μm SISFET at a drain voltage of 1.0 V.

which the allowed ohmic contacts butt up against the gate. This device was fabricated primarily to demonstrate the very low source-to-drain resistance of the intrinsic FET. (Frank et al. [55] accounted for the parasitic resistances of the "normal" SISFET and obtained a similar set of characteristics for the de-embedded FET.) The characteristics of the SISFET naturally lend themselves to a low-voltage logic application at low temperatures, i.e., the maintenance of a canonical threshold voltage near zero, and the attainment of a large transconductance within 0.2 V of threshold.

Typical gate-current characteristics vs. gate voltage at 77 K are shown in **Figure 10**, with drain voltage as a parameter. At low drain voltage, gate current flows via a thermionic-field emission mechanism [15]. At a larger drain bias, with both gate and drain bias being larger than the barrier height, hot-electron current can flow [55]. It is seen from the figure that the current saturates after an initial rapid increase. Two-dimensional simulations show that at sufficiently large drain voltages, a stable potential configuration exists at the end of the channel which moves into the channel with increasing drain voltage, but otherwise maintains its shape. A "potential window" exists in this region for hot-electron emission, where the electrons are energetic enough to surmount the barrier between the $Al_xGa_{1-x}As$ and the channel while not being excluded by the increasing opposing field in the $Al_xGa_{1-x}As$. This explanation was confirmed by studying hot-electron currents in FETs having gate lengths between 1 and 4 μm, for which the hot-electron current was found to be independent of channel length when the same field configuration at the drain end of the FET was maintained by biasing the FETs to obtain the same *drain current* at the same internal *gate-to-drain voltage.*

The hot-electron effect seems at first to limit severely the voltages on the gate and drain. This was shown not to be the case by circuit simulations [55], where effects were minimal up to a supply voltage of 2 V, since in normal operation the gate and drain voltages are not high simultaneously. In contrast to the Si MOSFET, there is no long-term drift in device characteristics associated with the hot-electron effect, since charge storage times in $Al_xGa_{1-x}As$ are so much shorter than those in SiO_2. We have not seen any obvious degradation of device characteristics due to hot-electron injection, even though our hot-electron currents are many orders of magnitude higher than in Si MOSFETs.

• *ac characteristics of the SISFET*

The gate capacitance of a SISFET closely resembles that of a standard MOS capacitor except that it decreases at high gate bias due to depletion of the gate. (This effect is accentuated in the SATFET structure.) In strong contrast to this, the gate capacitances of the MESFET and MODFET increase at high gate voltage. Correcting the extrinsic transconductance for the known effects of source resistance, we have obtained carrier velocities for $\simeq$0.6-μm FETs of 2.2×10^7 and 1.7×10^7 cm/s at 77 K and 300 K, respectively. Recent microwave

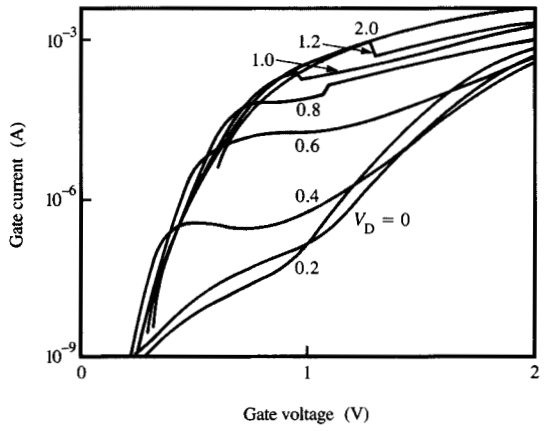

Figure 10

Gate current vs. gate voltage for a 1 × 20-μm^2 SISFET at 77 K, showing the presence of hot-electron current at the higher gate voltages.

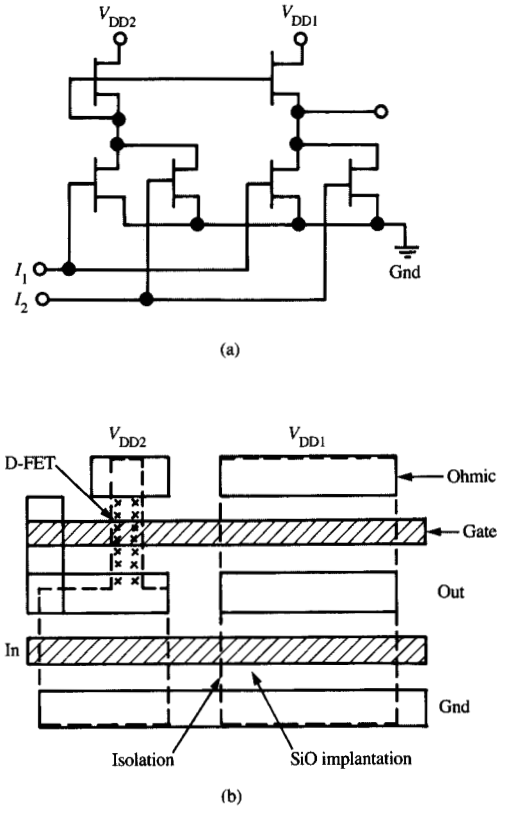

Figure 11

(a) Super-buffer logic NOR circuit; (b) typical layout of an SBL inverter.

measurements by Hirano et al. [56] of NTT at 300 K, and by Kwark et al. [57] of IBM at both temperatures have supported this result. Very high values for the current-gain cut-off frequency, f_T, of 48 GHz and 60 GHz for a 0.6-μm SISFET were obtained at 300 K and 77 K, respectively. The microwave measurements indicate that the low-frequency parameters of the FET are well-preserved up to frequencies of 10 GHz, beyond which the gate resistance causes a degradation of g_{me}. Considerable scatter exists in published f_T values, normalized to gate length. Nonetheless, our f_T values and those of NTT are considerably higher than those reported for both MESFETs and MODFETs in a recent review article [58], and are comparable to the best reported data (obtained with 0.5-μm MESFETs [59]).

• *Circuit applications of the SISFET*

The SISFET can be compared to the n-channel MOSFET in terms of its circuit applications. It has a much higher speed and transconductance than a MOSFET of comparable channel length, and it has a lower voltage range. If clocked at a higher speed, many of the "dynamic" logic configurations used in MOSFET circuits become feasible for the SISFET as well, although our main line of investigation has been for high-speed low-power NOR logic gates.

As described in [34], power can be reduced at low temperatures by reducing voltages. Thus, if manufacturing tolerances permitted direct-coupled NOR gates to be run at a power supply voltage of 0.25 V at 77 K, the power would be reduced by about a factor of 16 from that for a 1.0-V power-supply voltage at 300 K. Unfortunately, the simple DCFL gate has a rather poor noise margin, especially when operating with a large fan-in. In addition, a DCFL circuit is slow when driving with a large wiring capacitance. Both noise margin and ability to drive wiring with a large capacitance can be improved considerably if a super-buffer-type circuit is used, as has been done for MESFETs by Anderson et al. [60]. An SBL NOR gate and the layout of an SBL inverter are shown in **Figures 11(a) and 11(b)**. Although the transistor count is high, the circuit layout is very dense, with the inverter taking $\simeq$300 μm^2 of area at a 1-μm ground-rule layout. The SISFET version needs two power supplies and hence requires additional wiring; however, the lower power supply does not consume much dc current, since only one of the output driver transistors is "on" at a time, as in CMOS logic circuits. Also, as in such circuits, the logic swing is rail to rail, although a

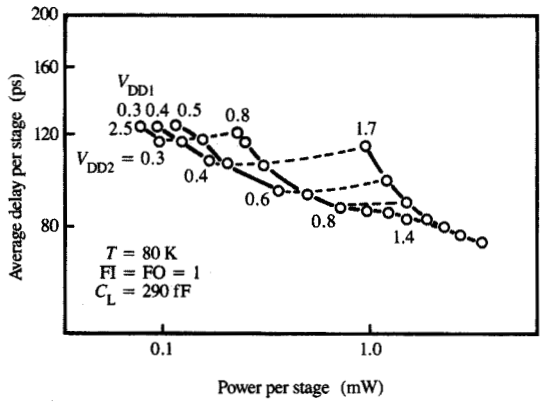

Figure 12

Average delay vs. power (per stage) for a 0.8–0.9-μm SISFET SBL circuit, loaded with 0.29 pF, as a function of the voltage on its two power supplies. The widths of the devices were 5 μm for the input stage E-FET, 2.5 μm for the D-FET, and 10 μm and 15 μm, respectively, for the pull-up and pull-down devices of the output stage.

smaller logic swing is used in order to reduce power to the minimum. Our simulations suggest that at a 0.5-μm gate length, under typical loading conditions applicable to VLSI [fan-in (FI) and fan-out (FO) of 3, C_L = 0.2 pF], a 50-ps delay should be realized at 77 K at a power level of 0.16 mW and power supplies of 0.4 V and 0.56 V. At room temperature the voltages would have to be raised to about 1 V and 1.2 V, and the power at constant delay would increase by about 6 times. Leakage would be important at 1 V at room temperature. It should be possible to achieve a significant improvement to the SISFET by the use of other materials, lattice-matched or pseudomorphic, having larger barrier heights to the channel and gate, as described in the final section.

SISFET circuits have been fabricated both by us and by a group at NTT (Japan). The latter were very high performance frequency dividers [45], with a maximum toggle frequency of 16 GHz at 36 mW for 0.9-μm-gate-length devices. Our ring oscillators displayed gate delays from 20–40 ps for DCFL circuits with resistor and depletion-mode loads and a gate length of 0.7–0.9 μm. This agreed well with simulations using our circuit models. We have also tested asymmetric 6NOR, single-clock-frequency dividers using 0.6–0.7-μm-gate-length FETs and resistor loads. The maximum frequency of division, at room temperature, was 6.4 GHz and 5.8 GHz at power supply voltages of 1.5 V and 1.0 V, respectively, and power dissipations of 7.4 mW and 3.2 mW. The circuit in these dividers was different from that of the NTT group and involved about 4.5 rather than 2 gate delays; hence, the measured delay per gate was comparable in the two cases. The performance and operating regimes of our dividers were predicted accurately by our circuit simulations.

The average delay vs. power (per stage) for one of our SISFET super-buffer circuits, at 77 K, is shown in **Figure 12**. The devices had a 0.8-μm gate length and the circuit was loaded with a 0.29-pF load capacitor (FI = FO = 1). The average delay varied from 80–120 ps for power levels from 4.2 mW to 77 μW. The last result especially, coupled with the agreements between measurements and simulations, lends support to our prediction of the attractive performance of such devices in future high-speed computers.

Complementary-heterostructure FETs

• *Background*

In the 1980s, the CMOS IC technology emerged as the prevailing silicon circuit technology for a wide range of applications requiring not only low power but high speed. The improvement in high-speed performance for liquid-nitrogen-cooled CMOS circuits has been of interest for some time [40] and has now been employed in a commercial high-speed computer, the ETA10 supercomputer [61].

The possibility of exploiting the enhanced transport properties in III–V heterostructures for realizing high-speed complementary circuits superior to Si CMOS circuits is of considerable interest. Some advantage can be gained in C-HFETs even at room temperature as a result of the excellent characteristics of n-channel HFETs at this temperature. However, C-HFETs offer their greatest potential at low temperatures because of the large associated reduction of leakage currents and enhancement of hole mobility by more than a factor of ten.

Various types of p-channel HFETs have been demonstrated. In comparison with n-channel devices, transconductance in p-channel HFETs has been limited not only by the inherently lower mobility of holes, but also by relatively high values of source resistance. This latter factor is a result of the less mature state of the ohmic contact and implantation technologies developed for p-channel HFETs. Transconductances as high as 50 and 110 mS/mm have been obtained for 1-μm implantation-self-aligned MISFETs at 300 and 77 K [62], and further improvements have been achieved more recently, as described in the following.

The development of an attractive scheme for integrating p- and n-channel HFETs having suitable device characteristics has been a critical issue in the development of C-HFET circuits. A variety of device

architectures utilizing planar, vertically integrated, or regrown channel regions have been proposed. The first reported C-HFET structure was based on the integration of n-MESFETs and p-MODFETs [63]. C-HFETs based on n-SISFET/p-MISFET [64], n-MISFET/p-MISFET [65], n-SISFET/p-SISFET [66], and n-MODFET/p-MODFET [67] combinations have also been reported.

The potential circuit performance of (Al,Ga)As/GaAs C-HFET devices has been investigated in computer simulations [68, 69]. Results for 0.7-μm C-HFET circuits indicate that power–delay products 1/5 to 1/8 that of Si-CMOS circuits of comparable gate length should be possible. This power–delay advantage is mainly due to the lower supply voltages possible because of the higher mobilities of electrons and holes in C-HFETs. Circuits based on the use of C-HFETs at 77 K should provide speeds about four times faster than CMOS circuits operated at 77 K, with comparable power dissipation. The simulations also indicate that C-HFET circuits could offer speeds about three times faster than CMOS circuits at 300 K, provided that a reduced circuit density is tolerable and that gate leakage is sufficiently low to permit operation at a 1.25-V supply. Although experimental C-HFET circuit results have thus far been limited, p-channel MODFET ring oscillators have been operated with propagation delays of 233 ps at 77 K [20], and C-HFET ring oscillators have been operated with delays of 76 to 94 ps at 300 K [64, 70] and approximately 60 ps at 77 K [64, 67] for 1.0- to 1.5-μm gate lengths.

• *High-performance C-HFET approach*

Much of the advantage of CMOS circuits over other types of silicon circuits is related to their low static currents. Low static gate and drain currents not only provide low power dissipation, but also contribute to the sharp transfer characteristics needed for high noise margin and make possible the use of dynamic circuits for enhanced logic function.

The previous work on C-HFETs illustrates the range in device design and architecture possible with III–V heterostructures and demonstrates, to some extent, the potential speed of C-HFET circuits. However, the reported approaches are limited in their usefulness for realizing a high-performance circuit technology, primarily as a result of high static leakage currents. In general, gate leakage is much higher in heterostructure FETs because of low associated barrier heights, as discussed earlier in this paper. The useful logic swing in C-HFET circuits is limited by this gate leakage. At the same time, the thresholds of the p- and n-channel FETs must be sufficiently large to ensure very low drain leakage in both logic states. Suitable values are about +0.2 and −0.2 V for n- and p-channel HFETs at a 1.0-V supply. Hence,

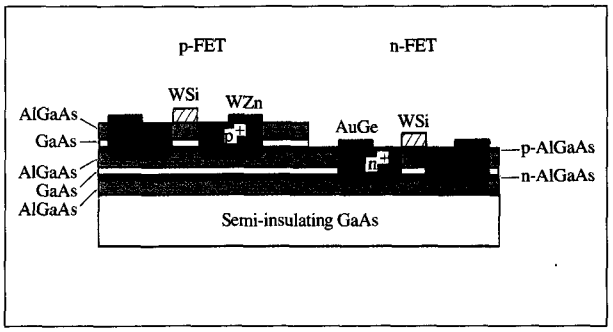

Figure 13

Complementary p- and n-channel HFETs based on a double-quantum-well heterostructure.

the C-HFET device characteristics must be optimized to provide a high large-signal transconductance within a limited logic swing, while exhibiting very low current in the off state. Meeting these requirements requires optimization of the threshold voltages, drain-current characteristics, and gate-current characteristics for both the p- and n-channel FETs.

The C-HFET device architecture shown in **Figure 13** represents a highly attractive approach for meeting the above design constraints for complementary circuits [71–73]. This approach was conceived by Kiehl at IBM. As illustrated, p- and n-type quantum-well channels residing in different strata are vertically integrated in a single heterostructure. The p-channel FETs are fabricated on the full structure and the n-channel HFETs are formed in regions of the wafer where the top layers are removed by compositionally selective etching. Alternating layers of (Al,Ga)As and GaAs define the two quantum wells, while thin impurity layers positioned beneath the wells provide the band-bending required to obtain the desired p- and n-channel threshold voltages. Although two quantum wells are present beneath the gate in the p-channel HFET, appropriate design of the heterostructure layers permits both devices to operate in a fashion similar to that of a single-channel quantum-well MISFET.

• *Quantum-well MISFETs (QW-MISFETs)*

The quantum-well FETs utilized in this approach are based on an (Al,Ga)As/GaAs/(Al,Ga)As heterostructure which is undoped except for a thin layer beneath the quantum well. This type of device also has been referred to as a QW-MI^{3}SFET (for QW-metal-insulator-inverted-interface FET) [74] and an I^2-HEMT (for inverted-interface HEMT) [75].

The band diagram and electron accumulation for an n-channel QW-MISFET under strong forward bias are shown in **Figure 14**. The calculations in this figure are

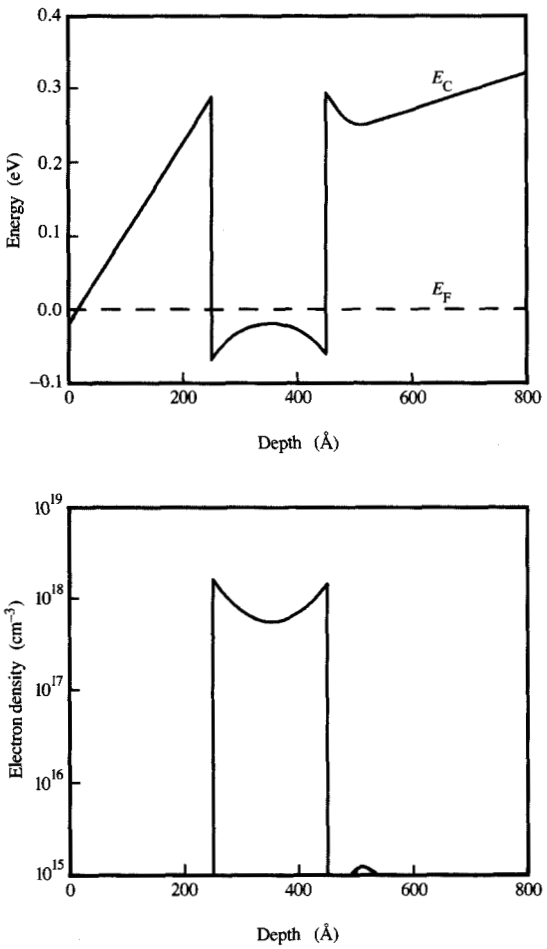

Figure 14

Calculated band diagram and electron accumulation for an n-channel QW MISFET under strong forward gate bias.

based on a numerical model developed by Warren[2] which implements a finite-difference iterative technique to accurately calculate band-bending and charge distributions in heterostructures. Temperature-dependent material parameters and accurate Fermi–Dirac statistics are included, together with a compositionally dependent deep-donor model. The model is one-dimensional; hence, the results correspond to the case of zero drain–source bias.

The QW-MISFET has a number of important advantages over other HFETs for use in complementary circuits. As is apparent from Figure 14, the gate leakage in the QW-MISFET under strong forward bias is determined by vertical transport across an undoped (Al,Ga)As/GaAs heterojunction interface. Thus, gate leakage in this device is the result of the same thermionic, tunneling, and hot-electron injection mechanisms described earlier for the SISFET. Because of the increased barrier at the metal–semiconductor interface, however, the gate-current characteristic of the QW-MISFET is shifted by 0.8 V (toward higher gate voltages) with respect to that of the SISFET. This has the important advantage of significantly increasing the logic swing allowable for a given gate-leakage limit.

The threshold of the QW-MISFET is controlled by the thin doped layer positioned beneath the channel. The doping in this layer serves to bend the energy bands so that electron (or hole) accumulation begins near the bottom of the quantum well at a small bias above threshold. Carrier accumulation at the bottom of the well increases with increased forward gate bias and is followed by an accumulation near the top of the well at high gate bias, as indicated in Figure 14. In effect, the doped layer produces an "inverted" modulation-doped interface which serves to transfer electrons to the channel in addition to those transferred by the gate field, thereby increasing the channel carrier density.

While doping either the channel or the top (Al,Ga)As layer also has been used to shift the FET threshold [11], the QW-MISFET of Figure 14 has important advantages over such alternative structures. Doping the channel is less desirable, since this reduces the mobility due to impurity scattering, particularly at low temperatures. Doping the top (Al,Ga)As layer is less desirable, since it increases gate leakage and parallel conduction. Positioning the doped layer beneath, rather than above, the channel is important for reducing DX-center trapping effects associated with n-type impurities in high-x $Al_xGa_{1-x}As$ layers. Such trapping is reduced in the QW-MISFET due to the partial screening of the gate field by the channel electrons, which limits the change in trap occupation with changes in gate bias [71]. Moreover, the magnitude of x in the bottom $Al_xGa_{1-x}As$ layer can be reduced to a level where trapping does not occur, while retaining a high mole-fraction in the top layer, as is desired for low gate leakage.

An additional advantage of the QW-MISFET results from the quantum-well channel design itself. In single-interface HFETs, electrons are confined at the source end of the gate by the triangular potential well formed by the gate field under forward bias. However, the degree of confinement decreases toward the drain end of the gate, because of the widening of the triangular well by the drain potential. In a quantum-well structure, on the other hand, the bottom confinement barrier is maintained throughout the device, since this barrier is an intrinsic

[2] A. C. Warren, IBM Research Division, Thomas J. Watson Research Center, Yorktown Heights, NY, unpublished work.

feature of the energy bands. It should be mentioned that hot-electron injection over the bottom barrier is possible in the high-field region at the drain end of the gate. However, this effect should have little influence on the device characteristics, since the injected carriers are immediately collected by the drain.

Two potential problems which could limit the transconductance of QW-MISFETs have been dealt with in earlier IBM work: high source resistance and degraded channel mobility. The source resistance R_s tends to be high due to the influence of the quantum well on the ohmic contacts and on the current flow in the access regions outside the gate [71]. Recessed-gate geometries with heavily doped GaAs cap layers have commonly been used to lower the source resistance in MODFETs. The recessed-gate geometry is less effective in QW-MISFETs, however, since the (Al,Ga)As layer is undoped, thereby preventing current flow between the cap and the channel. As a result, the room-temperature sheet resistance r_{sh} is high (~900 Ω/□). (A low r_{sh} value of ~200 Ω/□ is possible, however, at 77 K.) Source resistance also tends to be high in recessed-gate QW-MISFETs because of a high contact resistance R_c (0.5 to 2.0 Ω-mm) at both temperatures. The effectiveness of ion-implanted n^+ regions for reducing R_s in a QW-MISFET is dependent on the conductivity of the n-type (Al,Ga)As layers. Because of the rapid decrease of conductivity in n-$Al_xGa_{1-x}As$ for $x > 0.23$, implantation has not been effective for structures with high mole fractions beneath the channel. However, R_c and r_{sh} values as low as those of MODFETs have been achieved in implantation-self-aligned QW-MISFETs by reducing the mole fraction beneath the channel to 0.2 [72]. The conductivity of p-type $Al_xGa_{1-x}As$ depends only weakly on mole fraction and, hence, the source-resistance of p-channel QW-MISFETs is much less dependent on heterostructure design.

A second potential problem relates to the carrier mobilities attainable in the quantum-well channel. The carrier mobilities near inverted interfaces have generally been lower than those near normal interfaces due to impurity segregation [76] and interface roughness in MBE-grown structures. However, electron mobilities as high as 130 000 cm^2/V-s at 77 K have been obtained for inverted interfaces through the use of modified growth interruptions combined with low growth temperatures [77]. Typical electron mobilities in our QW-MISFET structures are 6000 and 30 000 cm^2/V-s at 300 and 77 K, respectively. The mobility at 77 K exceeds that required for achieving enhanced FET performance.

The mobility is more important in the case of holes, as mentioned earlier. For p-channel QW-MISFETs, we have obtained mobilities as high as 4100 cm^2/V-s with a density of $6.8 \times 10^{11} cm^{-2}$ at 77 K [78], which is comparable to that obtained for normal interface structures [18, 19]. However, since the characteristics of HFETs are dominated by mobility below 10 000 cm^2/V-s, additional improvement in hole mobility is desired. On the basis of the hole mobility in very pure GaAs, it is expected that mobilities approaching 10 000 cm^2/V-s may be possible at 77 K.

• *C-HFETs based on a double-quantum-well heterostructure (DQW-MISFET)*

The integration of p- and n-channel HFETs in the double-quantum-well MISFET (DQW-MISFET) structure of Figure 13 is attractive for realizing high-performance C-HFET circuits from a number of points of view. The vertical integration in this approach is important for device optimization, since this allows critical layer parameters to be optimized independently for the p- and n-channel devices. For example, the AlAs mole fraction x needed to maximize the interface barrier is different for p- and n-channel devices because of the different x-dependences of ΔE_C and ΔE_V shown in Figure 3. Vertical integration allows x to be tailored in the top two $Al_xGa_{1-x}As$ layers to maximize these barriers, while trapping can be eliminated with a low level of x in the bottom (Si-doped) layer. The layers in the vertical structure also possess a useful interrelationship, wherein they mutually enhance the characteristics for both device types. For example, while the p-layer primarily serves to shift the threshold of the p-channel HFET, it also acts to increase the barrier height in the n-channel HFET. Similarly, the n-layer provides threshold shifting for the n-channel HFET, while also serving to reduce drain leakage in the layers beneath the p-channel HFET. The reduction of drain leakage is a useful feature, since the unintentional p-type background of most undoped MBE layers typically results in drain leakage in planar-integrated p-channel HFETs.

With regard to ease of fabrication, the C-HFET structure of Figure 13 allows two important simplifications. First, the epitaxial layers defining the p- and n-channel devices are grown continuously in a single heterostructure, thereby circumventing the potential problems associated with regrowth. Second, gates for both p- and n-channel HFETs may be formed in the same step using processes similar to those developed for GaAs MESFETs, thereby reducing overall fabrication complexity.

For optimized circuit operation with a 1.0-V supply, the p- and n-channel QW-MISFETs must have threshold voltages of about −0.2 and +0.2 V, respectively. The thresholds for the p-channel HFET (in the unetched region) V_{TP} and for the n-channel HFET (in the etched region) V_{TN} are approximately given by

$$V_{TP} = -\phi_P + \Delta E_V + \frac{q}{\varepsilon_1}(N_{sP} - N_{sN})d_1 \qquad (4)$$

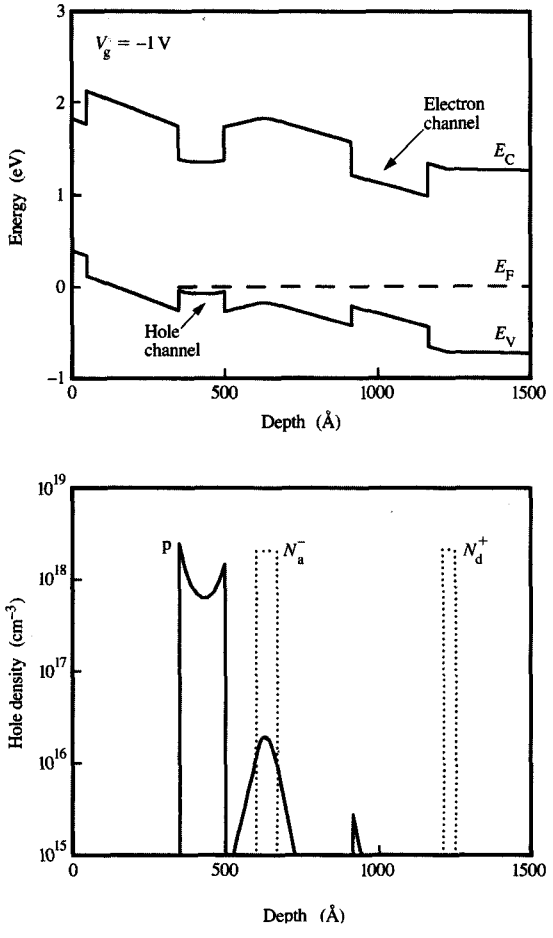

Figure 15

Calculated energy bands and free hole density for p-channel HFET at a gate bias of −1.0 V. Doping densities N_a^- and N_d^+ are also shown.

and

$$V_{TN} = \phi_N - \Delta E_C + \frac{q}{\varepsilon_1}[(N_{sP} - N_{sN})d_2 - N_{sN}d_3], \quad (5)$$

where d_1 is the distance between the surface and the bottom of the p-channel, d_2 is the thickness of the undoped spacer between this channel and the p-layer, and d_3 is the distance between the p-layer and the bottom of the n-channel. The terms N_{sP} and N_{sN} are the sheet doping densities, and ϕ_N and ϕ_P are the surface potentials. Assuming that the Fermi level is at the band edge at threshold, ϕ_P and ϕ_N correspond to ϕ_1 in Equation (1) and ΔE_C and ΔE_V correspond to ϕ_2. The back-field of Equation (1) is implicitly incorporated in N_{sN}. Typically, the spacer d_2 is small, and the n-channel threshold is determined by N_{sN}, while the p-channel threshold is determined by the net density $(N_{sP} - N_{sN})$. Accordingly, the desired threshold can be obtained for both devices simply by adjusting these doping densities for a given set of layer thicknesses. It should be mentioned, however, that the sensitivity of V_{TP} to variations in doping is greater than that for single-channel devices, due to the need to compensate for N_{sN} with N_{sP}.

In addition to the requirement for suitable thresholds, it is necessary that the bottom quantum well of the structure remain depleted of carriers beneath the p-channel device under all bias conditions in order to avoid unwanted capacitive effects and hysteresis. Thus, while the Fermi level must be close to the conduction band of the bottom well in the n-HFET regions (to result in a value for V_{TN} near zero), it must be near mid-gap in the p-HFET regions. This is achieved by exploiting the shift in the Fermi-level position with the removal of the upper layers in the structure, as first described in [63]. Because of this shift, the threshold of the bottom channel in the p-HFET (unetched) region differs from V_{TN} and is given by

$$V'_{TN} = \phi_N - \Delta E_C + \frac{q}{\varepsilon_1}[(N_{sP} - N_{sN})(d_1 + d_2) - N_{sN}d_3]. \quad (6)$$

Thus V'_{TN} is considerably larger than V_{TN}, thereby ensuring that the bottom quantum well is maintained depleted of electrons beneath the p-HFET even under large reverse gate biases (equivalent to a voltage on the gate which is greater than a typical C-HFET supply voltage). It may be possible to populate the bottom well because of electron heating at high drain bias; however, such effects have not been observed in our experiments, as discussed later.

In order to check the validity of the threshold equations, calculations were performed for the actual DQW-MISFET structure of our experiments using the model mentioned above. Although carrier transport was not included, the band-bending and charge distribution could be determined, since the applied gate voltage is known to drop between the gate and top quantum-well channel as a result of the highly conductive state of this channel and the nearby implanted source region. The results for a −1.0-V gate bias are shown in **Figure 15** for top and bottom quantum wells of 15 and 25 nm, respectively; other layer parameters were assumed to be identical to those of the experimental structure described below. A 2D hole-gas with a sheet density 1.5×10^{12} cm^{-2} forms in the top quantum well while the lower channel remains virtually depleted of carriers because of the screening of the gate field by the 2D hole-gas.

• *QW-MISFET fabrication*

The p- and n-channel QW-MISFETs are fabricated with p^+ and n^+ source and drain regions which are self-aligned to refractory metal gates, as shown in Figure 13. For the double-quantum-well heterostructure, the fabrication process begins with the removal of layers in the n-channel HFET regions using a selective wet-chemical etch. Refractory WSi_x gates are then fabricated using a technology similar to that developed at IBM for GaAs MESFET circuits [79]. Following the blanket sputter-deposition of a WSi_x film, gates for both p- and n-channel devices are patterned and etched by CF_4/O_2 reactive ion etching. SiN_x is then deposited by plasma-enhanced chemical vapor deposition and formed into sidewalls by reactive ion etching.

The fabrication of implanted source and drain n^+ regions for the n-channel QW-MISFETs is similar to that used for GaAs MESFETs and SISFETs. The n^+ regions are formed by $^{29}Si^+$ implantation at 60 keV with a dose of $5 \times 10^{13} cm^{-2}$. Implantation activation is achieved by rapid thermal annealing at 875°C for 1 s in an arsine atmosphere [54]. Ohmic contacts for the n-channel FETs are based on a Ni–Au–Ge metallurgy and are alloyed at 570°C.

A key part of the C-HFET process is the fabrication of p-channel devices with a self-aligned geometry. Low-sheet-resistance p-type regions can be formed by implantation of such dopants as Be. However, such Be-implanted regions typically show excessive diffusion during annealing, making it difficult to achieve suitable shallow p-type regions. Lateral diffusion of Be is a particularly serious problem for implantation-self-aligned HFETs. Following the work at IBM by Tiwari et al. [80], we employ a sputter-deposited W/Zn film and rapid thermal diffusion to obtain controllable, shallow Zn-diffused regions. Key steps in the fabrication process used here are 1) chemical vapor deposition of a SiN_x film and patterning to open windows for the p^+ diffusion, 2) sputter deposition of a layered W/Zn film, 3) rapid thermal diffusion at 675°C, 4) masking of the contact regions with a Ti/Au film, and 5) chemical etching in a solution of H_2O_2 for removal of the W/Zn film except in contact regions. This self-aligned diffusion process has advantages over previously described W/Zn self-aligned ohmic processes [81] in that it requires no planarization step.

• *QW-MISFET characteristics*

Fabrication of p-channel QW-MISFETs based on the p/n double-quantum-well heterostructure of Figures 13 and 15 has been carried out [73]. The source and drain regions were formed by self-aligned diffusion, and the gate length and source-to-drain contact spacing were 1.5 μm and 6.0 μm, respectively. The (Al,Ga)As/GaAs heterostructure consisted of the following layers: 500-nm GaAs buffer; 100-nm u-$Al_{0.4}Ga_{0.6}As$; 3-nm n-$Al_{0.4}Ga_{0.6}As$:Si(2.0×10^{18}); 5-nm u-$Al_{0.4}Ga_{0.6}As$; 25-nm u-GaAs; 25-nm u-$Al_{0.4}Ga_{0.6}As$; 6-nm p-$Al_{0.4}Ga_{0.6}As$:Be(2.0×10^{18}); 10-nm u-$Al_{0.4}Ga_{0.6}As$; 15-nm u-GaAs; 30-nm u-$Al_{0.4}Ga_{0.6}As$; 5-nm u-GaAs (top); u designates undoped layers, and doping concentrations per cubic centimeter are indicated within parentheses. This structure included two quantum wells which were 15 and 25 nm thick and served as hole and electron channels, respectively. Thin p- and n-type impurity layers were positioned beneath the wells.

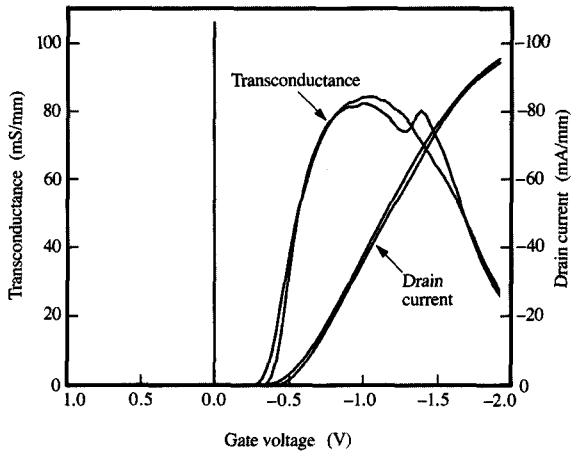

Figure 16

Transconductance and drain-current characteristics at 77 K for a p-channel DQW-MISFET having a 1.5×100-μm^2 gate and a 6-μm source–drain contact spacing. Curves with and without illumination are shown and indicate that no unwanted charge storage occurs in the double-well structure. (V_d = 2.0 V.) From [73], reproduced with permission; ©1989 IEEE.

Transmission-line measurements of R_c and of r_{sh} in the diffused p^+ regions performed subsequent to the removal of the W/Zn film give values of 0.29 Ω-mm and 289 Ω/□, respectively, at 300 K. At 77 K, R_c and r_{sh} were found to be 0.74 Ω-mm and 176 Ω/□. These values translate into source-resistance values of less than 1 Ω-mm for FETs with 1-μm source–gate spacings, which is considerably below previously reported values for p-channel HFETs.

At room temperature this device exhibited high gate leakage and a low transconductance of 17 mS/mm. At 77 K, however, both the leakage characteristic and transconductance improved dramatically, as shown in **Figures 16** and **17**. The transconductance reached 82 mS/mm and the gate-current characteristic shifted markedly to higher forward voltages, thus allowing

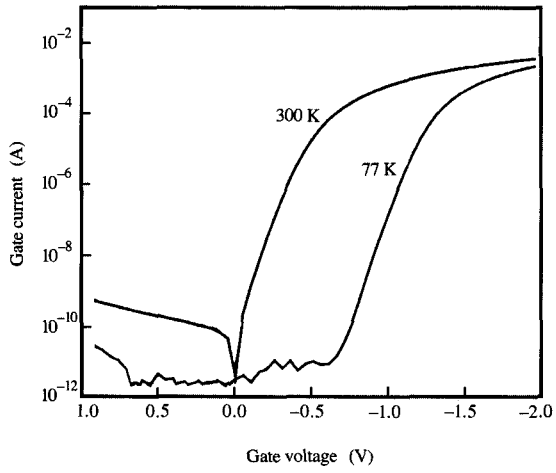

Figure 17

Gate-current characteristics of p-channel DQW-MISFET at 300 K and 77 K. From [73], reproduced with permission; ©1989 IEEE.

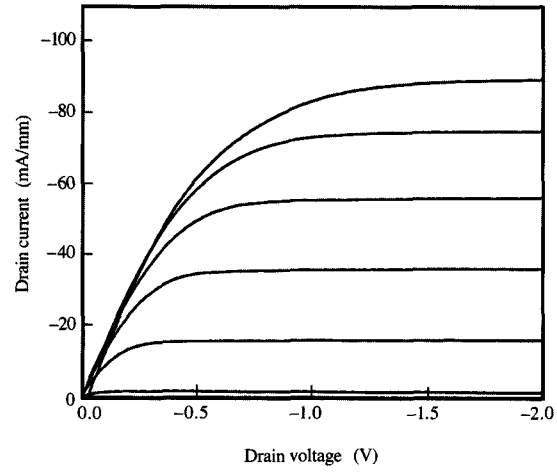

Figure 18

Drain current vs. drain voltage for p-channel DQW-MISFET at 77 K. Gate voltage for top curve: −1.75 V; magnitude of steps: +0.25 V. From [73], reproduced with permission; ©1989 IEEE.

operation at a forward gate bias of −1.1 V with a leakage three orders of magnitude below the drain current. It is also seen that a high K-factor ($K = \partial g_{me}/2\partial V_g$) of 0.17 S/V-mm and excellent pinch-off were obtained.

The characteristics in Figure 16 cover a wide range of gate bias, including large reverse biases, at a high drain bias of −2.0 V under both dark and illuminated conditions. No indication of unwanted carrier accumulation in the bottom quantum well of the double-quantum-well structure is apparent in the characteristics, which are normal in all respects. (The small bump in the characteristic in the dark at large forward biases is commonly observed in conventional device structures and is associated with the turn-on of gate current.)

The drain current vs. drain voltage characteristics shown in **Figure 18** at 77 K are strikingly ideal in shape, exhibiting nearly complete saturation in drain current. The source–drain resistance R_d was 5.9 Ω-mm. The extremely low output conductance of 0.57 mS/mm in the saturation region indicates both excellent hole confinement by the quantum well and the effectiveness of the buried n-type layer in eliminating drain leakage in the underlying layers.

These results contrast strongly with the reported results for other self-aligned p-HFETs, which show poor pinch-off and weak current saturation [62, 65]. The ratio g_{me}/g_d is an important figure of merit and relates to inverter gain in digital circuits. This ratio was 140 for this device, which is far above that obtained in other reported p-HFETs.

More recently, the characteristics of similar p-HFETs with more optimized device geometries have been examined. These devices contained 1.0-μm gate lengths and 2.5-μm source–drain spacings and are fabricated on a double-quantum-well structure similar to that described above. Transconductances of nearly 60 and 150 mS/mm were obtained at 300 and 77 K, respectively, the best values yet obtained for p-channel (Al,Ga)As/GaAs HFETs.

In addition, n-channel QW-MISFETs were fabricated on the same double-quantum-well wafer which contained the p-channel QW-MISFETs of Figures 16 through 18. The implantation-self-aligned devices were fabricated in regions where the top layers were removed by compositionally selective etching, as described above, and contained 1.5-μm-gate-length and 6.0-μm source–drain spacings. The measured transconductance of these devices was 105 and 165 mS/mm at 300 and 77 K, respectively. These g_{me} values were lower than for more optimized devices as a result of the larger gate-to-channel spacing (41 nm) and higher source resistance (R_c = 0.9 Ω-mm, r_{sh} = 415 Ω/□) of this structure. However, the characteristics were normal in all respects, exhibiting low gate leakage and a threshold uniformity comparable to that for non-etched QW-MISFETs, thereby demonstrating the feasibility of the vertical integration scheme.

Also examined were n-channel QW-MISFET devices with more optimal layer parameters [72]. The devices

had 1.5-μm gate lengths and 6.0-μm source–drain spacings and were fabricated on the following layers: 500-nm GaAs; 120-nm $Al_{0.2}Ga_{0.8}As$; 25-nm GaAs; 20-nm $Al_{0.4}Ga_{0.6}As$; and 5-nm GaAs (top). The structure was undoped except for a delta-doped n-type region with a Si sheet density of 2×10^{12} cm^{-2} positioned 5 nm beneath the quantum well. The mole fraction beneath the channel in this structure was 0.2, as desired for eliminating trapping effects and reducing source resistance. The measured values of R_c and r_{sh} in the access regions were 0.07 Ω-mm and 385 Ω/□, respectively, at 300 K. At 77 K they were 0.20 Ω-mm and 305 Ω/□, respectively. These parasitic resistances are much lower than obtained in early QW-MISFETs and are comparable to values for GaAs MESFETs fabricated by similar self-aligned processes [82].

The transconductance, drain-current, and gate-current characteristics at 300 K are shown in **Figure 19** for devices with $x = 0.2$ in the bottom barrier. The characteristics show that the device turns on rapidly above threshold with a K-factor equal to 0.15 S/V-mm, reaching a transconductance of 215 mS/mm. The logarithmic plot of drain current in this figure reveals an excellent subthreshold characteristic with full pinch-off of the channel. This is important for ensuring a low static drain current and indicates that electrons associated with the impurities are effectively transferred to the quantum well and do not contribute parallel conduction in the underlying layers. The gate-current characteristics shown in Figure 19 represent a worst-case condition with regard to hot-electron injection, since V_d is high (2.0 V). It is seen that that device exhibits low gate leakage even for large forward biases. In particular, the leakage is more than three orders of magnitude below the drain current for biases as high as 1.2 V.

The drain current vs. drain voltage characteristics at 300 K in **Figure 20** exhibit current saturation, with a g_d equal to 3.1 mS/mm. The minimum source–drain resistance is 3.8 Ω-mm and is consistent with what is expected because of the rather large 6.0-μm source–drain spacing in these devices. Improvement in device characteristics is seen upon cooling to 77 K. In particular, an increase in the peak transconductance to 350 mS/mm is obtained.

These results demonstrate that devices with excellent characteristics can be realized with QW-MISFETs integrated in a simple single-growth structure. The flexibility of layer parameters provided by the vertical integration scheme permits further improvements. In particular, a DQW-MISFET structure with $x \simeq 1.0$, 0.4, and 0.2 in its upper, central, and lower $Al_xGa_{1-x}As$ layers, respectively, would provide the maximum valence-band discontinuity in the hole barrier ($x = 1.0$ in the upper layer) and maximum conduction-band discontinuity in the electron barrier ($x = 0.4$ in the central layer), while eliminating DX-center-related trapping effects ($x = 0.2$ in the lower layer). While the growth of high-quality layers at mole fractions

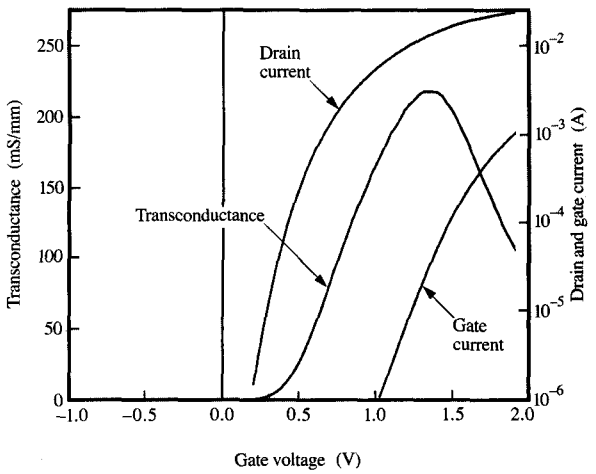

Figure 19

Transconductance, drain-current, and gate-current characteristics at 300 K for an n-channel QW-MISFET having a 1.5×100-μm^2 gate and 6-μm source–drain contact spacing. ($V_d = 2.0$ V.)

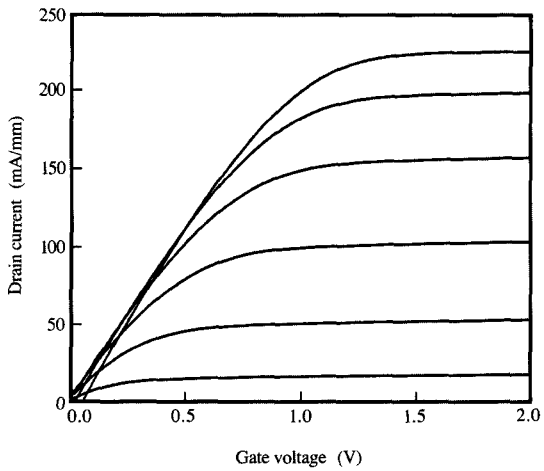

Figure 20

Drain current vs. drain voltage at 300 K for n-channel QW-MISFET. Gate voltage for top curve: 2.0 V; magnitude of steps: −0.25 V.

approaching 1.0 is technologically challenging, use of a high mole fraction in the p-channel barrier would result in an increase in the valence-band discontinuity by as much as a factor of 2.5, thereby greatly improving the possibility for room-temperature C-HFET operation.

Other III–V materials systems

The (Al,Ga)As system has been strongly emphasized in the work on heterostructure FETs to date. This system is attractive because of its closely matched lattice constants, good electron transport properties, and high-quality semi-insulating substrates. In addition, it is by far the most advanced III–V system from a materials growth standpoint. As we have seen above, the SISFET and the QW-MISFET devices are especially well suited to take advantage of the (Al,Ga)As band structure while circumventing deficiencies in this system such as DX-center electron trapping.

Other III–V materials systems offer further improvement of HFET devices as a result of both enhanced transport properties and increased band discontinuities. The increase in band discontinuities and intervalley separations in some of these materials systems provides enhanced high-field transport and increased quantum-confinement energies [83], which could be crucial to the successful scaling of HFETs to dimensions of less than 0.1 μm.

As demonstrated at IBM in the early 1970s by Matthews and Blakeslee [84], mismatched materials can be incorporated in heterostructures to form stable pseudomorphic (strained) layers, provided that the mismatch is small and the layers are thin. MESFET-like devices composed of a 17-period $In_{0.2}Ga_{0.8}As/GaAs$ strained-layer superlattice were the first FETs to be based on such materials [85]. For GaAs substrates, the InAs mole fraction y is limited by strain to about 0.2 in a $Ga_{1-y}In_yAs$ layer 20 nm in thickness, typical of that in a quantum-well HFET. A pseudomorphic HFET based on such a single-quantum-well channel was first reported by workers at IBM and Brown University [86] in their demonstration of $GaAs/In_{0.15}Ga_{0.85}As$ MODFETs. Recent work on similar $Al_{0.2}Ga_{0.8}As/In_{0.15}Ga_{0.85}As$ MODFETs [87] has resulted in significant improvements in millimeter-wave performance compared with conventional MODFET structures. While the role played by electron transport in these performance improvements is still unclear [88], pseudomorphic channels offer the advantage of increased electron density because of an increase in ΔE_C by about 0.15 eV over that for a GaAs channel.

The increased ΔE_C in pseudomorphic structures is also attractive for SISFETs and QW-MISFETs. An $In_{0.15}Ga_{0.85}As$ quantum-well channel would be attractive for increasing ΔE_C at the low-mole-fraction interface in a QW-MISFET. In addition, the negative threshold shift caused by the increased offset would ease threshold control to some extent. Although the negative threshold shift in an $In_{0.15}Ga_{0.85}As$-channel SISFET is undesirable, the increased offset would be useful for reducing its room-temperature gate current. Alternatively, (Ga,In)As should be attractive as a gate material in the SISFET, since the threshold shift should be in the correct direction for normally-off operation and since the reverse gate leakage should be lower.

The use of pseudomorphic InGaAs channels may also lead to improvements in p-channel quantum-well HFETs. While the increase in the valence-band offset is small for $In_{0.15}Ga_{0.85}As$ channels, strain-induced splitting of the light and heavy hole bands leads to a significantly enhanced hole mobility at low temperatures [89]. Hole mobilities as high as 8000 $cm^2/V\text{-}s$ have been achieved at 77 K for hole densities in the low 10^{11}-cm^{-2} range [90]. Unfortunately, the mobility enhancement decreases with increasing hole density because of valence-band nonparabolicity [91], thereby limiting the improvements expected at the 1×10^{12}-cm^{-2} densities required in HFETs. The experimental evidence for strain-enhanced mobility in p-channel HFET characteristics has thus far been obscured in experiments by the high source resistance in recessed-gate devices [92] and the likelihood of lateral diffusion in Be-implanted devices [93]. Further work is needed to establish the benefits of this approach.

Higher InAs mole fractions are possible in (Ga,In)As layers lattice-matched (or strained) to other substrate materials. Of particular interest are $Al_{0.48}In_{0.52}As/Ga_{0.47}In_{0.53}As$ heterostructures which are lattice-matched to InP substrates and similar pseudomorphic structures. $Ga_{0.47}In_{0.53}As$ channels offer an improved room-temperature electron mobility due to the lower effective mass for electrons in this material. Mobilities as high as 15 300 and 123 000 $cm^2/V\text{-}s$ have been achieved at 300 and 77 K, respectively, in modulation-doped heterostructures with strained $Ga_{0.2}In_{0.8}As$ on InP [94].

The lattice-matched system also offers a larger conduction-band discontinuity (0.52 eV) and appears to exhibit minimal trapping effects [95]. In addition, the low surface potential for both $Al_{0.48}In_{0.52}As$ and $Ga_{0.47}In_{0.53}As$ lowers source resistance as a result of reduced contact resistance and reduced surface depletion. Increased impact ionization represents a potential disadvantage for these and other materials with narrow bandgaps (0.73 eV for $Ga_{0.47}In_{0.53}As$), and kink-like anomalies have often been observed in the dc characteristics of MODFETs fabricated from these materials. $Al_{0.48}In_{0.52}As/Ga_{0.47}In_{0.53}As$ MODFETs with 0.1-μm gates have exhibited outstanding performance, with transconductances as high as 1000 mS/mm and a record millimeter-wave f_t of nearly 200 GHz [96]. Propagation

delays as low as 5 ps at 77 K have also been reported for ring oscillators based on normally-on MODFETs [97].

MODFETs fabricated from $Al_{0.48}In_{0.52}As/Ga_{0.47}In_{0.53}As$ have normally-on thresholds even for low doping levels because of the lower surface potential and increased ΔE_C of these materials. Structures with undoped or slightly p-type layers are required for obtaining the normally-off thresholds needed for low-power digital circuits. This materials system is particularly attractive for SISFETs, where the higher ΔE_C would enhance the feasibility of room-temperature operation because of lower thermionic and tunneling currents. While the increased ΔE_C would also tend to reduce hot-electron injection, the influences of lower effective mass and increased intervalley separation are less clear and more difficult to predict. InP-based QW-MISFETs could provide some advantage over GaAs-based QW-MISFETs in terms of ease of threshold control, since the threshold in undoped $Al_{0.48}In_{0.52}As/Ga_{0.47}In_{0.53}As$ QW-MISFETs would be close to optimal for normally-off operation. Preliminary work on both SISFET and MISFET devices in these materials has been reported [98, 99].

Heterostructures of $Al_{0.48}In_{0.52}As/Ga_{0.47}In_{0.53}As$ are also attractive for p-channel HFETs. The metal–semiconductor barrier and valence-band discontinuities are approximately 0.86 and 0.28 eV, respectively, and are comparable to those of $Al_{0.5}Ga_{0.5}As/GaAs$. Experimental 1.0-μm p-channel MISFETs with a g_{me} of 25 mS/mm at 77 K have been reported [100] for devices in these materials. The transconductance in these devices is limited by the high threshold (−0.7 V) of the undoped MISFET, which limits the forward gate swing. However, improved low-temperature performance should be possible in more optimized devices. The mobility at 300 K for these materials is comparable to that for AlGaAs/GaAs and still represents a limiting factor at room temperature. (A value for g_{me} of 8 mS/mm has been obtained at 300 K.)

Although in a very early stage of development, other narrow-gap III–V materials, such as the (Al,Ga)Sb materials system, may provide improved p-channel characteristics at room temperatures. This system has recently received attention for heterostructure bipolar transistors [101] and offers lower effective masses for both electrons and holes. In addition, the (Al,Ga)Sb system is more closely lattice-matched than most other III–Vs and has a maximum ΔE_V of about 0.40 eV. Hole mobilities as high as 1000 and 8000 cm^2/V-s have been obtained in GaSb at 300 and 77 K, respectively.

Concluding remarks

In this paper we have reviewed work on heterojunction FETs and their applicability to high-speed logic circuits, especially at liquid-nitrogen temperatures. We have focused on two logic-circuit approaches: the use of n-channel E/D logic circuits with GaAs gate FETs (SISFETs), and complementary logic circuits with p- and n-channel quantum-well MISFETs (QW-MISFETs).

Exploration of the use of the SISFET has progressed to the testing of simple logic circuits and the demonstration of high-speed capability under a realistic loading condition. The SISFETs have been characterized at both dc and microwave frequencies. The n-channel SISFETs show effective carrier velocities (as measured by g_{me}/C and f_T) which are comparable to those of the best GaAs FETs and are even higher at 77 K.

Exploration of QW-MISFETs has demonstrated p- and n-channel FETs with dc characteristics suitable for high-performance, low-temperature C-HFET circuits utilizing the integration of p-channel and n-channel FETs within the same layered structure. The p-channel QW-MISFETs based on a double-quantum-well heterostructure exhibit superior device properties and the highest transconductance yet reported for GaAs p-channel FETs.

Both approaches offer a high speed capability at considerably lower power levels than Si bipolar transistor circuits while being much faster than silicon CMOS circuits. The SISFET/SBL approach is faster and uses less area than the QW-MISFET/C-HFET approach; yet the C-HFET approach consumes less power, especially at lower clock rates (below ~250 MHz).

Part of the advantage of these approaches is a result of lower operating voltages compared with silicon circuits. The use of reduced voltages leads to smaller power–delay products. However, the use of lower voltages also leads to smaller absolute noise margins and, hence, greater sensitivity to process variables, especially those causing threshold voltage shifts. The optimal logic swing for the E/D SISFET at 77 K is ~0.4 V compared to ~1.2 V for the C-HFET, as dictated by power and speed considerations rather than breakdown voltages. Were the SISFET also to require use of 1.2 V, it would suffer a considerable power–delay product disadvantage. The lower operating voltage and narrower margins of the SISFET approach are mitigated by the lower sensitivity of the E-FET threshold to process variables. While the D-FET threshold control is a problem, especially considering the sensitivity of the present ion-implanted D-FET to epitaxial-layer thickness, for an SBL circuit, this affects circuit speeds more than noise margins. The higher sensitivity of QW C-HFET thresholds to variations in doping-thickness product, especially that of the top (p-) HFET, are mitigated by the reduced sensitivity of the higher-voltage C-HFET circuits to such variations.

Should cryogenic environments become key to future high-end computers, the high-speed, low-power characteristics of these two approaches should make them very attractive. Room-temperature operation is less attractive, but remains a possibility for both. Leakage-current issues could be addressed by using other III–V materials combinations. The speed issue for C-HFETs at room temperature, caused by low barrier heights and low hole mobility, could be alleviated by clever circuit design, although a materials solution would be preferable. Given the results achieved to date and the promise of further improvements, these HFET technologies should enjoy a wide range of high-speed digital and opto-electronic applications.

Acknowledgments

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