Submicron-gate-length GaAs MESFETs

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It is well known that reducing gate length is a powerful means to increase the transconductance and transit frequency of GaAs MESFET devices. However, by reducing the gate length without scaling channel doping and thickness, the performance obtained is limited by short-channel effects and parasitics. In this paper we present an overview of our work on two different MESFET structures, illustrating how device performance can be increased by decreasing the gate length, with the result that appropriately scaled MESFETs compare favorably with GaAs–AlGaAs heterojunction FETs. From our work—including some recent results on 0.15-μm-gate-length implantation-self-aligned MESFETs—we conclude that it should be possible to increase the speed of high-speed GaAs MESFET (logic, analog, and microwave) circuits through the use of devices having gate lengths less than 0.5 μm.

Introduction

Although the GaAs MESFET is currently the most important commercial GaAs device for both logic and microwave circuits, recent GaAs device research activities have concentrated on heterojunction FETs (HFETs). The large low-field electron mobility at GaAs/AlGaAs (and other III–V) heterojunction interfaces and the ease with which structures with aggressive vertical scaling can be grown by MBE or MOCVD have yielded devices with impressive performance, especially at short gate lengths.

Using the same means applied to state-of-the-art heterojunction FETs (namely epitaxial channels and submicron lithography), GaAs MESFETs can also yield advanced performance for short-gate-length devices with thin, highly doped channels. Additional advantages of submicron MESFETs include a relatively large charge confinement barrier (at least compared to the AlGaAs/GaAs HFET), a simple structure, and a relatively mature circuit technology.

The performance increase of GaAs MESFETs by fabricating fully scaled, submicron-gate-length devices has been demonstrated for both recessed-gate [1] and implantation-self-aligned MESFET structures [2]. The importance of the implantation-self-aligned structure lies in its similarity to the well-established silicon VLSI device technologies and its particular suitability for digital circuits.

In this paper an overview of work done at the IBM Zurich Research Laboratory on recessed-gate MESFETs is presented first. Then an overview of work done at the IBM Thomas J. Watson Research Center on self-aligned MESFETs, including some recent results on devices having 0.15-μm gate lengths, is presented. For both types of devices we show that the fully scaled MESFET is comparable to the GaAs HFET with regard to its transconductance, k-factor, and transit frequency. From comparable performance as well as circuit advantages of the GaAs MESFET, we conclude that for digital logic circuits as well as analog and microwave circuits, the GaAs MESFET remains an attractive alternative to the GaAs HFET.

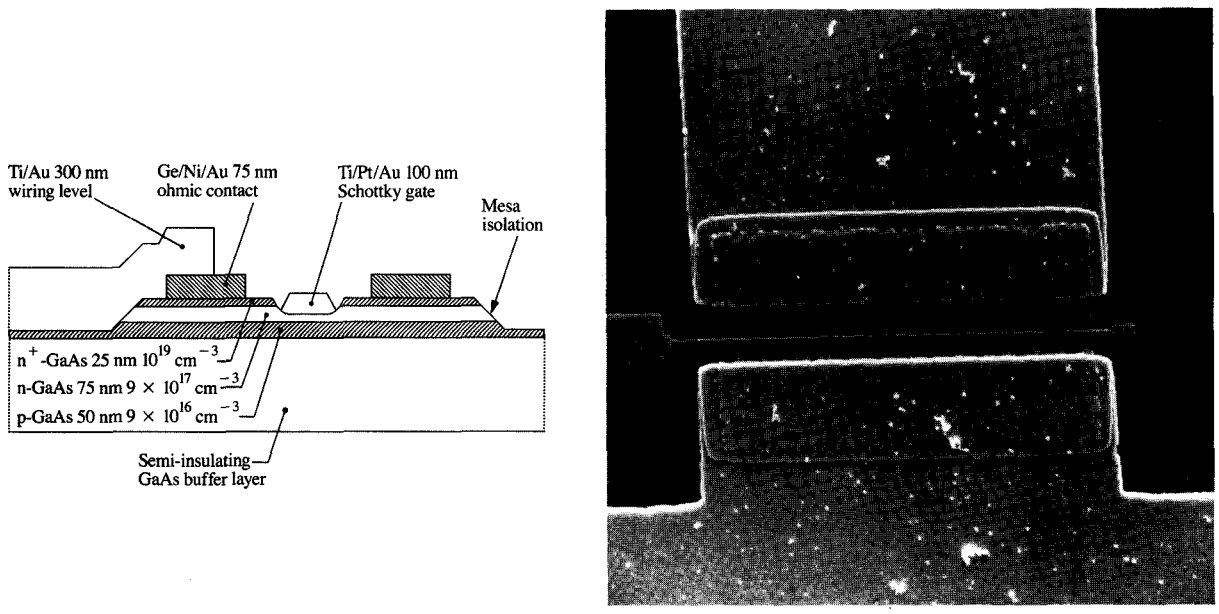


Figure 1

(a) Recessed-gate GaAs MESFET cross section. (b) Micrograph of such a device with a gate length of 0.25 μm.

Recessed-gate MESFET

The recessed-gate structure is the traditional MESFET device structure used in microwave applications [3]. In this section we describe the fabrication of submicron-gate-length recessed-gate MESFETs on very thin epitaxial channels. The purpose of our effort was to investigate thin-channel MESFETs, a task for which the chosen structure is very well suited, and to determine the intrinsic potential of the GaAs MESFET.

First device structure is discussed and the fabrication process of the recessed-gate MESFET is described. Then its device parameters are analyzed. Finally the gate-length dependence of the high-frequency capacitance and transit frequency is presented.

• *Fabrication*

The structure of the recessed-gate GaAs MESFET and a micrograph of such a device with a gate length of 0.25 μm are shown in **Figure 1**. Device fabrication starts with the growth of the required semiconductor layers by MBE. On a semi-insulating GaAs wafer, an undoped buffer layer is grown, followed by a 50-nm-thick 9×10^{16}-cm^{-3} beryllium-doped p-layer, a 75-nm-thick 9×10^{17}-cm^{-3} silicon-doped n-type channel layer, and a 25-nm-thick 10^{19}-cm^{-3} silicon-doped n^+ contact layer. The buried p-layer is fully depleted by the built-in potential of the p–n diode; it is included to improve the confinement of electrons in the MESFET channel by the field created by the acceptor atoms. An alternative approach is the use of a buried AlGaAs layer which creates a similar barrier for the electrons in the channel [4].

Fabrication continues with the deposition of Cr/Ti/Pt alignment marks for chip registration. Next, Ge/Au/Ni/Au ohmic contacts are deposited and alloyed at 370°C, and mesas defining the device active areas are etched to a depth of 120 nm using a 1:8:1000 H_2SO_4:H_2O_2:H_2O solution. After exposure and development of the gate pattern, the same etchant is used to etch through the n^+ contact layer before the metallic gate is deposited. This procedure results in a thin MESFET channel (25–45 nm in thickness) beneath the gate and a self-aligned spacing of 0.1 μm between the gate and the 100-nm-thick contact layers at both the source and drain ends. A 100-nm-thick Ti/Pt/Au Schottky gate is deposited after removing resist residues in an oxygen plasma and removing any oxide at the GaAs surface using 1:1 HCl:H_2O. These cleaning steps have been found to substantially improve the Schottky diode ideality factor on highly doped epitaxial layers. Finally the devices are completed by adding a 300-nm Ti/Au wiring level which connects the devices to bond pads.

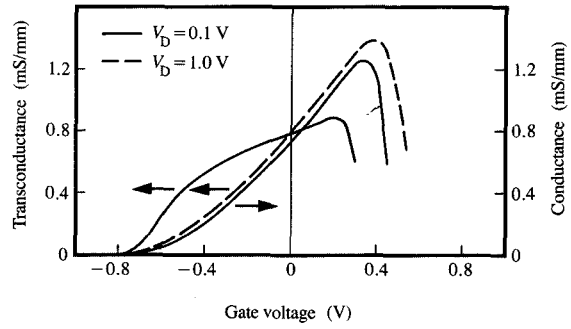
All resist exposures are carried out by direct-write electron-beam lithography. For the gate level, two layers of PMMA with different molecular weights are used to ensure a good lift-off profile with reproducible undercut [5]. For definition of the mesa patterns, a Novolak-type

positive photoresist is used as a negative electron-beam resist. After electron-beam exposure of the mesa pattern, the resist is flood-exposed with UV light and developed. The areas exposed by the electron beam are cross-linked and remain undeveloped. For all other metal layers, use is made of a double-layer resist process (Novolak on PMMA) which makes possible the lift-off of 300-nm-thick layers.

• *dc characteristics*

Figure 2(a) shows the dc characteristics of a large-area (100 μm by 75 μm) recessed-gate MESFET. Its transconductance in the saturated region (V_D = 1 V, where V_D is the drain-to-source voltage) is compared to its conductance in the linear region (V_D = 0.1 V). Both differ only by a small voltage shift which is due to the nonzero output conductance in the saturated region. This equality of transconductance and conductance follows from assuming a field-independent mobility in a long-gate-length device [6]. This property can be used to detect velocity saturation in submicron devices: When the conductance continues to increase as a function of gate voltage while the transconductance saturates, and the conductance is larger than the transconductance, one can conclude either that the device has nonlinear contacts or that velocity saturation occurs within the device. From measurements on contact-resistance test structures on the same wafer, one can exclude the possibility of nonlinear contacts and conclude that the transconductance saturation is caused by velocity saturation in the channel. Since velocity saturation depends on gate length and channel thickness, these effects are observed mainly for depletion-mode devices and increasingly so for those having shorter gate lengths. Enhancement-mode devices (discussed below) having a gate length of 0.5 μm do not show transconductance saturation resulting from velocity saturation due to their thin channels and low pinch-off voltage. The superlinear behavior of both the conductance and transconductance shown in **Figure 2(a)** is due to the variable thickness of the depletion layer with applied voltage [6].

The transconductance of the large-area recessed-gate MESFET in the linear region (V_D = 0.1 V) is also shown in **Figure 2(a)**. It can be shown that this transconductance is proportional to the small-signal capacitance. From the ratio of both capacitance and transconductance measurements, the MESFET channel mobility can be obtained as a function of depth. Capacitance-versus-voltage measurements can also yield the channel doping as a function of depth. Both channel mobility and doping as a function of depth are shown in **Figure 2(b)**. The channel mobility is 2500 cm^2/V-s for a doping level of 9×10^{17} cm^{-3}. For a depth beyond 60 nm, the measurement becomes unreliable due to the low



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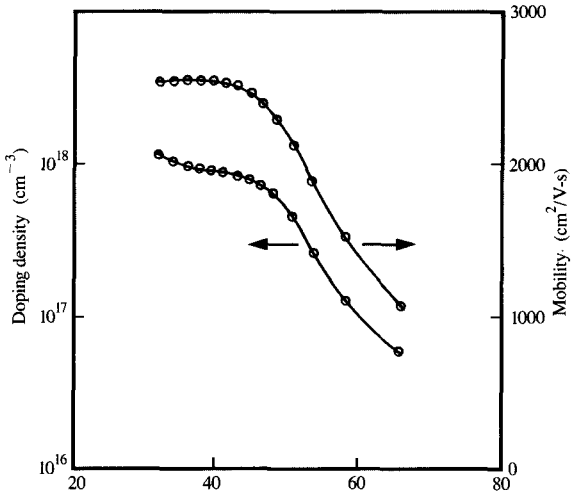


(b)

Figure 2

(a) The dc characteristics of a large-area (100 μm by 75 μm) recessed-gate GaAs MESFET, showing its transconductance and conductance in the linear region (V_D = 0.1 V) and transconductance in the saturated region (V_D = 1 V). (b) Mobility and doping profiles versus the depth of its epitaxial channel.

Q of the capacitance measurement caused by the large leakage current of the Schottky contact to the highly doped channel.

The quality of the Schottky barriers was analyzed in order to understand what parameters influence the barrier height and the ideality of the Schottky contact. Although a large barrier height is desired, it is not sufficient to choose preparation conditions which maximize the measured barrier height [7]. This is because an apparent increased barrier height can easily be caused by an interfacial layer which, while reducing the leakage current of the Schottky gate under forward bias

Table 1 Ideality factor and barrier height for devices on two wafers subjected to different cleaning procedures.

Wafer no.	*Gate length* (μm)	n (I–V)	ϕ (C–V) (eV)
1	1	1.52	0.99
1	20	1.24	0.94
2	1	1.24	—
2	20	1.25	0.78

conditions, also reduces the transconductance of the transistor (because the modulated charge is farther away from the gate metal). Such an interfacial layer also affects the threshold voltage; since it is not deliberately created, it has a variable thickness and composition across the wafer, which leads to variations in threshold voltage, transconductance, and leakage current. Experiments have shown that barrier height, as determined from I–V characteristics, is only weakly dependent on cleaning and deposition procedures. The diode ideality, as determined from the I–V characteristics, is, on the other hand, a good basis for comparing different Schottky diodes.

The ideality factor n characterizes the deviation from the ideal current–voltage behavior of a Schottky diode, and is defined by a fit of the measured current–voltage characteristic to the expression

$$I = I_0(e^{V/nV_T} - 1),$$

where V_T is the thermal voltage. The barrier height ϕ calculated from a C–V measurement [8] is also sensitive to preparation conditions.

As can be seen for one of the two wafers of **Table 1**, the C–V barrier height on wafer 1 was large and size-dependent, and the I–V ideality factor was large. This resulted in transistors with a large pinch-off voltage for the particular channel thickness used, and a relatively low (~250 mS/mm) transconductance. For wafer 2, which contained the same epitaxial layers, the C–V barrier height was distinctly lower and closer to the barrier height measured on more lightly doped layers, and the diode ideality factor was closer to one. (The C–V measurement of the device on wafer 2 having a gate length of 1 μm proved unreliable as measured at 13 MHz because of diode leakage current.) This wafer yielded transistors with distinctly larger transconductances (>400 mS/mm).

While scaling the channel thickness and length, it becomes more difficult to make adequate contacts: A thinner and shorter channel requires more shallow contact regions which cannot be contacted as readily as very deep contact regions. In addition, the current and transconductance of short-gate-length and thin-channel MESFETs increase, so that an even lower contact resistance is required. Therefore, ohmic contacts need to be adapted to the shallow contact regions, which can be achieved by changing the composition and alloy temperature of the Au/Ge/Au/Ni contact [9]. A contact resistance of 0.2 Ω/mm or 1.5×10^{-6} Ω/cm^{-2} for an n^+ sheet resistance of 330 Ω/square is thus obtained. An additional trade-off specific to the recessed-gate MESFET structure is the total layer thickness: A thicker structure reduces the contact resistance and the resistance per square of the region between the ohmic contact and gate. At the same time, it makes it difficult to etch the channel to a specific thickness and increases the self-aligned distance between the gate and n^+ contact layer. A total thickness of 100 nm has proven to be a good compromise. The total contact resistance thus obtained is 0.2 Ω/mm, which, for an intrinsic transconductance of 400 mS/mm, results in an 8% reduction in extrinsic transconductance because of the contact resistance component of parasitic source resistance.

Figure 3(a) shows the I–V characteristics of a 20-μm-wide, 0.5-μm-gate-length enhancement-mode device. No saturation of transconductance occurs. Depletion-mode devices (obtained by a more shallow recess etch) have a saturated transconductance of 540 mS/mm.

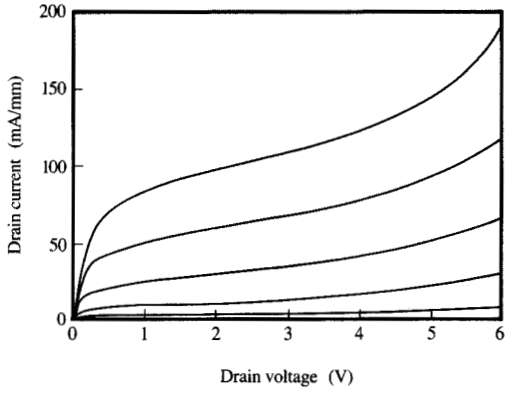
The change in transconductance with gate voltage, or k-factor, is important for logic circuits in which a transistor is driven from a fully off state, by applying a gate voltage lower than the threshold voltage, to a fully on state. This k-factor, which is described in detail in the section on implantation self-aligned devices, reaches a value of 580 mS/V-mm for a drain voltage of 2 V [10]; the k-factor and the maximum transconductance vary slightly with drain voltage due to finite output conductance. The enhancement-mode, recessed-gate MESFETs discussed here also have a very large g_m/g_d ratio (for instance, 33 for $V_G = 0.7$ V and $V_{DS} = 2$ V). This is consistent with their large gate-length to channel-thickness ratio, even at a gate length of 0.5 μm, obtained by use of a very thin (25-nm) channel.

The high-quality pinch-off characteristics of the device of **Figure 3(a)** are shown in **Figure 3(b)**, in which its transconductance and drain current are plotted on a logarithmic scale as a function of its gate voltage for drain voltages of 2 and 4 V. The threshold ideality (defined in the same way as the Schottky diode ideality factor) at a drain voltage of 2 V is 1.24. For gate voltages in the subthreshold region below 0.4 V, transistor characteristics are similar to those of bipolar junction transistors since both its drain current and transconductance vary exponentially with its gate voltage. Its transconductance can be approximated by $g_m = I_D/V_T$. Such devices can be used in this regime for low-power current-mode MESFET logic circuits [11]. The low power is obtained at the expense of speed because of the

low current levels and the thus-increased influence of parasitics.

In Figure 3(a) a tendency can be seen for the device to break down at 6 V even though full pinch-off is maintained, indicating that neither punch-through nor gate-drain breakdown (because of the low gate current at high drain voltage) is responsible for breakdown. Transconductance even increases with drain voltage, reaching a value of 1750 mS/mm at 6.5 V while retaining a transconductance-to-output-conductance ratio larger than 10. This high transconductance has a cut-off frequency of 500 MHz and results from avalanche multiplication of carriers in the high-field region near the drain and parasitic bipolar action [12] due to the injection of holes into the semi-insulating buffer layer; the resulting positive feedback between the two effects eventually causes breakdown within the device. This parasitic bipolar effect does not have an adverse influence on operation in digital circuits with low power-supply voltages (<4 V). Also, microwave applications are unaffected, regardless of operation voltage, because of the low cut-off frequency of this effect.

The parasitic bipolar effect also causes a negative input resistance between source and gate for large drain–source voltages [13] as a result of holes generated by the avalanche multiplication. The holes do not only travel through the buffer layer; some flow to the Schottky contact where they recombine, yielding a negative current for a positive applied voltage. For depletion-mode devices which do not show the increased transconductance due to bipolar action, this effect exists up to their cut-off frequency.



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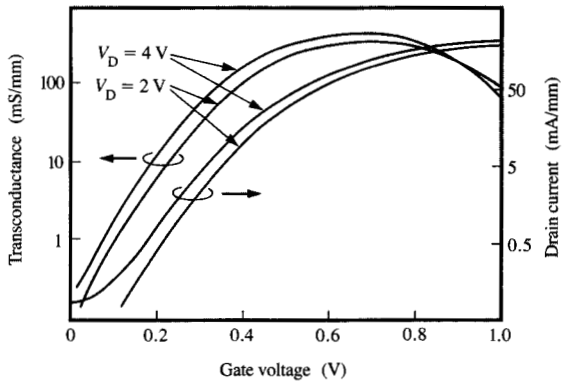


(b)

Figure 3

(a) I–V characteristics of a recessed-gate GaAs MESFET having a gate width of 20 μm and gate length of 0.5 μm; $V_G = 0.3$ V (bottom curve), 0.4 V, 0.5 V, 0.6 V, and 0.7 V (top curve). (b) Its transconductance and drain current versus its gate voltage at $V_D = 2$ V and 4 V.

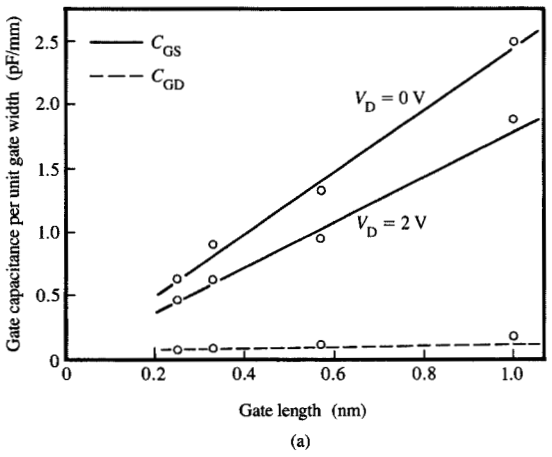
• *High-speed characteristics*

Figure 4(a) shows the gate capacitance C_{GS} per unit gate width, as obtained from s-parameter measurements at 4 GHz, for two different drain voltages and as a function of gate length. Even down to a gate length of 0.25 μm, C_{GS} decreases with decreasing gate length. The Miller capacitance C_{GD}, on the other hand, is almost independent of gate length, so that its relative influence becomes larger as the gate length is reduced. **Figure 4(b)** illustrates the effect of C_{GD} and gate fringe capacitance on the transit frequency f_T of the devices as a function of gate length. Extrinsic transit frequency is obtained directly from s-parameter measurements, whereas intrinsic transit frequency is obtained by subtracting gate fringe capacitance as well as Miller capacitance from measured gate capacitance.

Using such recessed-gate MESFETs, we have fabricated enhancement/depletion logic inverters connected in a ring-oscillator configuration. Such a ring oscillator with 0.33-μm-gate-length and 40-μm-gate-width devices yielded a 16-ps delay per gate and a power consumption of 6 mW per gate. Optoelectronic receivers with bandwidth in excess of 5 GHz were also fabricated on the same wafer. A more complete description of these high-speed circuits can be found in [14].

Self-aligned-gate MESFET

In contrast to the recessed-gate MESFET structure commonly used for microwave applications, a self-aligned-gate MESFET structure is typically used for digital circuit applications. The device design differences for digital GaAs MESFETs with submicron gate lengths arise primarily from the need to operate in a large-circuit environment.



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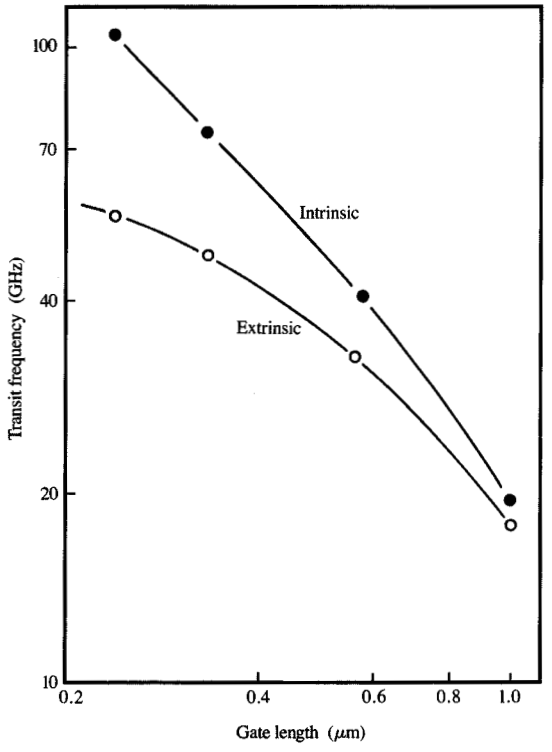

Figure 4

(a) Gate capacitance per unit gate width as a function of gate length for recessed-gate GaAs MESFETs. C_{GS} corresponds to the gate-to-source capacitance and C_{DS} to the drain-to-source capacitance. (b) Transit frequency as a function of gate length.

This has two primary consequences. First, large circuits imply the need for a low operating power per gate. This has led to the use of enhancement/depletion (E/D)-mode logic, with the important consequence that the voltage swing available is severely constrained: The logic high voltage is limited by the forward turn-on characteristics of the gate diode, and the logic low voltage is at best near zero for buffer-type logic and greater than that by a value related to the on-resistance of the drive MESFET for direct-coupled logic. This also means that the digital MESFET need not operate at large drain bias, whereas large drain bias capability is important for microwave devices for large power output. Second, large circuits imply long wires and therefore a large wiring capacitance. For many circuits this wiring capacitance dominates over the intrinsic device and device parasitic capacitances. Thus, the f_T of a device is not in itself a sufficiently accurate predictor of circuit performance, since C_{GS} is not the dominant driven capacitance.

Taken together, these operating requirements indicate the need for a device that can deliver large output current for a small input gate voltage, i.e., one for which the large-signal transconductance should be maximized. For the GaAs MESFET, a square-law approximation is often useful for characterizing device operation in the region from slightly above threshold to the state at which gate diode turn-on becomes significant. While the MESFET is properly a square-law device only for the case of a delta-doped channel, this approximation is surprisingly good for arbitrary channel doping profiles [15]. Thus,

$$I_D = k(V_G - V_T)^2,$$

and maximizing large-signal transconductance is equivalent to maximizing k. Since by differentiating twice with respect to V_G

$$k = \frac{1}{2}\frac{\partial g_m}{\partial V_G},$$

this is the same as maximizing the rate of turn-on of the small-signal transconductance of the device.

It is important to note that for large-scale digital applications, circuit speed can be increased by increasing k even if the f_T of the discrete MESFET remains unchanged. Again, this is because the driven capacitance of interest is not C_{GS} but an effective capacitance represented by perhaps several downstream gates and the wiring required to reach them. Since this total capacitance can far exceed the sum of all input C_{GS} terms, it is possible to increase circuit speed by increasing k even if the f_T of the discrete device is reduced. Intrinsic device speed is not enough; to maximize digital performance the MESFET should be optimized to use its speed to rapidly deliver as large a current as possible to the circuit in which it is embedded.

There are three obvious areas to be optimized in order to maximize the current drive capability of the GaAs

MESFET. First, the amount of controlled charge should be maximized. Second, parasitic feedback resistances should be minimized. Third, gate length should be minimized.

Since the charge-confinement barrier is fixed for a GaAs MESFET by the metal–semiconductor Schottky barrier height (and commonly by the mid-gap Fermi-level pinning position of GaAs), the only easily variable parameters to consider in order to maximize the controlled charge are the channel thickness and doping.

For a uniformly doped channel, the amount of controlled charge for the case of zero source-to-drain potential is

$$Q_c = N_d \Delta w = N_d \sqrt{\frac{2\varepsilon_s \Delta V}{qN_d}},$$

where Δw is the variation in channel gate depletion width and ΔV is the variation in gate potential that produced it. Q_c is maximized by maximizing the channel doping concentration N_D. For an enhancement-model MESFET this also means that the channel thickness is small, since the heavily doped channel must be fully depleted by the gate barrier. For a MESFET under normal biasing conditions, Q_c varies from the value given above, and increased channel doping is achieved at cost of channel mobility; nonetheless, thin, heavily doped channels are useful for maximizing the controlled charge. Channel doping cannot be increased without limit, however (even if this were technologically feasible). As the doping is increased, the gate barrier thickness is decreased (as desired), and tunneling current from the gate to the channel becomes a problem. Of course, the assumption of uniform channel doping is not necessary; the near surface doping can be reduced or eliminated to reduce the tunneling current due to the local fields from ionized impurities [16]. It is even possible to increase the gate barrier height by introducing a thin layer of a material with a larger gate barrier (e.g., AlGaAs) in the near-surface region.

The requirement that parasitic feedback resistances be minimized leads to the use of a self-aligned MESFET structure. As shown in **Figure 5**, heavily doped regions are butted directly up against the gate region. There are several techniques that can be used to produce such a structure. The two most commonly used are one in which a refractory gate is used as the mask for an ion implantation that produces the heavily doped regions [17], and one in which a temporary gate is used as the implantation mask and is subsequently replaced at a later point in the process with a permanent gate [18]. Of these two, the refractory gate process is simpler and provides better accuracy and reproducibility of the implantation positioning. This is achieved at the cost of significant material constraints, since the refractory gate must

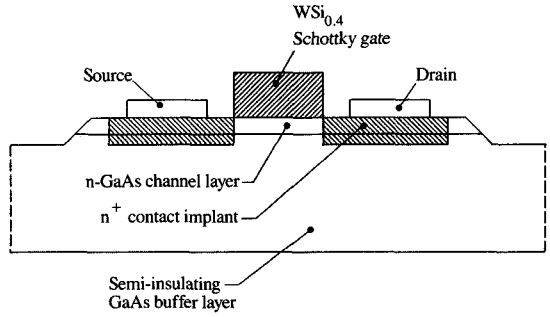

Figure 5

Self-aligned GaAs MESFET cross section.

survive the ion-implantation annealing that activates the heavily doped self-aligning implantation regions without significant interaction with the MESFET channel.

Reducing the gate length for digital MESFETs is, of course, similar to reducing it for microwave MESFETs. However, the control of short-channel effects is perhaps more important, since low output conductance is required not only to provide devices with large gain (as in microwave MESFETs) but also to produce circuits with acceptable operating margins. A rough requirement is that the ratio of maximum transconductance to output conductance be greater than 15 ($g_m/g_d > 15$). This is a particularly severe requirement for a self-aligned MESFET, since the n^+ regions which are self-aligned with the gate are produced by ion implantation, and implantation straggle effects or dopant lateral movement during the implantation–activation–annealing can cause strong short-channel effects. It is even possible to produce MESFETs with no intentional channel doping if the n^+ movement is sufficient and the gate length is sufficiently short [2]. Even in the absence of implantation straggle or dopant movement and with device doping as in Figure 5 (perfect alignment to gate, abrupt doping concentration change), short-channel effects can be severe because of carrier tailing and two-dimensional effects. These can be minimized by minimizing the depth of the n^+ region; however, this is difficult to achieve because it requires the formation of very shallow implanted layers with low sheet resistance.

- *Fabrication*

With the above criteria in mind, self-aligned refractory-gate GaAs MESFETs were fabricated with a large *k*-factor as the design goal—that is, MESFETs having thin, heavily doped channels and short gate lengths. Since a thin-channel structure is a prerequisite for short-gate-

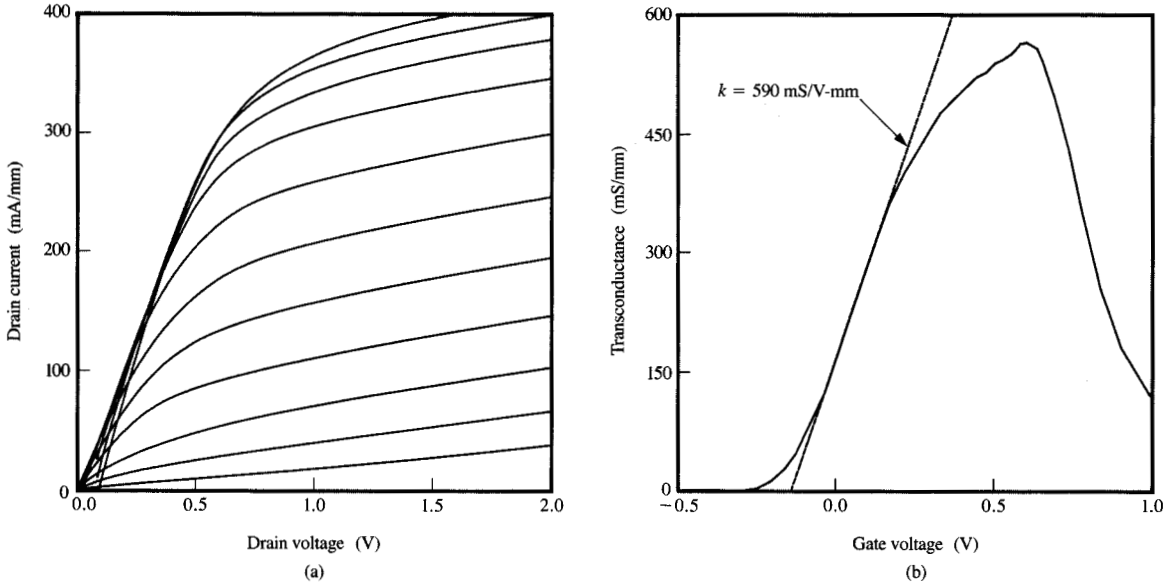

Figure 6

(a) The dc characteristics of a GaAs MESFET having an epitaxial channel and a refractory self-aligned gate 0.8 μm in width. The characteristics are shown at gate voltages of 0.0–1.0 V (at 0.1-V steps). (b) Its transconductance versus its gate voltage. From [2], reproduced with permission; © 1987 IEEE.

length devices if short-channel effects are to be well controlled, the fabrication of devices with thin, heavily doped channels was studied first.

Although thin channels can be formed by ion implantation, the use of epitaxial growth permits the formation of thinner channels with greater doping flexibility. Consequently, MOVPE (metal–organic vapor-phase epitaxy) was used to grow the channels for the devices described in this section. For simplicity, uniform channel doping was used. For the first devices studied, a channel layer 50 nm thick doped with Si at a level of $1.2 \times 10^{18}/\text{cm}^3$ was grown on an undoped buffer layer, on a semi-insulating GaAs wafer. After growth, mesa etching was used to provide isolation between devices. After mesa etching, a 250-nm-thick layer of $WSi_{0.4}$ was deposited by sputtering and patterned into gates by optical lithography and reactive ion etching. After patterning, the $WSi_{0.4}$ gates were used as a mask for a 60-kV, $5 \times 10^{13}/\text{cm}^2$, $^{29}Si^+$ implantation. Following implantation, the wafer was annealed at 900°C for 30 seconds, and Au/Ge-based source and drain contacts were deposited and alloyed to complete the devices.

Figure 6 shows the dc characteristics for a device fabricated as described, having a gate length of 0.8 μm. Its k-factor was 590 mS/V-mm—very large for a device with a 0.8-μm gate length. The maximum value of the transconductance g_m was also large, >500 mS/mm. These results confirm that a thin, heavily doped channel is effective in producing high-performance MESFETs.

Although the device structure described above provides good performance at long gate lengths (>0.5 μm), it is not directly applicable to short gate lengths. In fact, for devices fabricated as described above, the k-factor decreases for gate lengths <0.5 μm as short-channel effects begin to dominate device performance. This is because the self-aligning step is not well chosen for short-gate-length devices. For gate lengths <0.5 μm, the self-aligning step becomes perhaps the most critical in the fabrication of refractory-gate, self-aligned MESFETs. Essentially, as gate length is reduced, the heavily doped n^+ self-aligning region must be made thinner in order to keep short-channel effects under control. It is a simple matter to reduce the ion-implantation energy to provide a shallower self-aligning implantation layer, but it is not simple to maintain the low sheet resistance necessary for this layer to allow the performance of the intrinsic MESFET to be largely realized at the device terminals. Also, although bulk diffusion of the usual n-type implantation species (e.g., Si or Se) is low at annealing temperatures of interest, stress-driven diffusion effects

(from gate metal or implantation cap stress, or thermal expansion mismatch stress) can be important for short-gate-length devices [19]. This can be a significant problem even if so-called "lightly doped drain (LDD)" structures are used to minimize the sheet resistance requirements for the self-aligning implantation.

To improve our ability to fabricate devices with short gate lengths and shallow self-aligning ion implantations, an arsine ambient rapid thermal annealing system was constructed [19]. This provided the advantages of rapid thermal annealing (RTA) for these devices (reduced self-aligning implantation movement and reduced gate-channel interaction) while avoiding the difficulties of capped RTA (decapping problems, cap thermal mismatch-driven dopant movement) and the uncertain As loss characteristics of uncapped or proximity RTA [20]. Although the arsine ambient RTA system was used to fabricate the devices described above, the self-aligning implantation chosen was not sufficiently shallow for short-gate-length devices. By optimizing annealing conditions, ion implantations of $5 \times 10^{13}/cm^2$, 15-kV, $^{29}Si^+$ with sheet resistances as low as 300 Ω/square were achieved.

Using the arsine ambient RTA, short-gate-length devices with thin, heavily doped channels and shallow self-aligning implantations were fabricated. MOVPE was used to grow a 30-nm-thick channel layer doped with Si to a level of $1.7 \times 10^{18}/cm^3$ on a 250-nm-thick undoped buffer layer on a semi-insulating GaAs wafer. Mesa etching was used to provide device isolation for the epitaxial-channel enhancement-mode devices. After mesa etching, selective ion implantation ($^{29}Si^+$, 30-kV, $8 \times 10^{12}/cm^2$ + $^{24}Mg^+$, 50-kV, $2 \times 10^{12}/cm^2$) was used to form implanted-channel depletion-mode devices. Next, a 250-nm-thick layer of $WSi_{0.4}$ was deposited by sputtering and patterned by electron-beam lithography and reactive ion etching. After patterning, the $WSi_{0.4}$ gates were used as a mask for a 15-kV, $5 \times 10^{13}/cm^2$, $^{29}Si^+$ self-aligning implantation which was activated by a 900°C, 30-s annealing step without a cap in the arsine ambient RTA system. After the self-aligning implantation annealing, Au/Ge-based ohmic contacts were deposited and alloyed. An SEM micrograph of a completed device having a gate length of 0.15 μm is shown in **Figure 7**.

Figure 8 shows the dc characteristics for such a device. The *k*-factor for this device was larger than 800 mS/V-mm, and its maximum transconductance was larger than 500 mS/mm. This *k*-factor is significantly larger than that reported for any previous MESFET. An important point is that short-channel effects were well controlled, with g_m/g_d ratio > 20 for the device despite the extremely short gate length. For devices having a gate length of 0.25 μm, *k*-factors were greater than 700 mS/V-mm and g_m/g_d ratios were greater than 30.

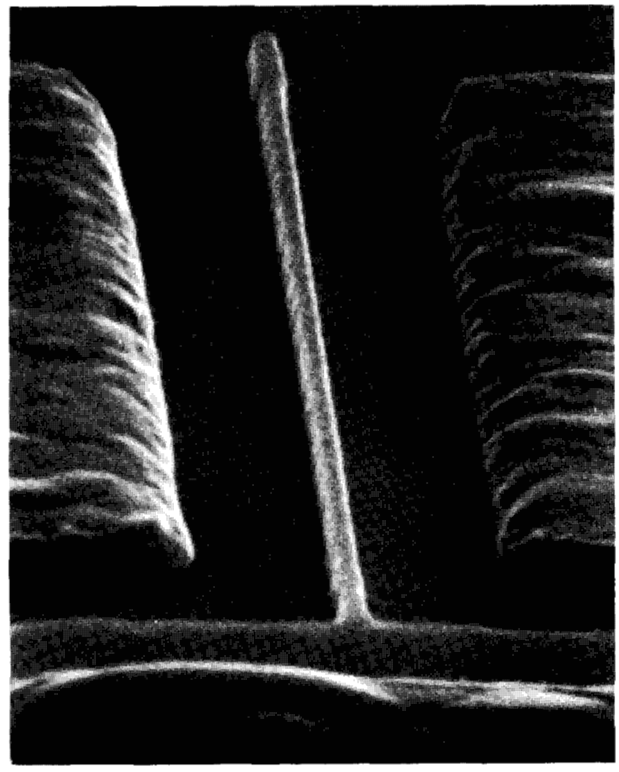

Figure 7

SEM micrograph of a GaAs MESFET having an epitaxial channel and a refractory self-aligned gate, 0.15 μm in width.

Simple circuits (inverters and ring oscillators) were fabricated using these devices. Propagation delays as small as 17 pS/stage were measured for unloaded ring oscillators fabricated with devices having a gate length of 0.25 μm at a power consumption of 2 mW/gate; a delay of less than 20 pS/stage was measured at 1 mW/gate. For both power levels, the delay was limited by the gate resistance of the nonoptimized 20-μm-gate-width devices.

Concluding remarks

We have demonstrated with two different device structures, by scaling channel thickness and doping, that the performance of GaAs MESFETs having submicron gate lengths is not limited by short-channel effects. High performance capability was demonstrated for devices having different gate lengths by measurements of transconductance, *k*-factor, and transit frequency. Results on ring oscillators confirmed the applicability of the devices to high-speed logic circuits. These results indicate that present-day (logic, analog, and microwave) circuits with devices having 1–0.5-μm gate lengths should be extendable to significantly higher speeds through the use of devices with gate lengths less than 0.5 μm.

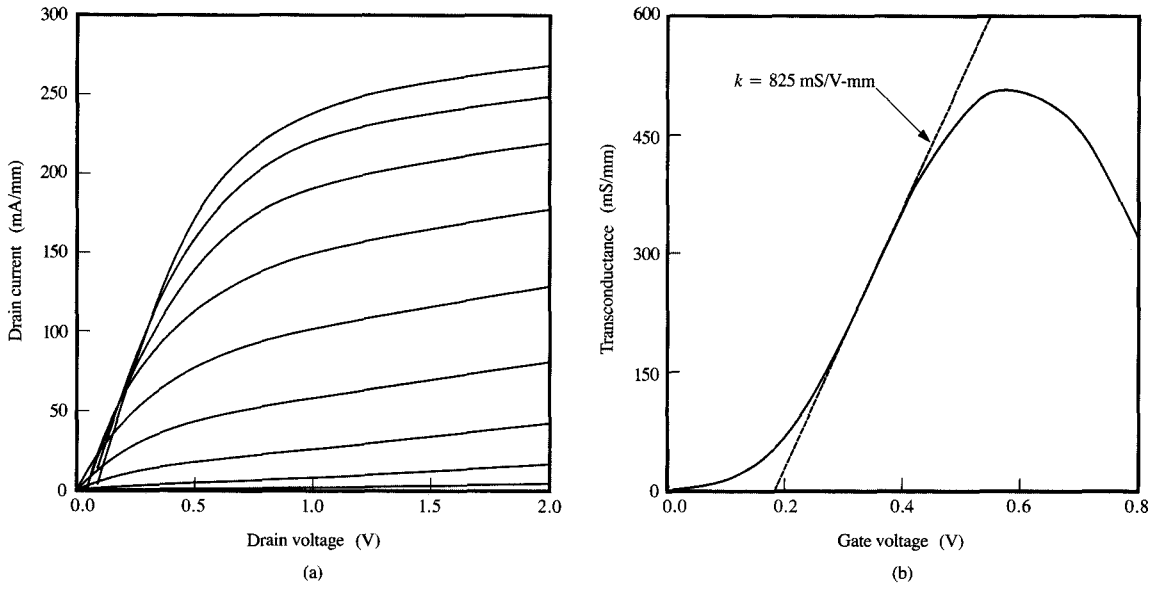

Figure 8

(a) The dc characteristics of device of Figure 7 at gate voltages of 0.2–1.0 V (at 0.1-V steps). (b) Its transconductance versus gate voltage.

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