

LAN interface chip and mixed-signal testing developments

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This paper describes the local area network (LAN) semiconductor chip, from early development through volume manufacturing production, highlighting the testing achievements associated with its qualification and release to production. The paper is divided into two sections dealing with laboratory development and production in manufacturing. The development section describes the importance of partitioning via latch-based boundaries, and how it reduced development cycle time by allowing independent debug and diagnostic tests. The development of tests to characterize the phase-lock loop (PLL) at application conditions and the evolution of these tests into efficient production test vehicles are discussed. Techniques are described that provide new approaches to analog testing, focusing on adapting a production digital tester to meet the characterization and production requirements of a very sensitive PLL/receiver/

transmitter analog design. The manufacturing discussion is centered around three areas, wafer testing, yield learning, and reliability. Unique concepts in each area are presented, along with detailed descriptions of specific applications.

Introduction

The unprecedented acceleration of new advances in silicon technology and integration has caused the amalgamation of previously incompatible technology and circuitry onto a single chip in mixed-signal (analog/digital) devices. The proliferation of small, mixed-signal chips began in the consumer electronics industry, soon spread to telecommunications, and is now very prevalent in the information processing industry. The test skills required are as diverse as the technologies; the breadth of the analog/digital technology touches all aspects from design through simulation, test data supply, automatic test equipment (ATE), and the manufacturing test floor. Anomalies exist in certain areas as the two different disciplines merge [1].

The local area network (LAN) chip represents a successful attempt to integrate six diverse chips and functions onto a single 8-mm-square silicon chip [2]. The functional content of the chip is summarized below:

- A new technology—1- μ m analog CMOS (ACMOS).
- A total of 40 000 circuits.

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- 187-ns, 16-bit custom microprocessor.
- 25 000 circuits of standard cell logic.
 - Controller.
 - Handlers.
 - Protocol interfaces.
 - Four embedded random-access memories (RAMs).
- Parallel digital communications to the user.
- 4/16-Mbps serial Manchester-encoded data communications to the token ring.
- A precision analog PLL/receiver/transmitter.

This chip was the harbinger of a new era in test engineering in which previously segregated skills— analog/digital and logic/memory—were forced to merge.

In the past, silicon products were easily distinguished and divided into specials (analog), logic (custom, standard cell, and gate array), and memory categories. Until recently, the analog chips remained a separate, unrelated niche. However, the competitive pressure to provide higher function/cost ratios in all product offerings forced semiconductor chip manufacturers to exploit an adaptable CMOS technology, thus driving the silicon integration to the point where the function of a card is now available on a chip. Hence, the analog chip and function have formed a mixed marriage with the digital chip. The far-reaching implications of the test requirements generated by this advance in silicon fabrication require real-time innovative responses and long-term solutions, from simulation techniques to ATE (automated test equipment).

The LAN demands placed upon the ATE initially seemed unwieldy, and were compounded as the myriad of specifications, volumes, schedules, and costs emerged and were identified. Costs and schedules required stringent coordination between laboratory characterization testing and manufacturing volume production testing at every step. A characterization test was not developed if it could not become a cost-effective production test with minimal modification.

Chip design

The amalgam of functions and the precise communication networking and protocols forced intense integration in design and complicated interdependent timings on the chip. The LAN chip provides a number of complex functions implemented through three distinct chip sections (see **Figure 1**). The sections are physically recognizable as a 16-bit microprocessor, the analog front-end macro (FEM) [3], and 25 000 gates of CMOS standard cell (CSC) logic. The CSC logic provides the circuitry for the protocol data handler, shared memory controller, interrupt controller, embedded RAMs, and clock timing generator. Both the CSC logic and microprocessor are level-sensitive scan designs (LSSD),

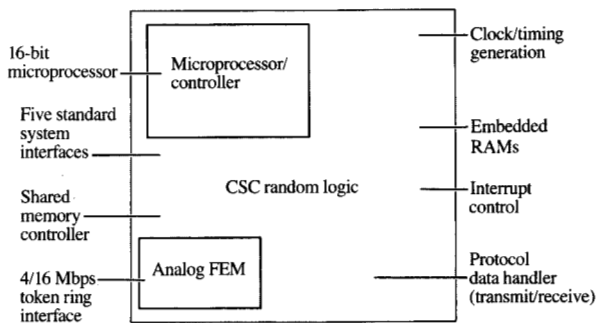


Figure 1

High-level diagram of LAN chip function.

with separate clocking for each [2]. Each of the three major subdivisions was designed to be physically and logically partitioned from the adjacent sections for testing purposes. The partitioning, controlled through stimulus supplied via the tester to the mode pins (see **Tables 1** and **2**) and latch boundaries (**Figure 2**), proved invaluable by allowing each chip section to be debugged independently of the others. Because the microprocessor, standard cell logic, and analog front end were not dependent upon successful mutual debugging, the debug cycle was shortened and diagnostics were made more efficient.

The physical and logical separation of the two digital sections allowed test patterns for each to be generated by the respective designers.

The partitioning of the analog FEM was more complex than the separation of the two digital sections. To provide the necessary isolation between analog and digital, an L1-L2 shift register latch (SRL) boundary was initially intended (**Figure 2**); however, latch-based multiplexors were found to provide the best solution.

The multiplexors were designed such that in actual application the boundary is essentially transparent. Delays due to data passing through the devices with the multiplexor were unavoidable, but were kept to a minimum and therefore did not affect performance. In addition, placing the FEM in a corner of the chip allowed accessibility via external input/output devices, which, in conjunction with the inherent controllability of clocked data in latch-based designs, provided the necessary testability/observability of the entire FEM function. Because the digital chip sections (microprocessor and CSC logic) were LSSD designs, it was necessary that the

Table 1 LSSD clocks and control.

<i>Pin function</i>	<i>Description</i>	<i>Active state</i>
A clock	CSC logic	Low
B clock	LSSD clocks	High
C clock		High
Ram clock		High
Scan gate		Low
Mode 0	See Table 2	Depends on mode
Mode 1		
Mode 2		
A clock	Processor	High
B clock	LSSD clocks	High
C1 clock		High
C2 clock		High
P clock		High

Table 2 Functional and test modes.

<i>Mode 0</i>	<i>Mode 1</i>	<i>Mode 2</i>	<i>Description</i>
High	High	High	Normal/Internal FEM
High	High	Low	Normal/External FEM
High	Low	High	Internal FEM isolate
High	Low	Low	Microprocessor isolate
Low	High	High	PROST* boundary scan
Low	High	Low	PROST auto load
Low	Low	High	PROST auto test
Low	Low	Low	Standard LSSD test

* PROST = Pseudorandom On-Chip Self-Test

clocks for the digital and analog remain isolated from one another. Otherwise, the testing of the digital sections would force a constant bombardment of the analog circuitry with spurious data clocked in from the inactive isolation circuitry.

To allow a cursory check of the analog function, a wrap function was designed into the FEM as a card/box diagnostic tool. This feature also provided a wafer screen for gross errors in the FEM. A detailed explanation is provided in the Manufacturing section.

Development

• Recognizable challenges

As in every development effort, the focus was on meeting the schedules. However, the normal manufacturing "ramp-up" had been replaced with a step function in production shipments immediately following product qualification. This fact dictated a set of unique issues requiring manufacturing impact evaluations during each step of the development cycle. The tests developed had to

generate detailed and consistent characterization data for qualification, and also offer a cost-effective production test vehicle with minimal modification. It was unsatisfactory to expend resources developing a test that demonstrated specification conformation, if that test was not cost-effective in production.

Test equipment limitations compounded the problem. In today's electronic industry, a variety of applications require mixed-signal circuit designs in order to be competitive in price and performance. However, the large data volumes and I/O associated with the microprocessor and CSC logic exceeded the specs of existing mixed-signal ATE. Modification of mixed-signal ATE to accommodate data volumes and I/O was cost-prohibitive, the manufacturing test systems had no analog capability, and production costs precluded a dual-pass test approach. Considering all aspects of the situation, analog adaptations on a digital manufacturing system constituted the best mix of feasibility, affordability, and expediency.

Digital

As mentioned previously in the discussion of the importance of design for testability, the partitioning of the digital section allowed parallel and independent debug of the microprocessor and CSC logic. The design of the partitioning offered great development flexibility and, in addition, incorporated foresight that included a mode/clocking combination. This combination provided the means to programmably configure the chip such that a composite pattern set could test both digital partitions as one logic block, thus enhancing the manufacturing efficiency. The flexibility of development/characterization details and cost-effective manufacturing was realized through real-time control of the inputs to the decode circuitry for mode selection.

Analog

The most formidable technical challenge to test engineering centered around the analog FEM. On an existing digital tester, using a single-pass approach, tests had to be devised to characterize the phase-lock-loop-based FEM under application conditions and provide a path to develop these tests into efficient test production equipment [4].

Analog FEM

For an overview of test methods used, the analog FEM functions are outlined below and illustrated in Figure 3 [5].

• Phantom drivers

- Ring insertion/extraction by current-selecting relay.
- Controlled by software via the microprocessor.

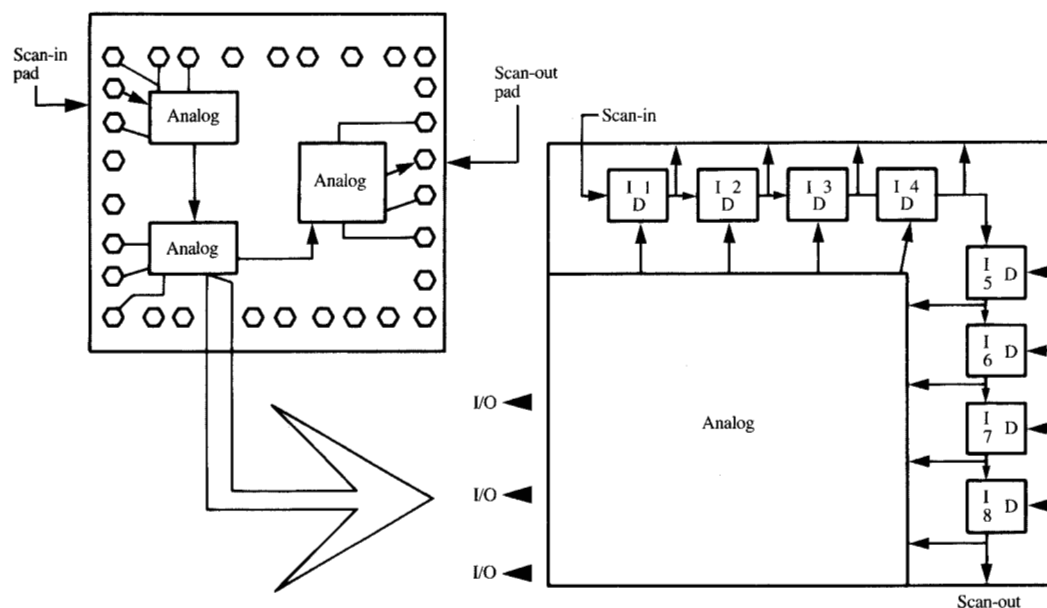


Figure 2

Analog partitioning via latch boundaries.

- Wire-fault circuits
 - Monitor ring for opens, shorts, or power supply failure.
 - Removed from ring automatically upon fault detection.
- Transmitter
 - Transmits Manchester-encoded data onto ring.
 - Receives serial data through protocol handler.
- Receiver/threshold
 - Receives Manchester-encoded data from ring.
 - Digital waveform reshaping.
- Phase-lock loop (PLL)
 - Uses voltage-controlled oscillator (VCO).
 - Derives system clocks from incoming serial data.

• *Early FEM testing*

Early test methods employed on the analog FEM consisted of basic current, voltage, and frequency measurement techniques implemented using a TR3340 Advantest VLSI tester. These techniques were adequate to guarantee static analog FEM functions of the phantom drivers, wire-fault circuits, and transmitter asymmetry. The precision, Manchester-driven PLL required significant characterization and test development.

Given the steepness of the manufacturing ramp up in support of the general announcement of the 16-Mbps LAN, and the analog circuitry's intolerance of process variations due to the critical dependence upon matched transistors, engineering test lots were processed under engineering control to simulate process variation effects and thereby anticipate manufacturing problems. Fluctuating yields on these first experimental lots showed conclusively that the PLL was very sensitive to process variations that could conceivably occur in manufacturing (see **Figure 4**).

On the basis of the initial data, it was decided to process a significant number of test lots, which would simulate the limits of allowable process variations in channel length, mobile charge contamination, voltage threshold (V_t) shifts, and a number of other anomalies possible in volume production.

Phase 1: Voltage-controlled oscillator (VCO) gain

The first test developed, VCO gain, utilized a force frequency/measure voltage method. Voltages were measured at FILTB that corresponded to FEXTAL input signals of 8.5 MHz and 7.5 MHz in the frequency acquisition mode of the PLL (see **Figure 3** and **Figure 5**).

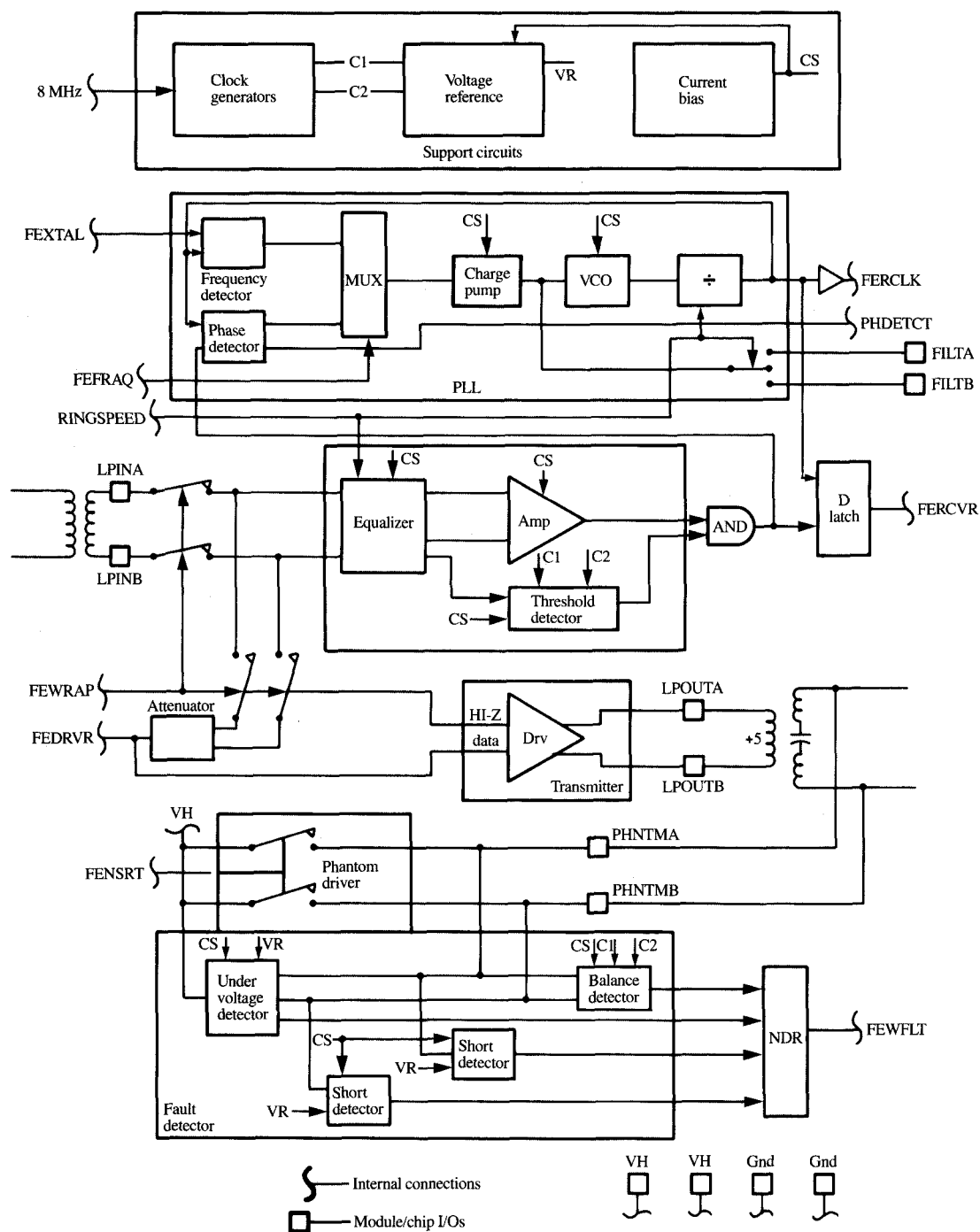


Figure 3

Detailed block diagram of analog FEM. Note that internal connection points are accessible through CMOS standard cell off-chip drivers and receivers. Terms: FEXTAL = Crystal (oscillator) input to PLL; FEFRAQ = Multiplexor selector (acquisition or phase-lock); RINGSPEED = Filter and divide-by (2 or 8) selector; FILTERA/B = Connection to 16-MHz or 4-MHz external filters.

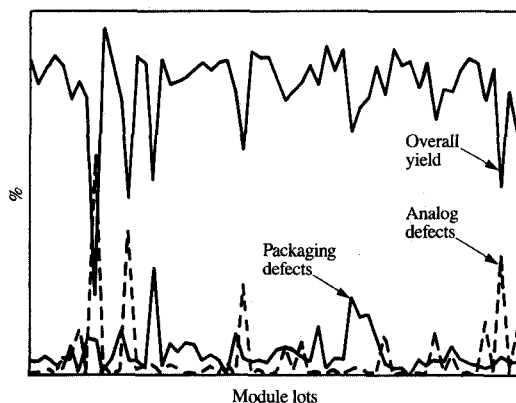


Figure 4

Early development test prototype lots. Note that these lots represent numerous process anomalies produced under engineering control. For clarity, the full spectrum of detractors is omitted.

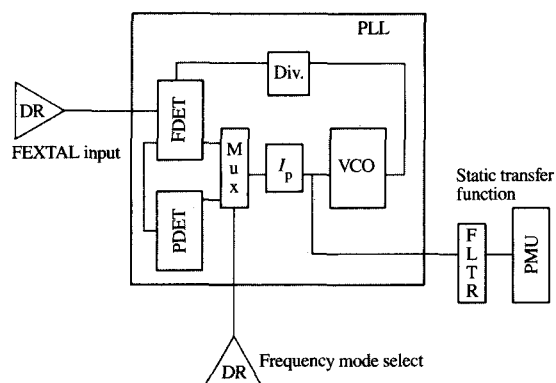


Figure 5

Block diagram of FEM and ATE used in the static gain test. Terms: FEXTAL = Crystal (oscillator) input to PLL; FDET = Frequency detector; PDET = Phase detector; I_p = Charge pump current; PMU = Parametric measuring unit; Div. = Divide-by.

The slope of the line VCO vs. frequency V_o was then calculated and compared against test limits for conformance to pass/fail criteria (Figure 6). The gain (V_o) alone, however, proved to be an incomplete determination of VCO gain characteristics. With extremes in the voltage and frequency response of the VCO's transfer function unknown, many hours were spent in detailed characterization, analysis, and test development [6]. The data revealed that to maximize yield and reliability, key characteristics had to be measured, and test stimuli and limits calculated individually by chip. Each chip required unique, process-dependent test conditions.

To understand the transfer function of each chip, several characteristics had to be measured [7]. The key parameters were the charge pump current (I_p) and gain (V_o). These two values were stored in real time and used in mathematical formulas to derive the F_{min} and F_{max} frequency endpoints. The slopes of the transfer function M_1 [F_{max} to $F(8.5)$] and M_2 [$F(7.5)$ to F_{min}] (where $F(8.5)$ and $F(7.5)$ are test frequencies of 8.5 and 7.5 MHz on this curve) were used to determine the roll-off at these extremes. To ensure that the VCO met the slope specifications at nominal, maximum, and minimum frequencies, slopes V_o , M_1 , and M_2 were calculated and compared against the specifications. (See the detailed test methodology explanation below.)

This test technique, which calculates test stimuli and pass/fail criteria by chip, proved crucial in guaranteeing

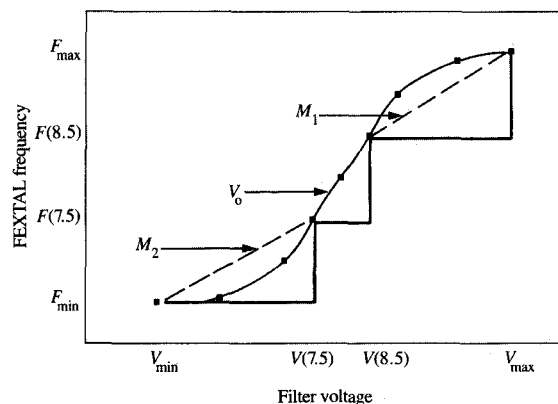


Figure 6

VCO static transfer curve.

LAN performance and reliability. The subject of performance-testing the PLL is discussed fully in the Manufacturing section of the paper under the Reliability subheading.

Static VCO gain test methodology

Please refer to the detailed block diagram in Figure 3

when reading this section; we define the terms introduced there as follows:

- FEXTAL = Crystal (oscillator) input to PLL.
 FEFRAQ = Multiplexor selector (acquisition or phase-lock).
 RINGSPEED = Filter and divide-by (2 or 8) selector.
 FILTA/B = Connection to 16-MHz or 4-MHz external filters.

The critical measurements are done on the points FILTA and FILTB (4 Mbps and 16 Mbps). These filters comprise a simple parallel R - C network in series with a second capacitor to ground. The value R_1 of the resistor determines the time domain response characteristics of the VCO voltage to the charge pump stimulus. Given the feedback information, the filter will charge or discharge via the current from the charge pump. (Static transfer characteristics of the VCO are shown in Figure 6.)

The test technique developed is as follows:

1. Force FEXTAL with a frequency equal to 1.1 times the nominal frequency of the PLL (i.e., FILTA/B with FEXTAL = 8.0 MHz).
2. Measure the voltage at FILTA/B [= $V(1.1)$, the voltage at 1.1 MHz].
3. Repeat steps 1 and 2 using a frequency equal to 0.9 times the nominal frequency [= $V(0.9)$, the voltage at 0.9 MHz].
4. The slope of the static transfer curve around the nominal frequency (= V_o) is calculated as follows:

$$V_o = \frac{F(1.1) - F(0.9)}{V(1.1) - V(0.9)}.$$

5. Measure the charge pump current (= I_p) at FILTA/B.
6. Calculate $F_{\max}$ and $F_{\min}$ for the chip under test as follows:

$$F_{\max} = F_{\text{nom}}(1.02) + \frac{I_p(R_1)}{V_o},$$

$$F_{\min} = F_{\text{nom}}(0.98) - \frac{I_p(R_1)}{V_o}.$$

7. $V_{\max}$ test
 - Force $F_{\max}$ at FEXTAL.
 - Measure $V_{\max}$ at FILTB.
8. $V_{\min}$ test
 - Force $F_{\min}$ at FEXTAL.
 - Measure $V_{\min}$ at FILTB.
- 9., 10. 16-Mbps test (optional—4-Mbps ring speed is adequate).
 - Repeat steps 5–8 using FILTA and a 32-MHz signal at FEXTAL.
11. Calculate the upper slope (M_1) and the lower slope (M_2):

$$M_1 = \frac{F_{\max} - F(1.1)}{V_{\max} - V(1.1)},$$

$$M_2 = \frac{F(0.9) - F_{\min}}{V(0.9) - V_{\min}}.$$

12. The pass/fail criterion is such that the slope of the roll-off is within 25% of the nominal transfer characteristic

$$0.75V_o < M_1 \text{ or } M_2 < 1.25V_o.$$

Phase 2: ac functional jitter

Although developments in the gain test method ensured the fundamental transfer characteristics of the VCO, it was clear that this test alone was necessary but not sufficient to meet the highest standards in quality, reliability, and performance necessary in the future. Minor perturbations in the transfer curve could be missed, causing subtle functional inconsistencies in the field that would not affect LAN operations in applications meeting the initial system specifications, but whose sum could cause intermittent faults in foreseeable future applications of the token ring. The need to guarantee that these inconsistencies were screened from the sample and functional integrity upheld was pursued. A functional test of the PLL was considered to be the best solution if it could be implemented on the digital ATE in manufacturing [8]. Intensive engineering experiments were performed to determine whether the functional voltage and timing requirements of the PLL could be met with the TR3340 Advantest test system.

The first major obstacle was introducing a 70-mV Manchester-encoded data pattern at 4-Mbps and 16-Mbps data rates. By using a resistor divider network feeding an isolation transformer from a tester channel, a differential signal was input at LPINA and LPINB (see Figure 7). This hardware design implemented on the device interface board (DIB) in a digital tester environment provided the noise-free, low-amplitude, high-frequency stimulus required. A reliable analog port through the digital noise environment was established.

The second technical hurdle to overcome was to synchronize the PLL with tester cycles and monitor cycle by cycle the differential 70-mV Manchester-coded input data on the products' output. The ability of the test system to set up window strobes across one cycle boundary and generate algorithmic patterns (ALPG option), and the high-performance design of the PLL made this possible.

To establish the necessary windows for jitter monitoring, the leading and trailing edge delays must be precisely and individually determined for each chip. Because the CPU in the tester is asynchronous with the PLL, the iterative procedure of moving tester detector

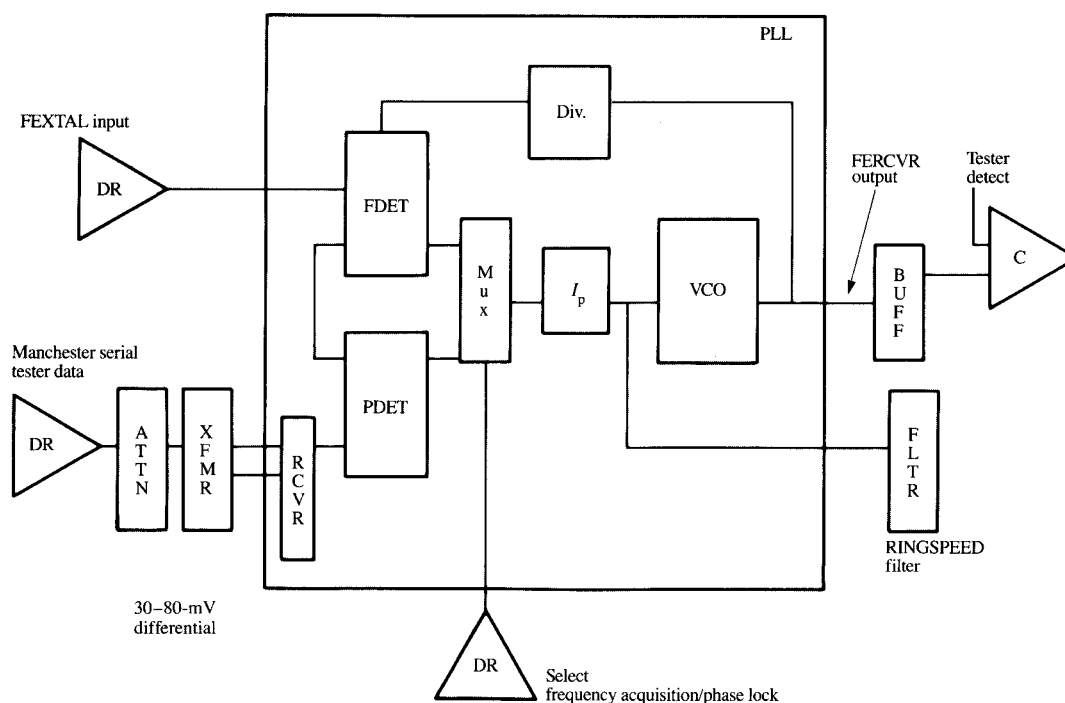


Figure 7

Block diagram of FEM and ATE used in the functional jitter test. Terms: FEXTAL = Crystal (oscillator) input to PLL; RINGSPEED = Filter and divide-by (2 or 8) selector; FDET = Frequency detector; PDET = Phase detector; ATTN = Attenuator; XFMR = Transformer; I_p = Charge pump current; Div. = Divide-by.

strokes to make delay measurements requires re-establishing the VCO phase lock on every iteration. The error strobe position is calculated per device from a Manchester-coded all-zero data delay measurement taken at a nominal V_{dd} voltage. A tester algorithm adjusts for the on-chip delay skews between the start and stop pulses. (Note that most test system timing and front-end errors are nulled simultaneously, leaving only an ATE timing jitter error [9].)

After establishing the rising and falling edges of the Manchester zero data in the time domain, a complete set of Manchester data patterns are applied. With allowance for a jitter specification, the window strobe is placed between a rising and falling edge of the Manchester code when the PLL is locked. The error strobe position (in ns) represents the allowable degrees of product (interface) jitter when the PLL is locked on the 70-mV Manchester

serial data pattern. Any sampled data-out point that has a transition occurring during the (window) error strobe will therefore exceed the allowable jitter specification and fail functionally. Failing patterns are stored for additional off-line characterization (i.e., pattern and voltage sensitivities) (see **Figure 8**). A number of functional test application codes consisting of numerous Manchester one/zero data combinations (**Table 3**) and start/stop delimiters are applied in addition to full application range V_{dd} and input receiver amplitude variation in the 30-80-mV range (which simulates cable length and transmission line mismatch allowances).

Functional patterns are run at both 4- and 16-Mbps data rates. (Serial data clocks at 8 and 32 MHz simulate 4- and 16-Mbps application specifications.) Acquisition time delays (frequency acquisition mode) precede functional test patterns (phase detect mode), thereby

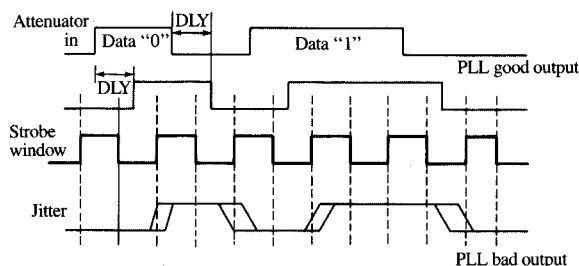


Figure 8

Time domain illustration of jitter test waveforms.

Table 3 Timing definitions.

Description	4 Mbps	16 Mbps
360 degrees	125 ns	31.25 ns
1 degree*	347 ps	87 ps
Clock rate	8 MHz	32 MHz
All 0s	4 MHz	16 MHz
All 1s	2 MHz	8 MHz

* Degrees of phase (radians)

combining previously measured PLL parameters and ensuring acquisition and phase-lock time delay specifications.

Manufacturing

• Wafer test

The low signal amplitude and high frequencies required in the jitter test could not be reliably applied because of the noise environment of the wafer station. Repetitive testing revealed very inconsistent yield information due to the parasitic effects on signals in the wafer station. The jitter test was too sensitive to be reliably applied during wafer test. Potential cost impacts forced data analysis to quantify the percent defective sent to module build resulting from the forced removal of the jitter test from wafer application.

The static nature of the VCO gain test had sufficient noise margin for application in a wafer station. The stimulus waveforms and measured voltages were minimally affected by the wafer environment, and the test required no modifications for wafer application. In addition to the gain test, the wrap function, initially designed for card/box diagnostic purposes, provided an excellent screen for the transmitter, receiver, and PLL sections of the FEM.

The wrap test attenuates a high-level signal supplied to FEDRVR, feeding it back to the receiver equalizer (interface) which drives the phase detector of the PLL through an operational amplifier. The wrap function is completed by setting the D latch from the PLL and measuring the output at FERCVR. This procedure is an excellent stand-alone stuck-fault or gross defect screen test of the total analog FEM (see Figure 3).

The data analysis on the remaining test lots quantified the module yield impact due to the removal of the jitter test at wafer level as a fraction of a percent. The gain test, in tandem with the opportunistic use of the wrap feature, provided the cost-effective and efficient wafer test tool required in high-volume production.

As is typical for LSSD logic and parametric tests, the digital tests of the microprocessor and CSC logic were applicable as developed.

• Yield learning

Because of the step function in production ramp-up, the time spent in yield learning had to be reduced to a minimum. The difference between the rate of yield learning and the rate of production ramp-up would translate to lost revenue and decreased serviceability.

Mixed-signal devices have inherent compound yield detractors. As discussed, analog is very sensitive to process variation—everything from delta L to mobile ions can cause instant, unexplained yield losses. Yet, because of the size of the analog devices, they are tolerant of defects. The opposite is true of 1- μ m CMOS. LSSD CMOS is resistant to process variation, and performance sorting due to this variation is easily accomplished [10]. On the other hand, CMOS logic yield is inversely proportional to defect densities. The device sizes and wiring widths are prone to faults caused by defects. To produce mixed-signal chips profitably, no aspect of process line control can be overlooked. Defects and/or process variations can cause severe yield and serviceability degradation.

The yield detractor analysis on the test lots provided invaluable insight into the sensitivities and process window required to make the LAN manufacturable, because it showed clearly that single-digit changes in millivolts, nanoseconds, or megahertz could cause significant yield losses.

The test data and the diagnostic capability derived from the design-for-test features provided the framework within which yield information, process variation, and design changes could best benefit one another.

• Reliability

The distinctly different characteristics and tolerances of analog and digital devices to reliability stress parameters required detailed research and experimentation in the

parameter determination. In the past, the vast majority of analog chips did not require preshipment stressing (burn-in) in order to meet the reliability requirements. This was true primarily because burn-in identified defects, and analog circuitry, as discussed, was tolerant of defects because of the larger size of analog devices. However, mixed-signal chips must be stressed because of the CMOS circuits. The opportunity now existed to stress the analog and potentially increase reliability, if a method of stressing the analog could be defined that would not damage the circuitry due to the high voltage and temperature required in burn-in. Engineering experimentation in reliability applications demonstrated that the FEM running at nominal frequency could tolerate the stress conditions with no ill effects, thus allowing the analog to be stressed simultaneously with the digital.

The test lots proved indispensable in developing reliability stress specifications. CMOS is defect-sensitive, and the reliability stress screens chips that have defects. Analog circuitry is sensitive to process variation, and the test lots made available product with process variations for reliability stress experiments. The FEM was very dependent upon matched p-channel transistors. The test yield data showed conclusively that mobile sodium ions in the silicon adversely affected the reliability of the FEM; this crucial information brought about the formation of two study groups. A group of process specialists were chartered to identify any possible sodium sources and implement process monitoring tools to guarantee an ionically clean process. Simultaneously, test and reliability engineers were commissioned to extract all the information about the behavior of ionically contaminated product and develop manufacturing tests and procedures that would screen this product from any sample. A significant sample of product processed with varying mobile ion concentrations existed in test lots, so the experimentation began using the tests that were already in place.

The work required constant interfacing with the reliability engineering (RE) group, who provided information from their experience with ionic contamination and the characteristics of mobile ions. Key information included the mobility of ions with increasing temperature, and the different characteristics of the ions with and without bias voltage applied. A bake procedure (temperature without voltage) would cause the ions to disperse randomly and therefore migrate away from the gates of the devices (in this case, sodium and p-channel devices). A burn-in process (temperature and stress voltage applied while the chip was stimulated functionally) caused the ions to congregate in the gate area of the devices and therefore disrupt normal operation of the device. It was also known that time

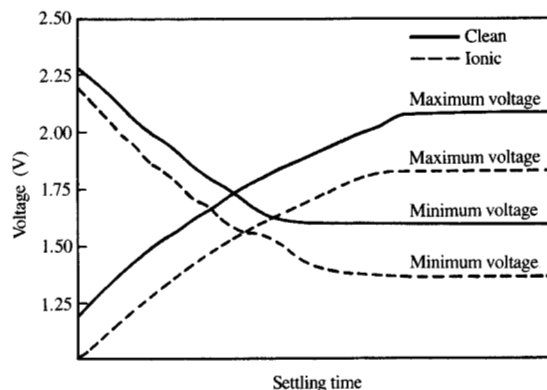


Figure 9

PLL response time deltas due to mobile ion changes.

duration was a critical factor. The challenge was to determine what burn-in duration caused the concentration of ions in the gate to reach a maximum, and then develop a test to apply at that time to screen the clean modules from the contaminated. The change of characteristics after baking was confirmation that the module was in fact contaminated with mobile ions. Failing modules at each burn-in readout were baked to determine whether they became good after baking. Determining the burn-in duration that maximized the fails in a given sample was a tedious but straightforward process. Developing a test that could distinguish a clean module from a contaminated module also required time-consuming experimentation, but the critical aspect was correctly connecting intuitive and empirical data from both qualitative and quantitative experiments.

The basic gain test on the FEM found the majority of the fails, but finding the majority was not satisfactory in meeting reliability requirements that are measured in hundreds of parts per million (PPM). Existing reliability data showed that mobile ions cause performance degradation in CMOS logic. Based on this, the performance of the PLL was characterized to see if there existed a phenomenon or characteristic that could lead to a definitive test. Engineering analysis of the data depicted in **Figure 9** revealed that the performance characteristics of the VCO under ionic influence could provide the foundation for a test methodology. There was a clear and measurable distinction between the response time of contaminated product and clean product. The gain test showed conclusively that a contaminated module could not reach an operating voltage extreme from a filter

precharged to the opposite potential in a specific time duration. The time duration was determined experimentally from the consistent performance of uncontaminated modules. The data from the test lots correlated with the process information and was verified on subsequent lots utilizing the process monitoring advances made by the study groups.

The modifications in the gain test and test procedures given below are marked with an asterisk. These are modifications to the static gain test procedure outlined previously.

- *1. Experimentally determine the point in the burn-in cycle of the product where the yield detractor, due to (process) charge mobility, is the greatest.
- *2. Burn-in the product, providing stimulus to the FEXTAL, such that the PLL is working at a nominal frequency (i.e., 8 MHz).
- *3. Remove the product from burn-in at the time determined by step 1.
4. Force FEXTAL with a frequency equal to 1.1 times the nominal frequency of the PLL (i.e., FILTA/B with FEXTAL = 8.0 MHz).
5. Measure the voltage at FILTA/B [= $V(1.1)$].
6. Repeat steps 4 and 5 using a frequency equal to 0.9F nominal [= $V(0.9)$].
7. Calculate the slope of the static transfer curve around the nominal frequency (V_o) as follows:

$$V_o = \frac{F(1.1) - F(0.9)}{V(1.1) - V(0.9)}.$$

8. Measure the charge pump current I_p at FILTA/B.
9. Calculate $F_{\max}$ and $F_{\min}$ for the chip under test as follows:

$$F_{\max} = F_{\text{nom}}(1.02) \frac{I_p(R_1)}{V_o},$$

$$F_{\min} = F_{\text{nom}}(0.98) - \frac{I_p(R_1)}{V_o}.$$

10. $V_{\max}$ test
 - *● Precharge node FILTA/B to 0.00 V.
 - Force $F_{\max}$ at FEXTAL.
 - *● Delay delta t (determined experimentally).
 - Measure $V_{\max}$ at FILTB.
11. $V_{\min}$ test
 - *● Precharge node FILTA/B to 3.00 V.
 - Force $F_{\min}$ at FEXTAL.
 - *● Delay delta t .
 - Measure $V_{\min}$ at FILTB.
- 11a/b. 16-Mbps test (optional—4-Mbps ring speed is adequate).
 - Repeat steps 5–11 using FILTA and a 32-MHz signal at FEXTAL.

12. Calculate the upper slope (M_1) and the lower slope (M_2):

$$M_1 = \frac{F_{\max} - F(1.1)}{V_{\max} - V(1.1)},$$

$$M_2 = \frac{F(0.9) - F_{\min}}{V(0.9) - V_{\min}}.$$

13. The pass/fail criterion is such that the slope of the roll-off is within 25% of the nominal transfer characteristic

$$0.75V_o < M_1 \text{ or } M_2 < 1.25V_o.$$

The LAN manufacturing group reconvened to assimilate the data from the process, test, and reliability engineering developments. The information was judiciously used by the chip designers to make minor modifications in the design to render the LAN chip as tolerant as possible of mobile ions. From the results of the joint study group, manufacturing acquired

- A clear process window definition and accurate monitoring techniques in the manufacturing line.
- A mixed-signal design resistant to process variation.
- Test procedures that reliably screened production volumes for mobile ion contamination.

The result was a significantly increased reliability in analog circuitry. The gain performance test did not affect the yield on uncontaminated product. Therefore, that test became the manufacturing test and provided a continual screen and monitor of the process line.

Techniques for reliability stressing and screening digital circuitry were known and implemented on the CMOS digital section, but frequent yield fluctuations existed. Yield data from test lots with process variations other than mobile ion concentrations experienced 30–70% yield losses during burn-in. The device failure analysis revealed latch-up in the digital sections. The puzzling aspects were the obvious lot dependence and the fact that the stress conditions and equipment were identical to those used on lots that were stressed and had yields that met the manufacturing target.

Analysis of the data from process, test, and tedious engineering experiments revealed that the common thread running through the sample of product in question was high current capacity. Various current-limiting methods were used, all of which were successful in increasing the snap-back voltage (voltage needed to cause latch-up), which demonstrated the dependence of latch-up on current capacity. If the correct processing characteristics came together such that a given lot was a high-performance lot, that lot would show high losses in burn-in. These lots, if not stressed, met specifications, but the combination of high performance (which equates to

high current) and standard reliability stress conditions was catastrophic.

CMOS is theoretically a low-power technology. In fact, 98% of the product cycle is low-power and therefore low-current. However, experimentation showed that the other 2% was the opposite. CMOS devices remain in the quiescent state until the functional clocks are fired. The instantaneous current during the 10–25 ns immediately following the clock activation can be measured in *amps* on large CMOS chips. The situation is aggravated in large mixed-signal designs. Mixed-signal chips have a steady-state current due to the analog circuitry, in addition to the instantaneous component, which augments an already undesirable characteristic. The simultaneous nature of LSSD clocking maximizes the instantaneous destructive current.

To reduce the instantaneous current, a number of options were available. Further process controls were ruled out, since that would eliminate any supply of high-performance product. Reduction of the stress voltage was the most obvious choice, but in order to maintain reliability, a reduction in voltage requires an increase in temperature or time duration. Packaging specifications precluded a temperature increase, and the required time duration forced undesirable decreases in throughput. The existing voltage had to be maintained.

Through engineering analysis of product simulation runs, it was determined that the instantaneous nature of the current could be used as a distinct advantage. Power requires current and voltage simultaneously at sufficient levels to cause damage. In this case, it was instantaneous power that was initiating latch-up, so reduction of either current or voltage or both would solve the problem.

A technique was devised to accurately measure the amplitude of the instantaneous current. Applying this technique, a series resistor value could be chosen and placed in series between the power supply and the chip that would provide the instantaneous protection needed. The high current amplitude required a low resistor value (1–3 Ω), which maintained the stress voltage after the 10–25-ns surge had subsided. The resistor value was chosen such that during the short high-current window, the effective voltage experienced by the chip was reduced to slightly below nominal ($0.9V_{dd}$). The quiescent current in CMOS is typically 1 μ A to 30 mA (mixed signal), which translates into a 3- μ V to 90-mV drop in stress voltage, assuming a 3- Ω resistor. Data on 10 000 LAN modules from various test lots showed conclusively the lot dependence and overall yield effects of limiting the instantaneous current component in burn-in (Figure 10).

The understanding of reliability phenomena and implementation of the described techniques resulted in overall reliability failure rates that remained consistently

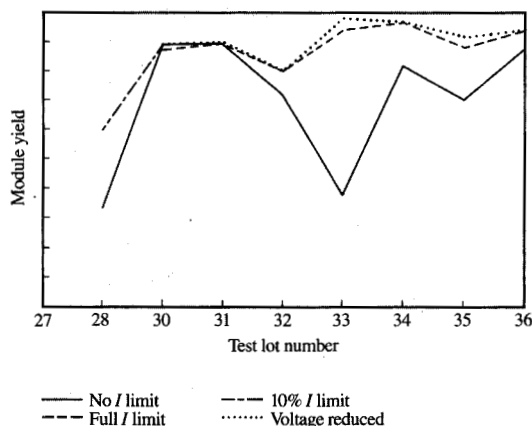


Figure 10

Effects of current limiting during reliability testing. (Note that each lot was split and different current-limiting techniques applied to each split to maintain process unity across the different techniques.)

well below the specifications. Yield and reliability had been maximized without significant cost.

Summary

This paper has taken the reader from early development through high-volume manufacturing of the LAN chip, highlighting the achievements associated with its development, qualification, and release to production.

Partitioning was shown to provide critical benefits in diagnostics, independent/parallel debug, and cycle time reduction during development. The implementation details and development of a combination of static VCO gain and functional jitter tests are outlined. The engineering evaluation showed that the VCO gain characteristics and the behavior of the static transfer curve were dictated by process anomalies and variation across the wafer. The data revealed that key characteristics had to be measured, and test stimuli and limits calculated individually by chip in order to maximize yield and reliability. Each chip required unique, process-dependent test conditions. This test technique, which calculates test stimuli and pass/fail criteria by chip, proved crucial in guaranteeing LAN performance and reliability. In addition, the static nature of the gain test filled a critical void in wafer testing capability.

Although developments in the gain test method ensured the fundamental transfer characteristics of the VCO, it was clear that this test was necessary but by itself

was not sufficient to meet the highest standards of quality, reliability, and performance. To protect potential future applications of the LAN, a functional test of the PLL was developed that provided the capability to sort product based upon very accurate jitter measurements taken at application speeds and conditions. The development of this unique test required the following:

- Noise-free, low-amplitude, high-frequency signal input.
- Test-system-to-PLL synchronization.
- Real-time Manchester-code application and monitoring.
- Calculation and application of functional speed test stimuli by chip.

The development and implementation of a novel test technique that reliably identifies and screens product contaminated with mobile ions (Na^+) is described. The ability to identify mobile ion contamination sensitivity and concentrations is provided by a unique performance test of the VCO circuit.

The authors were able to demonstrate the dependence of latch-up on instantaneous power dissipation, primarily driven by the combination of stress voltage and the magnitude of the short-time-duration switching currents. A unique technical solution that maintains stress conditions and protects against instantaneous power damage is described. This combination of new techniques has resulted in analog circuit evaluation that uniquely marries characterization and manufacturing test needs.

It has been shown that yield learning must begin with the first prototype lot in development. Test lots are mandatory—the benefits far outweigh the costs. The points are made that reliability requires development, not just definition, and that, like yield learning, reliability requires committed resource from the arrival of the first development lots.

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