Electron-beam technology for open/short testing of multi-chip substrates

by S. D. Golladay
N. A. Wagner
J. R. Rudert
R. N. Schmidt

We discuss the need for noncontact electrical testing of high-performance multi-chip substrates and describe an electron-beam tester developed for this application. We describe the operational principles of the tester and compare and contrast its performance with that of mechanical probe testers. Finally, we discuss the motivations and technical issues involved in extending the electron-beam test method to future high-performance packages.

Introduction

Multi-layer, multi-chip ceramic (MLC) packages for high-end computer systems have reached a high degree of sophistication. Introduced in the early 1980s in mainframe systems as part of the thermal conduction module (TCM), MLC substrates represented a new level of performance in providing chip interconnection, power distribution, and cooling [1].

©**Copyright** 1990 by International Business Machines Corporation. Copying in printed form for private use is permitted without payment of royalty provided that (1) each reproduction is done without alteration and (2) the *Journal* reference and IBM copyright notice are included on the first page. The title and abstract, but no other portions, of this paper may be copied or distributed royalty free without further permission by computer-based and other information-service systems. Permission to *republish* any other portion of this paper must be obtained from the Editor.

It is now widely appreciated that the high-end computer systems of the 1990s will require further improvements in MLC packages to fully exploit the opportunities presented by the continued evolution of semiconductor technology [2, 3]. Packages with finer and denser wiring are needed to support the increased input/output requirements of more highly integrated semiconductor chips.

These trends in high-performance packages make the task of testing substrates for opens and shorts with mechanical probes increasingly difficult. Smaller features are not only more difficult to contact, they are more likely to be damaged by contact. Future substrate design choices with respect to both feature size and materials could be constrained by the requirements of contact test to the detriment of electrical performance.

These improvements in package performance will almost certainly require a more complex manufacturing process, and one in which increased attention is paid to reducing particulate contamination of the product.

Electron-beam testing offers a way to obtain information about the electrical integrity of a product at any point in the manufacturing process without damaging or contaminating the product. In this paper we discuss noncontact test methods using electron beams as part of the test and inspection strategy for high-performance substrates. We base our discussion on the

theoretical virtues of the electron-beam (e-beam) test method, and on practical experience with a first-generation tester.

In its introductory role in the packaging laboratory at the IBM East Fishkill facility, e-beam contactless testing has provided process yield data, product design verification, test vehicle evaluation, and test of early user hardware. The pilot line system, PL1, aimed primarily at the testing of fired ceramic substrates ranging from single-chip modules to large multi-chip modules, laid a solid foundation for extending the technology to more advanced substrates.

In this paper we discuss the basic operational principles of the electron-beam test method and compare the e-beam tester to several types of contact testers. We then describe the applications, architecture, and performance of the pilot line system, and finally the issues involved in extending e-beam test to future applications.

Electron-beam test method

The e-beam test method employs multiple electron beams to generate and to detect voltage differences between the surface terminations of substrate conductor networks. When any solid is irradiated by sufficiently energetic primary electrons, scattering processes result in the re-emission of electrons. By convention, the total yield of re-emitted electrons is subdivided into two classes depending on kinetic energy: Secondary electrons (SE) have energies of 50 eV or less; all others are categorized as backscattered electrons (BSE).

The secondary electrons play a crucial role in both the voltage-generation (charging) and voltage-detection (reading) processes. Node voltages are measured or read by analyzing the kinetic energy of the SE and thereby the electrostatic potential of their point of origin. Intensity modulation of the SE signal arising from voltage differences is called voltage contrast.

There are numerous commercially available electron-beam instruments which exploit voltage contrast to measure voltages on internal nodes of integrated circuits. Input signals and power are provided from external supplies through mechanical contacts. The e-beam substrate tester is fundamentally different in that it uses the electron beam to charge or discharge nets, thereby contactlessly generating the voltage differences required to test a substrate for shorts between networks or opens within networks [4].

Substrates typically have interconnections between nodes on a single surface (top-to-top nets) and interconnections between the top and bottom surfaces (top-to-bottom nets). The testing of the two different kinds of connections involves two different methods of charging.

- *Dual-potential testing (top-to-top nets)*

Although for actual automated substrate testing the e-beam tool directs the primary beam just to the network nodes, the basic idea of defect detection can be illustrated by scanning the substrate to produce a voltage-contrast (VC) image of a defective net. The testing of nets with only top-surface nodes is illustrated in **Figure 1**, where a single chip attachment site has been imaged in voltage-contrast mode. (In the photograph the voltage-contrast intensity variations have been converted to color differences.) The integrated circuit chips are attached directly to the substrate at the array of round vias at the center of the image. These vias are in turn connected to the larger pads arranged around the perimeter of the chip site. Figure 1(a) illustrates continuity between a pad and its associated via. The pad was charged by the electron beam before the site was imaged. The similarity of the signal levels (colors) of the pad and its associated via confirms the continuity of their interconnect wiring. Figure 1(b) illustrates the detection of an electrical open between a pad and a via. The pad was charged by the same procedure as before, but in this case the signal level at the associated via remains at a level indicative of an uncharged condition.

The test method just described is known as dual-potential testing because the primary-beam energy is switched between two different beam potentials; a relatively high-energy beam is used to charge networks, and a lower-energy beam is used for reading net voltages, discharging nets, scanning the insulator [5], and producing VC images such as those in Figures 1–3.

- *Single-potential testing (top-to-bottom nets)*

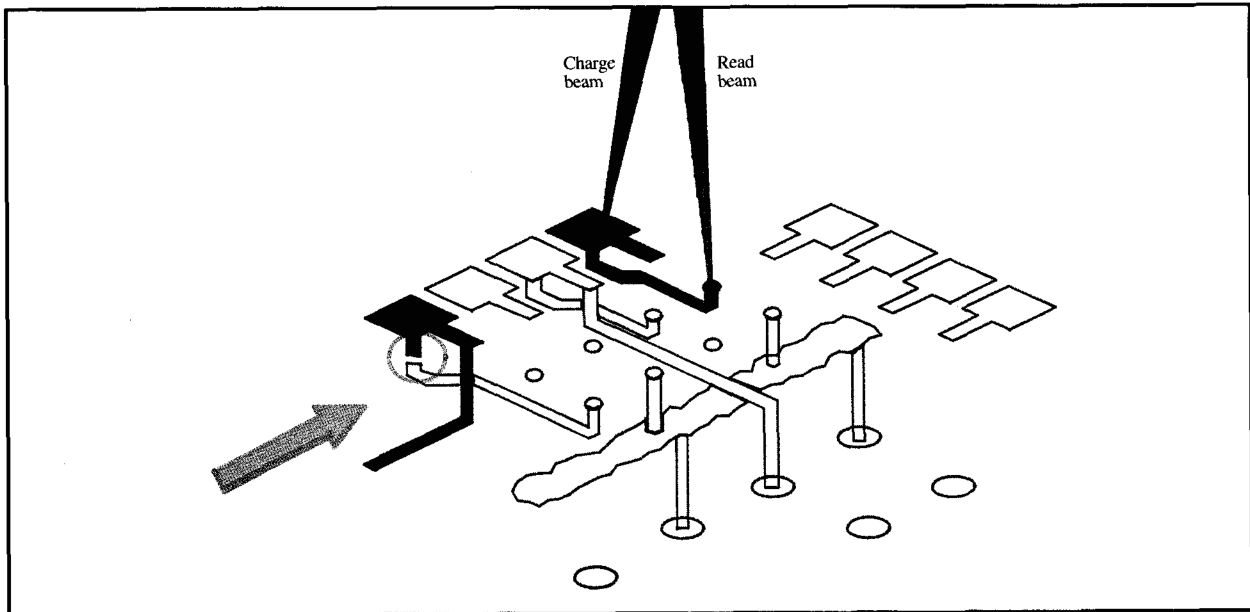
The continuity of connections between the top and bottom surfaces of the substrate is verified by using a different charging method. In this case all nets with bottom-surface nodes are charged from below using a broad flood beam of electrons. If the top surface of the substrate is again imaged, the networks with continuity to the bottom are clearly distinguished from those without, as illustrated in **Figure 2**.

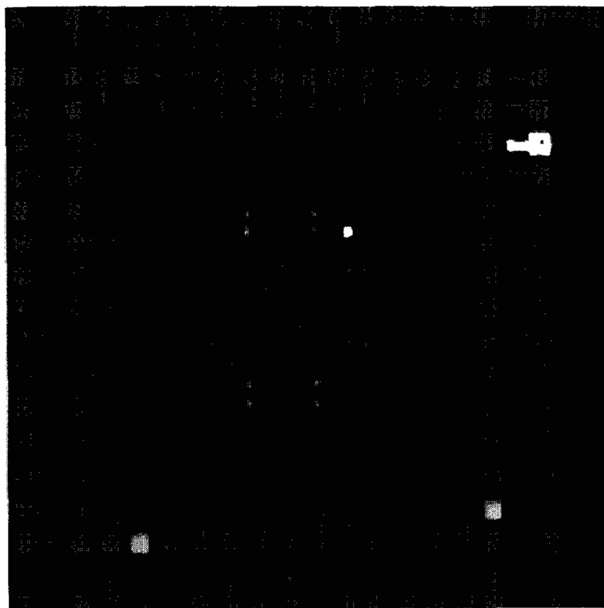
E-beam/contact test comparison

The strengths and weaknesses of e-beam contactless testing can be placed in perspective by comparison with mechanical probe contact testing.

Testing for shorts

In comparing test methods, it is important to realize that detection of shorts is potentially much more time-consuming than detection of opens. Consider the task of testing a substrate manually with two probes and an ohmmeter. Continuity verification within a net requires contacting each of the net nodes. Ensuring the isolation





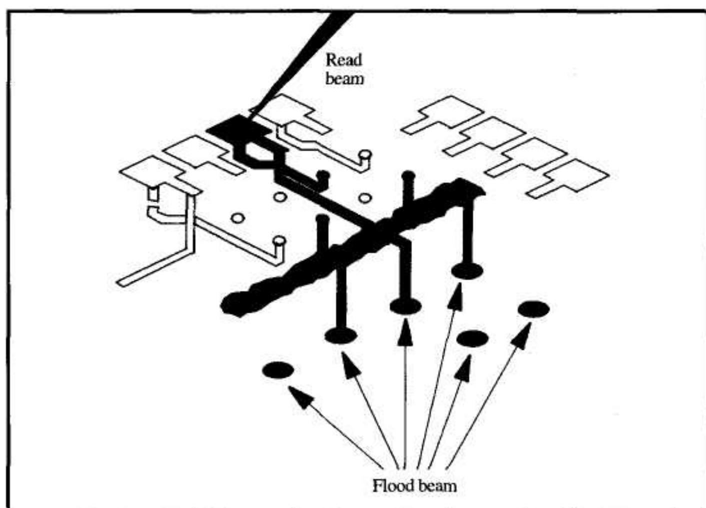
(a)

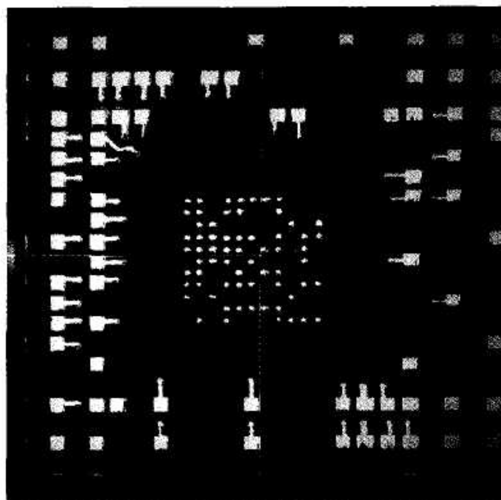
(b)

Figure 1

Top-to-top test. (a) Voltage-contrast (VC) image of a single device site on a multi-chip substrate. The continuity of the interconnection between the bright pad and its associated via is illustrated by the similarity of their signal levels. The pad was charged by the electron beam prior to producing the image. (b) The VC image of (a), with the addition of an open between the charged pad and its associated via. Note the absence of a via which exhibits a signal level similar to that of the charged pad.

of the net from all others requires contacting all other nets. A typical high-performance substrate might have 10 000 nets averaging only three nodes per net. In this case, testing a net against all others for shorts would require 10 000 contacts in contrast to only two to test for opens within a net. Taking into account that the test for shorts between a pair of nets need be done only once, one concludes that for the complete substrate, testing for shorts would take roughly 2500 times longer [i.e., 10 000/(2 × 2)], than testing for opens. Further increases in package density increase the factor by which testing for shorts dominates.





Top-to-bottom continuity

Figure 2

Top-to-bottom test. VC image showing the contrast between networks charged from beneath by an electron-beam flood gun and networks without connections to the substrate bottom surface.

All testers aimed at high throughput need some way to expedite shorts testing by introducing parallelism. Mechanical probers can accomplish this in two ways, as described in the following sections.

- *Cluster probers*

One method of introducing parallelism into the probing process is to use a probe head that contacts many features simultaneously. With this approach it is highly desirable to contact all test points at once; otherwise, testing involves extensive step-and-repeat operations, with each test point being probed multiple times. Assuming that there are no problems in making good electrical contact, cluster probing can provide good resistance characterization and high throughput. The difficulties of the method are associated with the probe heads, which present formidable design, manufacture, and maintenance challenges.

- *One/two-point probers*

An alternative approach to achieve parallelism in testing for shorts is to measure net capacitance relative to an internal or external reference plane. Capacitive short detection is practical as long as all nets are more strongly coupled to the reference plane than to any other nets. Since this condition also reduces signal crosstalk between networks, it is at least plausible that capacitive short detection should work well for high-performance substrates. Given strong coupling to the reference plane, if one considers the various possible combinations of small and large networks, it is clear that one net involved in a short will change its capacitance by at least a factor of two. This change in capacitance should be larger than that due to process variation or measurement errors. However, in cases where a very large net is shorted to a very small net, only the small net will be identified as defective. The second net involved in the short, the "silent partner," cannot be found with a single probe. Opens can be detected if capacitance measurements are made at each net node. In this way, a one-point prober can perform a "complete" test with a relatively simple mechanical system. The system also has a great deal of flexibility to adapt to varying substrate geometries.

These advantages are obtained at the expense of quantitative resistance characterization. For commercially available one-point probers, the dividing line between continuity and discontinuity is of the order of a megohm or more. The practical consequence is that compared to an ideal tester, the one-point prober may over-report shorts and under-report opens.

To eliminate the possibility of missing opens, a second probe may be used for true ohmic net continuity verification. To obtain reasonable throughput, detection of shorts must still be done capacitively. With two probes, one can now reprobe systematically to identify the shorted "silent partners." Depending on the number of defects in a substrate and the length of the list of potential partners, the shorts identification time can vary over several orders of magnitude. The effect on overall tester throughput can range from slight to very significant.

E-beam tester

Considering only mechanical contact test, the previous discussion illustrates some of the trade-offs to be made among tester throughput, resistance discrimination, system flexibility, mechanical complexity, and reliability.

The trade-off possibilities are greatly increased by the e-beam test method, which brings with it significant new capabilities in terms of speed, spatial resolution, and elimination of physical damage caused by probing, but at the expense of resistance discrimination.

The e-beam tester shares with the one-point prober the inability to distinguish between low-resistance interconnections and those with high internal resistance. Brunner et al. [6] estimate the minimum detectable resistance to be approximately 10 MΩ.

The e-beam test method has its own technique for introducing parallelism into the process of detecting shorts. It is based on the idea of storing charge on the nets. (Nets in MLC substrates are observed to retain charge for 12 hours or more under vacuum conditions.) In the dual-potential test mode, nets are charged to verify continuity and then left charged when the tester proceeds to the next net. Each net is read before charging. In effect, this initial read tests each net against all previously tested nets. The initial detection of a short identifies only one net involved in the short, but unlike the one-point prober, the e-beam tester can identify the other shorted net with additional testing. Subsequent to the first complete pass through all the nets, the substrate is discharged, all nets found shorted are charged, and the remaining nets are read. This step identifies all nets involved in shorts. Shorts pairing can proceed by a process of discharging a net and reading the nets which are potential partners.

E-beam tester throughput

The high throughput potential of e-beam test results from the speed with which the basic functions of beam deflection, voltage discrimination, and net charging can be accomplished. As already demonstrated on the pilot line system, PL1, the beam can be deflected to any test point within the deflection field in roughly 250 μs. Charged/uncharged voltage discrimination requires an additional time of the order of 5 μs.

In dual-potential testing, which is by far the slowest test mode, most of the test time is spent charging nets. Charging times are typically 0.1–10 ms per net. Assuming 5-ms charge times, a substrate containing 10 000 nets in 30 000 nodes could be tested in approximately two minutes, including realistic allowances for part transport into and out of the system.

In the case of single-potential through-connection testing, all the nets can be charged in a few seconds by the flood gun. Reading of top-surface nodes to detect opens can be done at a rate of approximately 2000 nodes per second.

The times quoted for basic system functions are representative of what is easily practical both technically and economically, rather than what is theoretically possible. Appreciably higher throughputs can be achieved if there are economic incentives to do so.

E-beam test experience

PL1 application

One of the first projects on PL1 was a study of whether the e-beam tester would fail to detect significant numbers of open defects. A sample group of multi-chip substrates, tested by mechanical probers and rejected for electrical defects, were retested by PL1. The test included approximately 860 000 net nodes. The result was that all open and short defects known to exist in the substrates were detected by the e-beam system. In measurements of the actual resistance values of several thousand opens, none were found with resistances which might be mistaken by the e-beam tester for continuity.

PL1 has been operating in a pilot line mode in the IBM East Fishkill packaging laboratory, where its flexibility has proven extremely useful. This flexibility helps reduce the time needed to manufacture new substrates by eliminating the need to build expensive probe sets for each new design. Data for the tester can be generated quickly in contrast to the 6–9 months needed to build cluster probes. The ability to test without probes also makes e-beam test attractive for low-volume substrate programs. The flexibility inherent in a software-driven tool is illustrated by the VC image of **Figure 3**, where a number of nets have been tested, left charged, and imaged.

Another role of PL1 has been to provide partial design verification and/or test capabilities for parts which have no test data. This is accomplished by using the tool in a voltage-contrast imaging mode which allows visual detection of voltage-plane opens and shorts and verification of through (top-to-bottom) network continuity. The imaging test mode which is so natural and simple in an e-beam system has no counterpart in contact testing. Through this method, PL1 has been able to provide early feedback on new substrate designs and on the yield of new processes.

Finally, PL1 has provided preproduction test capability in support of manufacturing. Because of its flexibility, there have been situations in which PL1 has been the only tester capable of testing the first substrates of a new design; consequently, it has played an important role in the delivery of substrates for prototype system tests.

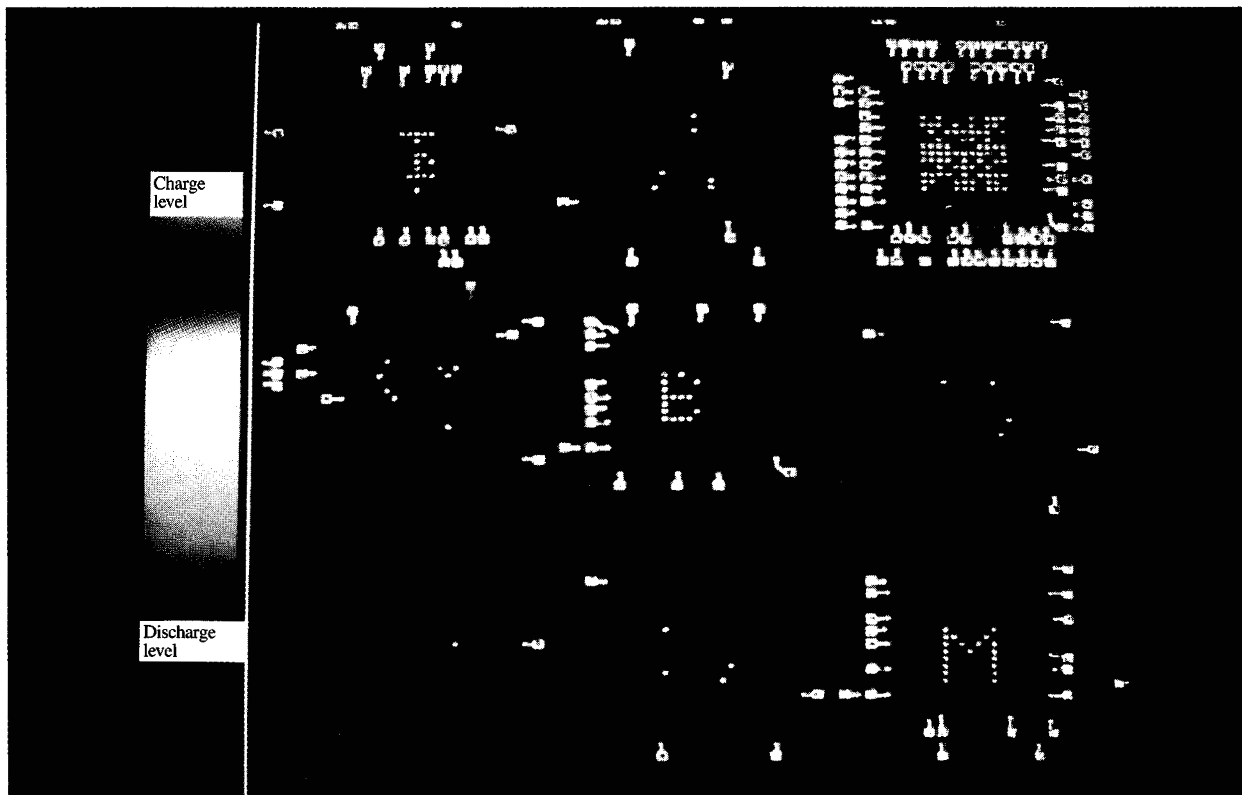


Figure 3

VC image illustrating the automated testing of a large number of networks on a substrate.

• *PL1 architecture*

The PL1 tools comprise several major parts—a mechanical and vacuum system, electron-beam column, control electronics, system computer, and software. A system block diagram is illustrated in **Figure 4**.

Mechanical/vacuum system This subsystem includes an x–y stage, a load/unload airlock for one substrate, vacuum pumping, and controls. Sequencing and vacuum measurement are controlled by a microprocessor which allows the user to operate the unit using high-level commands.

Column The function of the e-beam column is to generate, focus, and deflect the primary beam, and to detect secondary electrons produced when the primary beam strikes the substrate. The column and control electronics are internally developed using or adapting the IBM EL3 lithography system hardware to the extent possible. The column is reconfigured to support dual-potential operation. Beam energy is switched by a fast high-voltage FET switch. An SE voltage-contrast detector [7] and magnetic deflection system provide coverage of a 90-mm-square field with a probe beam of approximately 30-μm diameter.

Control computer The PL1 tool is controlled by a computer which communicates with a deflection control unit to provide raster scanning, vector beam addressing, and the capture of voltage-level feedback data for imaging or testing.

Control software The tool-control programs perform a number of functions to accomplish the test. Three levels of calibration are used to achieve the necessary beam-placement accuracy. First, there is the field calibration, which uses a standard grid to characterize the distortions inherent in the column deflection system and final lens. Then the substrate is registered to fix its location. Finally, each device site is mapped to measure the displacement

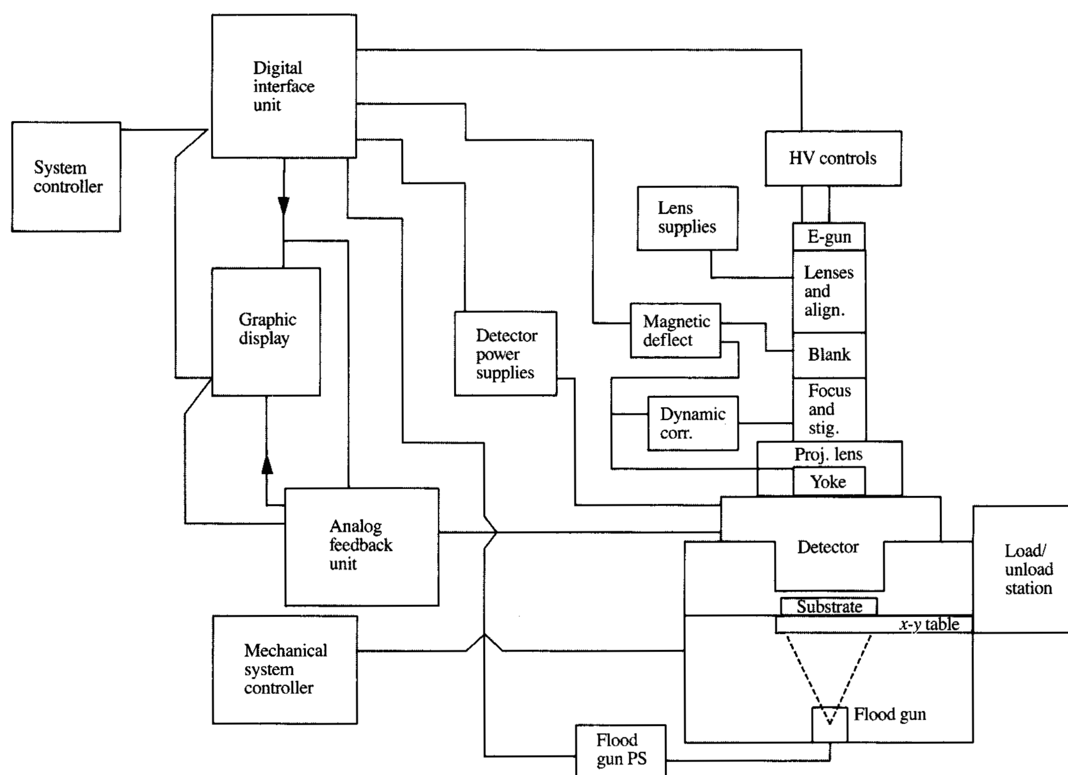


Figure 4

Block diagram of the PL1 electron-beam test system.

of test nodes from their nominal positions that occurs during the substrate firing process.

The test control program uses a standard format net list which describes the configuration of each net and the location of each accessible net node. Using the net list and various application programs, the main test program performs read and charge functions to detect open and short defects.

Advanced e-beam applications

The success of PL1 has served to build credibility for e-beam testing. However, most of the e-beam experience thus far has been on thick-film substrates where the combination of relatively large features, excellent yields, and the robust materials of the fired substrate permit a test strategy involving contact test of the final product only.

The manufacturing process for advanced products is likely to be more complex, and less tolerant of particulate contamination, while the product itself may be more easily damaged by mechanical probing. In such an environment, early defect detection by noncontact techniques for process control and cumulative yield improvement would seem to offer significant advantages.

Since there is essentially no risk of product damage by e-beam test, one can consider using it repeatedly at various points in the process of building layered substrates. Appropriate test points must be chosen, taking into consideration product and process characteristics as well as the applicability of other inspection, electrical-test, and defect-repair equipment. Unrepairable defects must be detected as early as possible. Some defects may be repairable in-process only if detected at the appropriate time, whereas others may be repaired later by the engineering change features incorporated into the product. The technical issues involved in extending e-beam test to

advanced product applications fall into two areas: compatibility of the test method with the relevant materials (in particular materials implications for the charging process), and trade-offs between beam size and deflection-field size.

Beam size/deflection-field size limitations

Considering the image resolution routinely demonstrated by electron microscopes, the extendibility of the e-beam tester to small feature sizes is obvious. In e-beam testing, there is also the issue of how large a field can be covered while maintaining a given beam size.

At the relatively low primary-beam energies required to control insulator charging, chromatic deflection aberrations limit the obtainable field size. Fortunately, the considerable development that has gone into the deflection system of the IBM EL3 e-beam lithography system is relevant. High-speed deflection with a considerable degree of chromatic aberration correction can be obtained using the EL3 approach of in-lens, magnetic deflection with a pair of air-core yokes [8].

Nevertheless, one can anticipate that substrates will eventually have a combination of minimum feature size and overall size which will require step-and-repeat e-beam testing. The consequences for tool throughput will vary depending on the actual network structure and the particular test performed. For in-process testing, certain layers may permit partitioning of testing into noninteracting subfields, in which case the throughput impact will be minimal.

E-beam charging

Next we discuss the issues involved in extending the e-beam charging processes to handle smaller features and a wider variety of materials. As mentioned previously, the dual-potential test method uses a relatively high-energy primary beam to charge individual nets negatively, and a lower-energy beam for reading net potential, discharging nets, and scanning the insulator. The choice of beam energies is influenced by the SE emission properties of the package materials. The total yield (δ), which is the ratio of emitted current to primary-beam current, varies with primary-beam energy, as illustrated schematically in **Figure 5**. The general shape of the curve is characteristic of both conductors and insulators because it reflects two fundamental but countervailing physical processes. As primary-beam energy increases, more energy is available to drive the inelastic processes which generate secondary electrons (SE). On the other hand, the inelastic processes occur increasingly at depths from which potential secondaries do not escape the material.

The variation in total yield permits several distinct charging processes. The charging methods differ in terms of their applicability to different materials sets, the methods employed to spatially localize the charging, and the method used to control the final potential reached by a network.

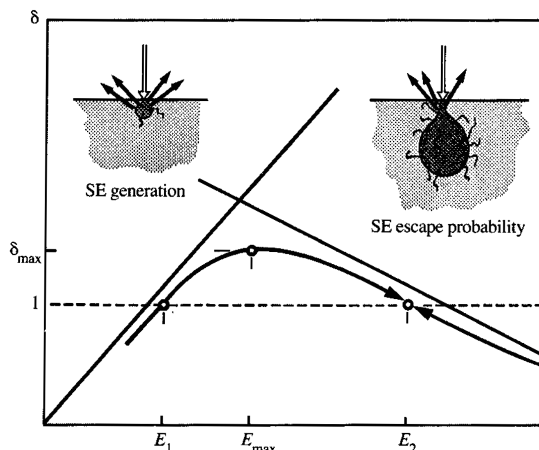


Figure 5

Schematic representation of the total electron yield, δ, which is the ratio of emitted current to primary-beam current, for a solid.

Low-energy-beam charging

If the primary-beam energy, E, is chosen to produce copious SE (i.e., $\delta > 1$, $E_1 < E < E_2$), materials can be charged either positively or negatively depending on whether the SE are extracted from the substrate or repelled back to it. A grid above the substrate can be biased to control the charging process. The irradiated point is driven toward an equilibrium potential at which SE emission just balances charge injection by the primary beam. Because the majority of SE have kinetic energies of only a few electron-volts, a potential difference of only a few volts is sufficient to reflect enough SE to balance electron injection and emission. The equilibrium potential is therefore just a few volts positive relative to the external grid, and can be manipulated by changing the grid potential.

If the primary-beam energy is chosen so that total yield exceeds 1 for both conductor and insulator, the grid-controlled charging process just described is applicable to all the conductors and insulators of interest for packages. In addition, the method involves only a single primary-beam energy and can therefore be implemented with a conventional electron-beam column.

There are two limitations with respect to grid-controlled charging. One possible problem with the grids is that they must be close to the sample surface so that the primary beam "sees" the substrates through the grid. The grid, currently consisting of 5-μm wires on 1-mm centers, is highly transparent and at present has negligible impact on testing. If or when product feature sizes approach those of the grid wires, refinements to the grid structure or test method may be required to avoid grid wire interference.

A second, more fundamental limitation arises with grid-controlled negative charging. Although positive charging is well localized to the irradiated feature, in the case of negative charging the external grid repels many secondary electrons back to the substrate. To confine the returning secondary electrons to a small feature requires external fields so strong that they may interfere with the primary-beam resolution and/or placement. A practical limit on feature size (for negative charging only) is approximately 100 μm. (This finding is based on private communication with Kam Leung Lee of the IBM Research Division, Thomas J. Watson Research Center, Yorktown Heights, New York.)

The nonlocal character of negative charging can, however, be used to advantage to charge entire surfaces uniformly, as is required for through-connection testing. In fact, if all the networks in a substrate have through connections, as is the case for a single-chip module, a complete test is possible using only grid-controlled charging. All nets are charged negatively from below by the flood gun and then sequentially discharged from the top with the focused probe beam. This kind of test is relatively easy to implement and is applicable to any substrate materials.

High-energy-beam charging

For the testing of nets with only top-surface nodes, it is desirable to utilize a charging process which permits well-localized negative charging. Because SE emission declines with increasing primary-beam energy, a sufficiently energetic beam can ensure negative charging that is independent of applied fields.

In contrast to grid-controlled charging, the high-energy process must be actively controlled by the test system to prevent overcharging of conductors or insulators; this process is therefore more sensitive to the particular properties of the substrate materials. The tester monitors the node potential during the charging and stops charging by blanking the beam when the desired potential is reached. Overcharging must be avoided, as it results in strong local fields which interact with the emitted secondary electrons to interfere with voltage contrast.

For the conductive pastes and inorganic insulators of the multi-layer ceramic substrate, the beam energy can be chosen to charge the conductor negative and the insulator positive. In this case, the insulator-charging process is grid-controlled; i.e., charging is limited by the external grid potential. This situation makes the charging process very "forgiving" in the sense that if the insulator is exposed to the charge beam, very little charging takes place.

For certain other combinations of insulators and conductors, the high-energy charging process is "unforgiving." If the beam energy required to charge the conductor negatively also charges the insulator negatively, extra care must be taken to avoid excessive charging of the insulator. Materials combinations falling into this category include most metals with organic insulators or gold with practically any insulator. With these materials, a slight spillover of the primary beam onto the insulator may be problematic, because the effective capacitance of the insulator is very small, and it can therefore be charged rapidly to a high negative potential. This potential can affect SE trajectories locally to the extent that the normal voltage-contrast signal is suppressed.

One approach to avoiding this problem would be to exercise extreme diligence in preventing inadvertent exposure of the insulator to the beam. A more practical approach is to accept some insulator charging but adopt a procedure which subsequently "cleans" it up. The dual-potential capability of the system allows easy implementation of such a procedure. Recent experiments show the feasibility of slightly overcharging nodes with the charge beam and then discharging them to the desired potential using the read beam (i.e., grid-controlled positive charging). In this way the conductor can be driven to the desired negative potential while simultaneously discharging any incidental insulator charging. This method promises to make e-beam testing capable of performing a complete test on any substrate regardless of the conductor or insulator combination, and in a way which is compatible with further improvements in spatial resolution.

Acknowledgments

The authors wish to acknowledge the contributions to e-beam testing made by colleagues at the IBM Thomas J. Watson Research Center, the IBM Endicott facility, and the IBM East Fishkill facility.

References

1. A. J. Blodgett and D. R. Barbour, "Thermal Conduction Module: A High-Performance Multilayer Ceramic Package," *IBM J. Res. Develop.* **26,** 30–36 (1982).
2. See, e.g., Rao R. Tummala, Robert W. Keyes, Warren D. Grobman, and Shukla Kapur, in *Microelectronics Packaging Handbook*, Rao R. Tummala and Eugene J. Ramaszewski, Eds., Van Nostrand Reinhold, New York, 1989, Ch. 9.
3. *Ibid.*, Evan E. Davidson and George A. Katopis, Ch. 3.

4. H. C. Pfeiffer, S. D. Golladay, and F. J. Hohn, "A Practical E-Beam System for High Speed Continuity Testing of Conductor Networks," *Proceedings of the XIth International Congress on Electron Microscopy*, Kyoto, Japan, 1986, pp. 185–188.
5. F. J. Hohn, D. P. Kern, P. Coane, W. Bruenger, and T. H. P. Chang, "A Tripotential Method for Electron Beam Testing," *Tenth International Congress on Electron and Ion Beam Science and Technology*, Montreal, Canada, 1982, pp. 150–158.
6. M. Brunner, D. Winkler, and B. Lischke, "Crucial Parameters in Electron Beam Short/Open Testing," *Microcircuit Engineering 84*, A. Heuberger and H. Benking, Eds., Academic Press, London, 1985, pp. 399–410.
7. W. H. Bruenger, F. J. Hohn, D. P. Kern, P. J. Coane, and T. H. P. Chang, "Electron Energy Analyser for Applications in Large Scan Field Electron Beam Testing," *Tenth International Conference on Electron and Ion Beam Science and Technology*, Montreal, Canada, 1982, pp. 159–169.
8. J. L. Mauer, H. C. Pfeiffer, and W. Stickel, "Electron Optics of an Electron-Beam Lithographic System," *IBM J. Res. Develop.* **21**, 514–521 (1977).

Received May 22, 1989; accepted for publication September 19, 1989

Steven D. Golladay *IBM General Technology Division, East Fishkill facility, Route 52, Hopewell Junction, New York 12533.* Dr. Golladay received his A.B. in physics from Dartmouth College in 1968. He joined IBM in 1979 after receiving a Ph.D. in physics from the University of Chicago. His thesis work was done in the field of high-resolution electron microscopy. Dr. Golladay's current interests include the design of electron-optical components and applications of electron-beam technology.

Nancy A. Wagner *IBM General Technology Division, East Fishkill facility, Route 52, Hopewell Junction, New York 12533.* Ms. Wagner joined IBM in 1981 after receiving a B.S. degree in electrical engineering from Lehigh University. Since that time her primary involvement has been with electron-beam testing of multi-layer substrates. She is currently a staff engineer in the packaging laboratory test development area. Ms. Wagner is a member of Eta Kappa Nu and Tau Beta Pi.

J. R. Rudert *IBM General Technology Division, East Fishkill facility, Route 52, Hopewell Junction, New York 12533.* Mr. Rudert joined IBM in 1962 after receiving an M.S.E.E. degree from Stanford University. He has held a number of product design and development positions, and is currently manager of electron-beam system applications at the IBM East Fishkill facility. His principal project is noncontact testing of substrates using electron beams.

Robert N. Schmidt *IBM General Technology Division, East Fishkill facility, Route 52, Hopewell Junction, New York 12533.* Since joining IBM in 1963, Mr. Schmidt has worked in the area of automated equipment development for both semiconductor and advanced packaging applications. His primary concentration is in the field of inspection, measurement, and test technology, where he has had various technical and managerial responsibilities. He is currently project manager of Advanced Inspection and Test Systems Engineering at the East Fishkill Packaging Laboratory.