# A submicron MOSFET parameter extraction technique

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**A technique is introduced for measuring electron and hole mobilities as a function of temperature and normal field in inverted silicon surfaces. We also introduce a new definition of threshold voltage which allows the method to measure mobility independent of channel dimensions and resistance in series with the channel. The results are used to extract the resistance in series with the channel, the effective channel dimensions, and the intrinsic MOSFET transconductance. The technique is demonstrated on MOSFETs with channel lengths ranging from 0.25 $\mu$m to 20 $\mu$m.**

## Introduction

Several methods of determining the surface mobility from MOSFET transfer characteristics have been reported [1, 2]. These techniques rely on the definition of effective channel length $L_{EFF}$ and width $W_{EFF}$, and on the measurement of source and drain resistances in series with the channel, which we will call the extrinsic resistances $R_{EX}$. Though satisfactory for most technologies, these methods become inaccurate as the device dimensions are reduced below ~0.5 $\mu$m and the ratio of $R_{EX}$ to channel resistance increases. Errors are particularly acute when the difference between designed and effective channel dimensions and the magnitude of extrinsic resistance depend on device size and applied bias conditions. The problem becomes more severe with lightly doped drains and at low temperature because of carrier freeze-out.

In this paper we introduce a measurement technique for determining the surface mobility as a function of normal field, temperature, and threshold voltage for arbitrary channel dimensions and $R_{EX}$. The results are then used to extract the effective device dimensions, the extrinsic resistance, and the intrinsic device transconductance in submicron MOSFETs.

## Threshold voltage

This section briefly describes three methods of defining and measuring the threshold voltage $V_T$.

- *Linear extrapolation method*

A widely used method is to extrapolate to $I_D = 0$ the linear part of the curve representing drain current $I_D$ versus gate voltage $V_G$. The extrapolated threshold voltage may, however, change significantly because of variations in the extrinsic resistance.

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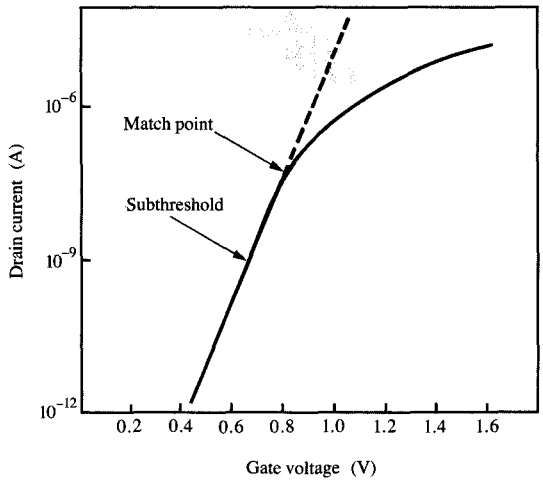


**Figure 1**

Definition of $V_T$ at match point where the measured drain current deviates by 5% from the exponential subthreshold extrapolation.

• *Constant inversion charge density method*

In another common technique, the gate voltage is measured at a constant inversion charge density $Q_{INV}$. This is typically done in the linear mode at a constant drain current per unit channel area,

$$I_{VT} = I_{SQ} \frac{W_{eff}}{L_{eff}}, \tag{1}$$

where $I_{SQ}$ is the drain current per square of channel corresponding to a constant inversion charge density, which is chosen in the $10^9 q$ cm$^{-2}$ range. This method, however, requires the ability to define the device dimensions and $I_{SQ}$ before threshold voltage measurement.

• *Match-point method*

We introduce a new definition of threshold voltage as the gate voltage for which the exponential extrapolation of subthreshold current deviates by 5% from the measured current (see **Figure 1**). In this method, known as the match-point method, $V_T$ is determined from subthreshold slope measurements independent of tolerances in channel dimensions and extrinsic resistance.

## Mobility as a function of normal field

The surface mobility decreases as the field at the silicon surface increases [3–5]. Its dependence on normal field is determined by measuring the mobility as a function of gate voltage above threshold and solving Poisson's equation to define the field in silicon for each measurement.

• *Channel conductance method*

The surface mobility is commonly determined from measurements of drain current in the linear mode by the relationship

$$\mu_{EFF} \simeq \frac{I_D}{V_D}\left(\frac{L_{EFF}}{W_{EFF}}\right)\frac{1}{C_{OX}\left(V_G - V_T - \frac{V_D}{2}\right)}, \tag{2}$$

where $C_{OX}$ is the gate-oxide capacitance, and $V_D$, $V_G$ are the drain-to-source and gate-to-source voltages, respectively.

This method is satisfactory when the relative tolerance in device dimensions and the magnitude of extrinsic resistance are known or negligible. In the presence of high values of $R_{EX}$, the voltage drop outside the channel must be taken into account. Also, the magnitude of threshold voltage may increase due to the body effect. In this case, $V_G$ is replaced by $V'_G - I_D R_{EX}$ and $V_D$ by $V'_D - 2I_D R_{EX}$, where $V'_G$ and $V'_D$ are the externally applied gate and drain voltages, respectively.

A typical method of determining the extrinsic resistance and effective channel length is described in [6]. It consists in measuring the MOSFET resistance, which includes the channel and extrinsic resistances, in the linear mode on devices having the same channel width and different design channel lengths. The measurements are made for different gate voltages above threshold. The extrinsic resistance and $\Delta L$, the deviation in channel length from the design value, are found graphically or analytically from the intersection of the plots. A similar technique is used to find the deviation in channel width $\Delta W$. This method, however, assumes that $R_{EX}$, $\Delta L$, and $\Delta W$ are constant in a set of adjacent devices, and are independent of gate voltage. Our measurements on submicron devices show that this is not always the case (see **Figure 2**). It is evident that the plots cannot be approximated by single straight lines, and their intersection is not well defined; this precludes a unique definition of $R_{EX}$ and $\Delta L$.

• *Van der Pauw method*

We introduce a surface mobility measurement technique which uses an inversion-layer Van der Pauw structure, as illustrated in **Figure 3**. Details of the Van der Pauw structure can be found in [7, 8]. The structure allows the measurement of surface mobility as a function of normal field and temperature, for arbitrary extrinsic resistance and device dimensions. It comprises four diffusion tabs defined during source/drain diffusion, a gate electrode, and a substrate or well contact.

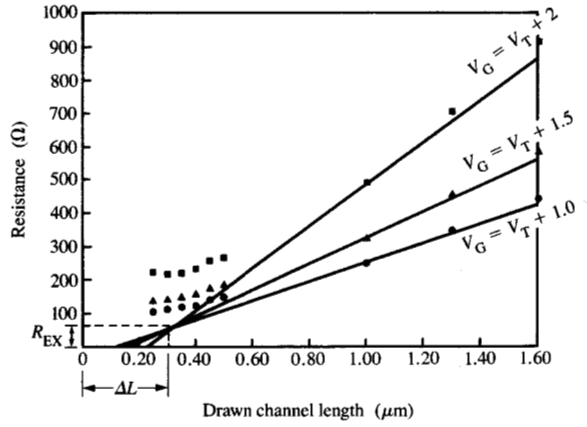


**Figure 2**

Determination of $R_{EX}$ and $\Delta L$ using the method described in Equation (6). The values obtained from the intersection are not uniquely defined in the submicron range.

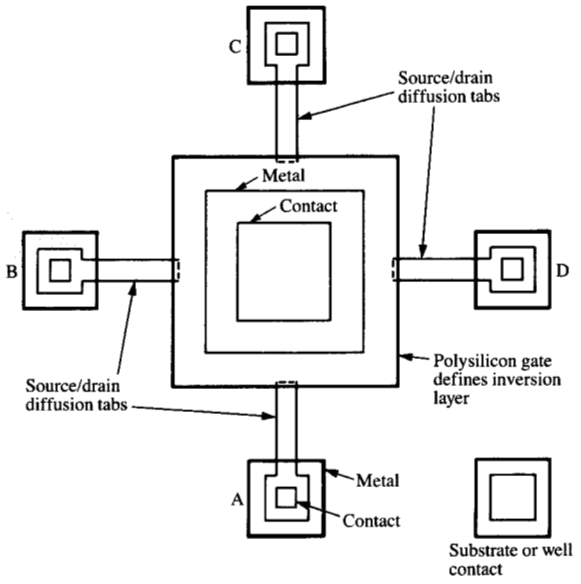


**Figure 3**

Inversion-layer Van der Pauw structure.

The threshold voltage is first measured using the match-point technique described above. The sheet resistance $R_S$ of the inversion layer is then measured as a function of gate voltage above threshold by forcing a current $\Delta I$ between two adjacent diffusions and measuring the voltage $\Delta V$ between the two other diffusions. The following well-known relationship holds for the sheet resistance:

$$R_S = \frac{\pi}{\ln 2}\left(\frac{\Delta V}{\Delta I}\right). \quad (3)$$

The effective surface mobility is determined from the calculated inversion-layer charge density $Q_{INV}$ and the measured sheet resistance:

$$\mu_{EFF} = \frac{1}{|Q_{INV}|R_S}. \quad (4)$$

## Extraction of $R_{EX}$, $L_{EFF}$, and transconductance

The effective surface mobility found from Van der Pauw measurements is used to determine the MOSFET extrinsic resistance, effective channel length, and transconductance for a given device.

- *Extrinsic resistance*

In the linear mode, the drain current may be approximated as

$$I_D = \gamma \frac{W_{EFF}}{L_{EFF}}\left(V'_G - V_T - \Delta V_T - \frac{V'_D}{2}\right)(V'_D - 2I_D R_{EX}), \quad (5)$$

where $\gamma = \mu_{EFF}C_{EFF}$, $C_{EFF} = (C_{OX}C_{INV})/(C_{OX} + C_{INV})$, and $\Delta V_T$ is the increase in threshold voltage due to the body effect. The inversion layer capacitance $C_{INV}$ is approximated from [9, 10]. Its effect, however, is negligible when $|V_G - V_T| \geq 2$ V and the gate-oxide thickness $t_{ox} \geq 15$ nm.

For all structures analyzed, it was found that the increase in threshold voltage $\Delta V_T$ due to the body effect was negligible in the linear but not in the saturation mode. In this case, the extrinsic resistance was found by taking the ratio of drain currents for two gate voltages,

$$R_{EX} = \frac{V'_D(K\Delta V_{G1} - \Delta V_{G2})}{2(K\Delta V_{G1}I_{D1} - \Delta V_{G2}I_{D2})}, \quad (6)$$

where $K = I_{D2}\gamma_1/I_{D1}\gamma_2$ and $\Delta V_G = V'_G - V_T - V'_D/2$. The subscripts 1 and 2 refer to the two applied gate voltages.

- *Effective channel dimensions*

To determine the effective channel length, measurements were made on a wide MOSFET where it could be assumed that the tolerance on $W_{eff}$ was negligible. The nominal width was determined from scanning electron microscope (SEM) measurements. The effective channel length was then found by substituting $R_{EX}$ from (6) into (5). Similarly, the effective channel width was found by

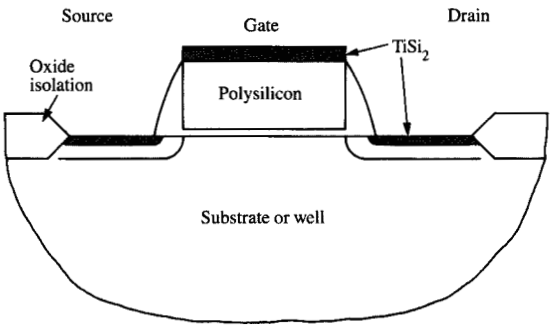


**Figure 4**

MOSFET cross section typical of CMOS-A and CMOS-B technologies.

**Table 1** Main features of two CMOS n-well technologies.

| *Parameter* | *CMOS-A* | | *CMOS-B* | |
|---|---|---|---|---|
| | *n-channel* | *p-channel* | *n-channel* | *p-channel* |
| $t_{ox}$ (nm) | 15 | 15 | 11 | 11 |
| $V_T$ (V) | 0.75 | −0.75 | 0.65 | −0.65 |
| Gate | n-type | n-type | n-type | p-type |
| $X_j$ ($\mu$m) | 0.40 | 0.45 | 0.15 | 0.15 |

**Table 2** Measured mobility parameters of two CMOS n-well technologies.

| *Parameter* | *CMOS-A* | | *CMOS-B* | |
|---|---|---|---|---|
| | *n-channel* | *p-channel* | *n-channel* | *p-channel* |
| $\mu_0$ | 433 | 193 | 356 | 90 |
| $\theta$ | 0.065 | 0.147 | 0.073 | 0.085 |

**Table 3** Extraction of $R_{EX}$, $L_{EFF}$, and $g_m$ (measurements made on p-channel MOSFETs in CMOS-B).

| $L_{DESIGN}$ ($\mu$m) | $R_{EX}$ ($\Omega$) | $L_{EFF}$ ($\mu$m) | $g'_m$ (ms/mm) | $g_m$ (ms/mm) |
|---|---|---|---|---|
| 5.00 | 168 | 5.058 | 9.38 | 9.54 |
| 2.00 | 141 | 2.069 | 21.50 | 22.35 |
| 1.00 | 129 | 0.711 | 48.96 | 53.90 |
| 0.80 | 154 | 0.758 | 45.83 | 51.78 |
| 0.65 | 125 | 0.601 | 55.70 | 64.50 |
| 0.50 | 164 | 0.429 | 66.70 | 85.38 |
| 0.35 | 112 | 0.266 | 91.67 | 117.90 |

characterizing a long MOSFET where the tolerance on channel length might be neglected.

- *Saturation transconductance*

When the device does not operate at scattering-limited velocity, the saturation transconductance per unit channel width is measured as

$$g'_m = \frac{1}{W_{EFF}} \left( \frac{\delta I_D}{\delta V'_G} \right). \tag{7}$$

The modulation of the effective channel length by the drain field and the effect of $R_{EX}$ on $\gamma$ were neglected for the bias voltage conditions used in this study. This was justified by two-dimensional simulations of the structures. The measured $g'_m$ was typically smaller than the intrinsic $g_m$ because of the voltage drops outside the channel. The ratio of intrinsic to measured transconductance is approximated by

$$\frac{g_m}{g'_m} \simeq \frac{V'_G - V_T}{V'_G - V_T - \Delta V_T - I_D R_{EX}}. \tag{8}$$

## Sample preparation

The samples were fabricated in two CMOS n-well technologies we call CMOS-A and CMOS-B. The main features of the technologies are summarized in **Table 1**.

The structures were fabricated on $p^+$ substrates upon which a 2–3-$\mu$m-thick p-type epitaxial layer was deposited. A buried channel was implanted in CMOS-A p-channel MOSFETs to adjust for the work function of the gate material. A MOSFET cross section which is typical for both technologies is shown in **Figure 4**. The Van der Pauw structures were comprised of 100-$\mu$m × 100-$\mu$m inversion layers with 1-$\mu$m tab widths. For $\Delta L$ measurements, the MOSFETs were designed with a 20-$\mu$m channel width and channel lengths varying from 0.25 $\mu$m to 20 $\mu$m; the nominal channel width was determined from SEM measurements as $W_{EFF} \simeq 19.4$ $\mu$m. For $\Delta W$ measurements, the channel length was 20 $\mu$m, and the width was varied from 0.8 $\mu$m to 20 $\mu$m; the nominal channel length was determined from SEM measurements as 19.8 $\mu$m. The polysilicon gates were defined in photolithography for CMOS-A and in e-beam lithography for CMOS-B.

## Results

The results obtained for surface mobility as a function of gate voltage above threshold and temperature in the range 297 K to 473 K are summarized for CMOS-A in **Figure 5**. The following semi-empirical relation is used to approximate the surface mobility [5]:

$$\mu_{EFF} \simeq \frac{\mu_0}{1 + \theta(|V_G - V_T|)}, \tag{9}$$

where $\mu_0$ and $\theta$ are extracted from measurements; a suggested model for their physical interpretation is described in the Appendix.

The temperature dependence of $\mu_0$ is approximated from Figure 5 for n-channels as

$$\mu_{0T} \simeq \mu_0(297)\left(\frac{T}{297}\right)^{-1.74}, \quad (10)$$

and for p-channels as

$$\mu_{0T} \simeq \mu_0(297)\left(\frac{T}{297}\right)^{-1.21}. \quad (11)$$

Similar results were found for CMOS-B. **Table 2** summarizes the measured room-temperature values of $\mu_0$ and $\theta$ for the two technologies. The effective mobilities are smaller in CMOS-B than in CMOS-A. This is caused by the difference in the gate oxide thickness and channel impurity profile, as discussed in the Appendix. The larger difference in the p-channel mobility is caused by the p-type buried layer present in CMOS-A (n-type gate, buried channel) but not in CMOS-B (p-type gate, surface channel).

The MOSFET drain current is measured in the linear mode at $|V'_D| = 0.2$ V and $|V'_G - V_T| = 2$ V and 3 V. In the saturation mode the bias conditions were $|V'_D| =$ 3.4 V and $|V'_G| = 3.0$ and 3.1 V. The substrate or well was maintained at ground potential. The saturated transconductance was measured for $V'_D = 3.4$ V and $\delta V'_G = 0.1$ V.

Values for $R_{EX}$, $L_{EFF}$, and $g_m$ obtained for p-channel structures in CMOS-B at 297 K are shown in **Table 3**. The corresponding values for $\gamma$ are found from Van der Pauw measurements as $\gamma_1 = 27.13$ $\mu$S/V and $\gamma_2 =$ 25.70 $\mu$S/V. It can be seen from the table that the structures exhibit a large extrinsic resistance that varies between 2.2 k$\Omega$-$\mu$m and 3.3 k$\Omega$-$\mu$m. It was also found that $\Delta L$ is not constant but varies between $-0.069$ $\mu$m and $+0.29$ $\mu$m. Finally, the table shows an increasing difference between measured and intrinsic transconductance as the channel length is decreased. This is caused by an increase in the ratio of extrinsic to channel resistance.

Similar results were obtained for CMOS-A and for n-channel structures in both technologies.

## Conclusions

A technique which uses a specially designed Van der Pauw structure was introduced to measure electron and hole mobilities in an inverted silicon surface as a function of normal field and temperature. A new definition of threshold voltage is introduced, which allows the method to measure surface mobility, independent of variations in channel size and resistance outside the channel, referred to here as the extrinsic resistance.

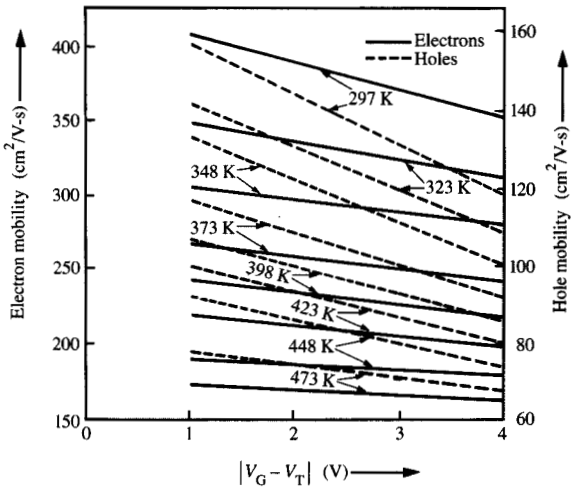


**Figure 5**

Electron and hole surface mobilities as a function of $|V_G - V_T|$ for $|V_D| = 0.2$ V (temperature as parameter).

The measured mobility and threshold voltage were used to extract the extrinsic resistance, effective channel dimensions, and intrinsic transconductance in submicron n-channel and p-channel MOSFETs. The method was successfully demonstrated on submicron MOSFETs fabricated in CMOS technologies having different gate oxide thicknesses and channel impurity profiles. The surface mobility as a function of gate voltage above threshold was approximated in terms of two parameters ($\mu_0$ and $\theta$), which were determined empirically. A model was suggested to relate the two parameters to the gate oxide thickness, channel impurity profile, and temperature.

## Appendix: Model for dependence of mobility on normal field

The dependence of surface mobility on gate voltage above threshold is given in Equation (9) as

$$\mu_{EFF} \simeq \frac{\mu_0}{1 + \theta(V_G - V_T)}, \quad (A1)$$

where $\mu_0$ and $\theta$ are determined empirically [5]. In this section we suggest a model that relates $\mu_0$ and $\theta$ to the oxide thickness, channel impurity profile, and temperature. We begin with the following assumption on

the degradation of surface mobility due to normal field:

$$\frac{1}{\mu_{EFF}} \simeq \frac{1}{\mu_L} + \frac{1}{\mu_I} + \frac{1 + C_1|E_{Si}|}{\mu_S}, \quad \text{(A2)}$$

where

$\mu_L$ = lattice-limited mobility,
$\mu_I$ = impurity-limited mobility,
$E_{Si}$ = normal field at the silicon surface,
$\mu_S$ = surface-scattering-limited mobility extrapolated to $E_{Si} = 0$.

In this analysis it is assumed that for a given process technology, $C_1$ is constant and $\mu_S$ depends only on temperature. $C_1$ and $\mu_S$ are determined empirically. Equation (A2) may be rewritten as

$$\mu_{EFF} \simeq \frac{\mu_S}{1 + \frac{\mu_S}{\mu_B} + C_1|E_{Si}|}, \quad \text{(A3)}$$

where

$$\frac{1}{\mu_B} \simeq \frac{1}{\mu_L} + \frac{1}{\mu_I}. \quad \text{(A4)}$$

In [11], $\mu_I$ is defined as

$$\mu_I = \frac{AT^{1.5}}{N_I \ln\left(1 + \frac{BT^2}{N_I^{2/3}}\right)}, \quad \text{(A5)}$$

where $A$ is a constant that depends on the carrier effective mass, $T$ is the temperature in K, $N_I$ is the ionized impurity concentration at the silicon surface, and $B$ is expressed in terms of universal constants as

$$B = \left(\frac{3\varepsilon_{Si}k}{q^2}\right)^2 \simeq 2.81 \times 10^6 \text{ cm}^{-2}\text{-K}^{-2}, \quad \text{(A6)}$$

where $\varepsilon_{Si}$ is the dielectric constant of silicon and $k$ is the Boltzmann constant. From independent measurements on specially designed structures, we find $A \simeq 1.5 \times 10^{16}$ for electrons and $A \simeq 7.3 \times 10^{15}$ for holes. The lattice-scattering-limited mobility is given by [12] as

$$\text{(electrons) } \mu_L \simeq 2.1 \times 10^9 T^{-2.5} \text{cm}^2/\text{V-s} \quad \text{(A7)}$$

and

$$\text{(holes) } \mu_L \simeq 2.3 \times 10^9 T^{-2.7} \text{cm}^2/\text{V-s}. \quad \text{(A8)}$$

We now rewrite (A3) as

$$\mu_{EFF} \simeq \frac{\mu_{max}}{1 + C_2|E_{Si}|}, \quad \text{(A9)}$$

where

$$\mu_{max} = \frac{\mu_B\mu_S}{\mu_B + \mu_S}$$

and

$$C_2 = \frac{C_1\mu_B}{\mu_S + \mu_B}.$$

The electric field in silicon $E_{Si}$ is approximated from [3] as

$$E_{Si} = \frac{Q_B + \frac{Q_{INV}}{2}}{\varepsilon_{Si}}, \quad \text{(A10)}$$

where $Q_B$ is the bulk charge density which is found by solving Poisson's equation for a given channel profile. The inversion charge density is approximated as

$$Q_{INV} = C_{OX}(V_G - V_T). \quad \text{(A11)}$$

Equation (A9) is finally rewritten in the form of Equation (A1), with

$$\mu_0 = \frac{\mu_{max}}{1 + \frac{C_2|Q_B|}{\varepsilon_{Si}}} \quad \text{(A12)}$$

and

$$\theta = \frac{C_2C_{OX}}{2(\varepsilon_{Si} + C_2|Q_B|)}. \quad \text{(A13)}$$

When substituted into Equation (A1), Equations (A11) and (A12) allow the prediction of surface mobility as a function of oxide thickness, temperature, and channel impurity profile.


## Acknowledgments

We thank G. Gravenites for the design and initial characterization of the inversion layer Van der Pauw structure, N. Jones for successfully carrying out the experiments, and the advanced technology group at IBM, Essex Junction, Vermont, for preparing the samples. Discussions with M. Wordeman of the IBM Thomas J. Watson Research Center are greatly appreciated.


## References


1. H. I. Hanafi, L. H. Camnitz, and A. I. Dally, "An Accurate and Simple MOSFET Model for Computer-Aided Design," *IEEE J. Solid State Circuits* **SC-17,** 882 (1982).
2. S. C. Sun and J. D. Plummer, "Electron Mobility in Inversion and Accumulation Layers on Thermally Oxidized Silicon Surfaces," *IEEE Trans. Electron Devices* **ED-27,** 1497 (1980).
3. A. S. Sabnis and J. J. Clemens, "Characterization of the Electron Mobility in the Inverted ⟨100⟩ Silicon Surface," *1979 IEDM Tech Digest*, p. 18 (1979).
4. K. Yamaguchi, "Field-Dependent Mobility Model for Two-Dimensional Numerical Analysis of MOSFETs," *IEEE Trans. Electron Devices* **ED-26,** 1068 (1979).
5. K. Y. Fu, "Mobility Degradation Due to Gate Field in the Inversion Layer of MOSFETs," *IEEE Trans. Electron Device Lett.* **EDL-3,** 292 (1982).
6. J. Chern, P. Chang, R. Motta, and N. Godinho, "A New Method to Determine MOSFET Channel Length," *IEEE Electron Device Lett.* **EDL-1,** 170, 1980.

7. L. J. Van der Pauw, "A Method for Measuring Specific Resistivity and Hall Effect of Disc of Arbitrary Shape," *Phillips Res. Repts.* **13,** 1 (1958).
8. W. R. Tonti, "Field and Temperature Dependence of Surface Mobility," Ph.D. Dissertation, University of Vermont, Burlington, Vermont, 1987.
9. G. Baccarani and M. R. Wordeman, "Transconductance Degradation in Thin Oxide MOSFETs," *1982 IEDM Tech. Digest,* p. 278 (1982).
10. M. S. Liang, J. Y. Choi, P. K. Ko, and C. Hu, "Inversion-Layer Capacitance and Mobility of Very Thin Gate-Oxide MOSFETs," *IEEE Trans. Electron Devices* **ED-33,** 409 (1986).
11. E. M. Conwell, "Properties of Silicon and Germanium," *Proc. IRE* **40,** 1327 (1952).
12. G. W. Ludwig and R. L. Watters, "Drift and Conductivity Mobility in Silicon," *Phys. Rev.* **101,** 1699 (1956).

*Received May 26, 1989; accepted for publication September 4, 1989*

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