Internal probing of submicron FETs and photoemission using individual oxide traps

by Phillip Restle
Antonio Gnudi

In submicron field-effect transistors with channel area less than 0.5 μm^2, the capture or emission of a single electron (or hole) in the gate oxide has an easily observable effect on the device resistance. Measurements are described in which the time and amplitude of the resistance change due to each capture and emission event from an individual trap are extracted to obtain the average capture and emission times, and the amplitude of the resistance change, at different temperatures, device biases, and light intensities. Techniques are described for using the data at different biases to characterize the trap, find the location of the trap in the device, and then use the trap as a probe of the oxide field (or surface potential) and the surface charge density within a 5–50-Å radius of the trap. In some devices a single trap can be resolved over almost all designed bias regions of the FET near room temperature. In effect, individual traps can be used as internal probes into VLSI devices of the present and future. Results from 2D computer device modeling of these devices are used to evaluate and understand these techniques. Methods for applying these techniques to the study of device degradation are discussed. Data are presented in which photoemission is observed from a single electron trap.

Introduction

With recent advances in VLSI processing, we have reached the point at which the effect of a single electron on a typical device can be quite significant. While such effects will eventually cause fundamental scaling and reliability problems, parallel advances in physics have helped create opportunities for extracting new kinds of information about VLSI devices by observing single-electron trapping effects.

After an introduction from the more historical perspective of low-frequency noise, a general discussion of the trapping mechanism in field-effect transistors (FETs) is included. In fact, very few assumptions are needed to extract several different kinds of useful device

information from the observed trapping signals, and these assumptions are identified in later sections as they are used in the analysis. The experimental techniques and computer analysis of the trapping signal data are then described, as well as some complications encountered in specific noise traces.

Using these techniques, we can extract three parameters for a single trap from each noise trace: the average capture time, the average emission time, and the device resistance change or signal amplitude of a trapping event. We then proceed to use these results from different bias conditions to extract information about the trap and the device. First we *calibrate* the trap as a probe of the internal device potentials using capture and emission time data from the simplest (linear) region of device operation. Then we find the trap location, taking advantage of the device symmetry. At this point the trap is used as a voltage probe inside the device, with known location. Finally, the amplitude of the trapping signal is used to measure the change in device resistance caused by a single trap under different bias conditions. This information is directly applicable to studies of device degradation. This is followed by observations of photoemission from a single trap, and conclusions.

Using noise

Low-frequency noise, often with a power spectrum proportional to 1/frequency ($1/f$ noise), has always been a problem in conductors and electronic devices, and continues to be so. Recently, however, the understanding of these noise sources has progressed to the point where this noise can be used as a tool to understand physical phenomena and practical devices. For recent reviews, see [1, 2].

One reason for the recent advances is the fabrication of small-size samples, in which the individual events causing the noise become important. The observation of random telegraph signal (RTS) noise in FETs (as in Figure 3, shown later) by Ralls et al. [3] inspired a number of experiments and successful models for understanding $1/f$ noise and FET trapping kinetics in detail. Methods were developed by several groups [3–5] to extract the trap energy and cross section, the trap barrier energy or activation energy, and the distance of the trap from the silicon–oxide interface for individual traps. Similar RTS noise (or "burst noise") has been studied in a number of other structures, including silicon diodes [6], tunnel diodes [7], dc SQUIDs [8, 9], and scanning tunneling microscope studies of very thin oxides on silicon [10]. Single-trap emission has been studied in an extension of deep-level transient spectroscopy (DLTS) for micrometer-size devices [11].

This paper is an extension of previous work [12] which shows the feasibility of using these well understood and characterized traps as fortuitous stationary probes inside normally processed submicron FETs. These devices are typical of advanced VLSI processes for CMOS logic and memory. Except for results with limited resolution from voltage-contrast scanning microscopy of cleaved structures, it has always been difficult to make localized internal measurements inside operating, fully processed devices. Ironically, it is the continued shrinking of devices that makes individual trapping events observable, so that the internal probing techniques presented in this work become possible. While an accurate two- or three-dimensional numerical computer model is an important tool, advanced devices will always challenge modeling efforts, and the ability to make detailed internal measurements inside operating devices will aid design and modeling efforts.

Trapping mechanism

After Ralls et al. [3], several groups reported RTS noise in small FETs [13–15]. The switching times are random, while the amplitude of the resistance change is a constant for a particular trap when a simple RTS is observed. Most researchers have identified these random two-state systems with oxide traps close enough to the silicon to communicate with the conduction electrons in the silicon inversion layer. The recent review by Kirton and Uren [2] contains a thorough discussion of this topic. In the present work, it was observed that the time in the high-resistance state always increased when the magnitude of the gate voltage was increased above threshold, and the time in the low-resistance state always decreased (in contrast to the findings of Ralls et al. [3]). This is consistent across about 70 n-channel devices and 10 p-channel devices near room temperature. Kirton and Uren also stress this result for their n-channel device measurements near room temperature. Since increasing the gate voltage above threshold is expected to increase the rate of capture of inversion layer carriers and reduce the rate of emission from oxide traps, this suggests that the high-resistance state always corresponds to an occupied trap at some distance from the silicon–oxide interface near room temperature. No definite identification has been made between a particular defect and this noise. A somewhat featureless distribution of trap energies, activation energies, and locations for these traps is observed, consistent with the $1/f$ noise spectrum typically measured in larger devices. An unambiguous defect identification is difficult due to the glassy nature of the oxide; in fact, the density of all controllable defects must be reduced as much as possible in these devices for individual traps to be observable at all.

The amplitude of the resistance change due to trapping events is qualitatively consistent with the amplitude expected due to the change in the number of conduction

electrons [3, 13]. However, there is a large variation of this amplitude even between different traps in the same device which is not explained by this simple model. Narrow-channel, short-channel, and surface roughness effects can create nonuniformities in the device that may explain this variability. In addition, data from cross-shaped silicon-on-sapphire resistors in magnetic fields imply a reduction in surface mobility correlated with the decrease in the number of carriers [16]. Since the resistance always increased upon carrier capture in this work, any mobility change due to capture must be small or always negative. This kind of detailed information can be used to improve existing $1/f$ noise models for devices [17].

Both capture and emission times are thermally activated near room temperature, but these times are often longer than expected tunneling times for these traps near the Si–SiO_2 interface. In addition, the trapping times are much less sensitive to the effective electron temperature than to the lattice temperature [18]. This suggests that there is a transition state involving rearrangement of both the electron and the atoms near the trap [19]. Atomic rearrangement such as a softening of the lattice near the occupied trap is also suggested by a change in entropy upon trapping found to be necessary in the model of Kirton and Uren [5].

The possibility of using traps to study devices was suggested by the observed strong dependence of the capture and emission times on the gate voltage. We follow a simplified version of the model of Kirton and Uren [5]. Using a simple trapping model and standard FET analysis, the capture and emission times are given by

$$\langle \tau_c \rangle = \frac{1}{\sigma_0 v n} e^{\Delta E_B / k_B T}, \quad (1)$$

$$\langle \tau_e \rangle = \frac{1}{g \sigma_0 v N_c} e^{(\Delta E_B + \Delta E_{CT})/k_B T}, \quad (2)$$

where τ_c is the trap capture time, τ_e is the emission time, σ_0 is the trap cross-section prefactor, v is the RMS (root-mean-square) thermal velocity, n is the mean electron density in the inversion layer, g is the trap degeneracy factor, N_c is the effective density of states in the conduction band, k_B is Boltzmann's constant, and T is the temperature. The energy terms refer to the energy of the trap and electron system: ΔE_B can be interpreted as a capture barrier energy, and ΔE_{CT} refers to the additional energy required to move the electron from the trap to the conduction band.

Note that the capture time depends inversely on the number of carriers in the inversion layer, and exponentially on the capture barrier energy ΔE_B. The emission time, on the other hand, does not depend directly on the charge density in the inversion layer in this simple model. This model was initially used by Kirton and Uren to explain trapping kinetics at constant gate voltage and different temperatures. The effect of changing gate voltage is not completely understood, especially near threshold. The main modifications necessary to model different gate voltages are to include a gate-voltage dependence in the barrier energy terms, ΔE_B, ΔE_{CT}, and σ_0. The simplest effect is due to the change in potential at the trap location due to the change in potential across the gate oxide. Thus the trap-to-conduction-band energy ΔE_{CT} should include a term describing the electric potential at the trap location due to the average electric field in the oxide: $eE_{ox}d_t$, where e is the electron charge, E_{ox} is the vertical electric field in the gate oxide, and d_t is the distance of the trapped electron from the silicon surface. Kirton and Uren [2] have also found that the cross section σ_0 and the entropy change due to trapping seem to have a significant gate-voltage dependence.

For most of this work, a detailed understanding of the trapping mechanism is not required. Certain assumptions about the trapping kinetics that are necessary for the analysis are discussed as needed. Note that these devices do not exhibit quantum coherence phenomena near room temperature (the region considered in this work); these become important in silicon FETs at low temperatures [20].

Effective trap size

A question arises as to the effective "size" of a trap when it is used as a stationary probe in a FET. In fact, three characteristics are extracted from the RTS signal of the trap: the average emission time, the average capture time, and the amplitude of the resistance change. Each one of these variables may have a different characteristic size when it is used to probe the FET. Electrons cannot tunnel through more than 5 or 10 Å of oxide in the trapping times measured, so the capture time probably samples a region of the device with approximately this radius. The emission time depends primarily on the oxide field between the trap location and the silicon; thus, the emission time probes a region of size d_t, which appears to be between 5 and 20 Å for these traps. This length scale may be slightly different from the capture-time length scale, since the rate-limiting mechanism is not simple tunneling. Finally, a trapped charge perturbs the inversion layer in a region with radius approximately equal to the screening length in the inversion layer (typically 5–50 Å, depending on gate voltage), or the trap distance from the silicon, whichever is larger. Thus, the relevant length scale in discussing the RTS amplitude as a device probe is the screening length or d_t, whichever is larger. Because these sizes tend to scale somewhat with

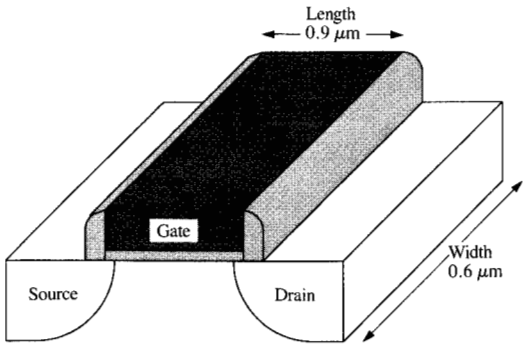

Figure 1

Schematic diagram of device A.

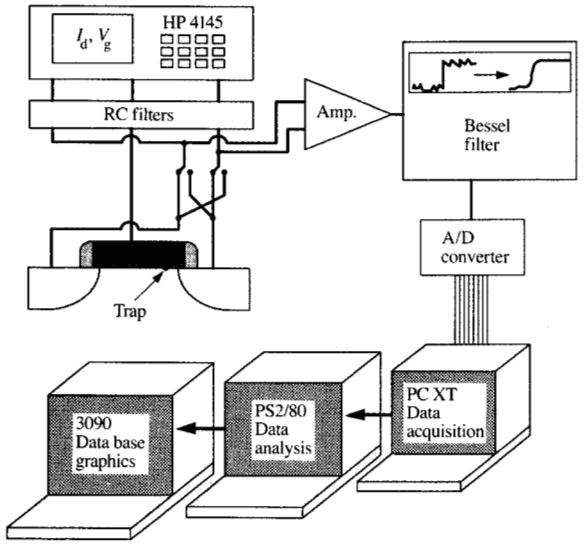

Figure 2

Schematic diagram of experiment.

the device dimensions (such as oxide thickness), these *probes* should not become too large in the near future.

Experiment

The silicon FETs were fabricated by the IBM Research Division, Thomas J. Watson Research Center Silicon Facility. The devices used in this study were from half-micron (devices A and C) and quarter-micron (device B) CMOS technologies. Device A (see **Figure 1**) had length 0.9 μm, width 0.6 μm, oxide thickness 125 Å, and threshold voltage 0.36 V; an arsenic–phosphorus lightly doped drain (LDD) process was used. Device B had length 0.2 μm, width 2.0 μm, oxide thickness 70 Å, and threshold voltage 0.23 V. Device C had length 0.4 μm, width 2.2 μm, oxide thickness 110 Å, and threshold voltage 0.15 V. Other devices showed similar results, but most were not studied in such detail. A number of devices were screened to find devices in which a single trap was easily observed over a wide bias region. The fraction of usable devices was generally greater for smaller device dimensions.

Devices were biased at constant gate voltage V_{gs}, drain current I_d, and substrate bias V_{sub}. When the channel resistance of the device changed by ΔR, the drain voltage changed by $\Delta V_{ds} = \Delta R \times I_d$.

The measurement system (**Figure 2**) consists of a Temptronics temperature-controlled wafer chuck on a Rucker and Kolls 666 manual probe station, a Hewlett-Packard 4145A Semiconductor Parameter Analyzer with external RC filters to supply quiet dc biases, Ithaco 1201 low-noise preamplifiers, and a Frequency Devices 9016 filter system with 8-pole Bessel low-pass anti-alias filters. Drain voltages were sampled with a Scientific Solutions Inc. Labmaster by an IBM PC XT, allowing over 20 000 consecutive drain-voltage measurements with 12-bit resolution at up to 20 kHz.

Bessel filters were chosen for minimum overshoot in the response function, to eliminate the overestimation of step-function amplitudes caused by sampling at peaks in a ringing response function. The corner frequency of the Bessel filters was set to 0.7 times the sampling rate, so that the 0.5%–99.5% rise time of the filter is less than the sampling period. This guarantees less than 1% systematic error when measuring a step amplitude, while filtering out as much high-frequency noise as possible.

Because of the inevitable background noise and the random nature of the capture and emission process, a large amount of resistance fluctuation data must be analyzed automatically to make these measurement techniques useful. Without an efficient data analysis algorithm, the analysis time becomes much longer than the data acquisition time. The most time-consuming task is to accurately determine the time and amplitude of each step in drain voltage caused by the trapping events of a particular trap in the device. This is complicated by the fact that, inevitably, in some regions of device operation, the steps of interest are almost obscured by other noise sources in the device, including other traps with both larger and smaller step amplitudes. The following algorithm was developed to extract the desired trapping events from many time series of voltage measurements

$\{V_i, i = 1, 2, \cdots 20\,000\}$. First the difference function $D_i = V_i - V_{i-2}$ is calculated. To eliminate measurements made during the filter rise time, all elements D_i that are less than either D_{i-1} or D_{i+1} are then eliminated. For accurate measurements, the sampling period must be less than 2% of the average trap times, so at least 95% of the elements D_i do not describe steps and can be eliminated at this point for computation efficiency. To accomplish this, a search is made for a D_{crit} so that 90–95% of $D_i < D_{crit}$, and these D_i are eliminated. To identify which of the remaining D_i describe the time and amplitude of the relevant trapping events, we note that an increase in resistance, or "up" step, cannot be followed by another up step (if the steps are from one trap), and the same is true for down steps. A search is done to find the range $D_{min} \rightarrow D_{max}$ that maximizes the number of consistent trapping events found with step amplitudes in this range while minimizing the number of up–up and down–down errors. This algorithm was implemented in the C language on an IBM PS/2 Model 80 and takes 3.8 seconds to process a time series of 20 000 measurements. Approximately 10^8 samples have been analyzed using this algorithm.

A single device was typically studied at several temperatures, gate voltages, drain voltages, and voltage sampling rates, all under computer control; approximately 10^5 drain-voltage measurements were recorded under each set of conditions. Several sampling frequencies were used in each case, so that at least one time series would cover a large number of trapping events with sufficient time resolution. Since constant drain-current biasing was desired at specified average drain voltages, a search routine was used to find the bias current to produce each drain voltage desired.

Trapping noise traces

Figure 3 shows typical resistance fluctuations from device A at several drain voltages. Each trace shows step-increases in channel resistance due to the capture of an electron in an interface state in this n-channel FET, and step-decreases of the same amplitude when the electron leaves the trap, as discussed above in the trapping mechanism section. The background noise is partly thermal noise and partly due to other traps in or near the channel of the device that give a smaller signal, either because the device is not as sensitive to trapped charge at their location, or they have faster trapping kinetics and are partially filtered out. Both fast traps and thermal noise produce "white," or frequency-independent, noise power in the experimental bandwidth.

A number of devices with these dimensions were screened to find devices in which a single trap is the dominant noise source throughout the bias and temperature regions of interest, so that more than 95%

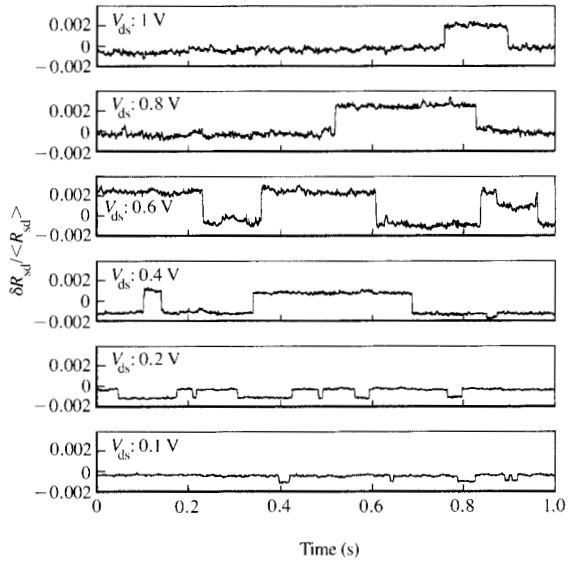

Figure 3

Fractional resistance fluctuations from the mean for device A, with $V_{gs} = 1.0$ V, at different drain voltages.

(usually 100%) of the capture and emission events for a single trap could be successfully resolved using the analysis software.

In some of the quarter-micron CMOS devices studied, the capture and emission events from a single trap were observable over most of the operating region above the threshold voltage.

Non-RTS signals

In a few percent of the FETs studied, more complicated noise signals were observed from traps or interacting trap systems with more than two states [14, 21, 22]. Although these devices were not used in this work, information about the physical extent and orientation of these multiple-state systems might be obtainable by studying the kinetics as a function of both vertical and horizontal fields in these devices. In one case, a small fraction of the data taken on a trap was slightly inconsistent with the rest of the data, probably as a result of a weak interaction with another very slow trap in the same region of the device. The trap density is low enough in these devices that trap interactions of this sort are a rare occurrence.

In the usual case where there are no significant interactions with other traps in the device, the capture and emission times are found to be exponentially distributed, which is consistent with the simplest two-

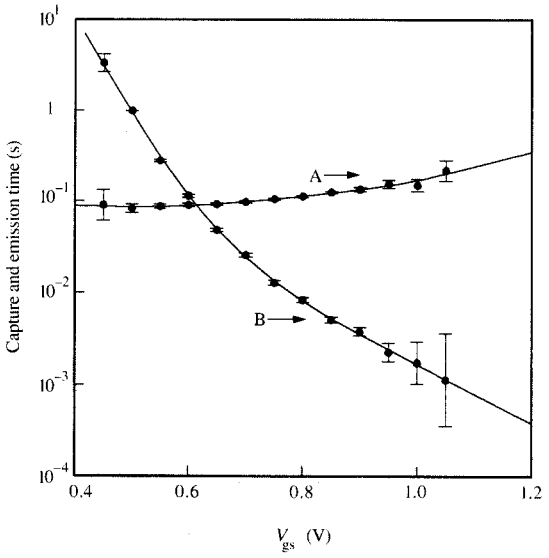

Figure 4

Average emission time (curve A) and capture time (curve B) for device A with small source–drain voltage. The lines are cubic-spline fits to the data, and are used as the calibration functions F_{τ_c} and F_{τ_e} for this particular trap.

state model in which the probability of capture in a time element dt is determined by a constant capture rate $P(t)dt = (dt/\tau_c)$. For this distribution, the mean and standard deviation are equal. Since, for multiple-state or interacting traps, the mean and standard deviation of the capture (or emission) times are not expected to be equal, this was used in practice as a test to screen for more complicated signals or data analysis errors.

In the simple two-state traps used in this work, the mean capture time τ_c, the mean emission time τ_e, and the step amplitude completely describe the noise from the trap of interest. In this case, the fractional uncertainty (one standard deviation) for the mean capture and emission times is given by

$$\frac{s_{\overline{\tau}_c}}{\overline{\tau}_c} = \frac{s_{\overline{\tau}_e}}{\overline{\tau}_e} = \frac{1}{\sqrt{N_{\text{events}}}}, \tag{3}$$

where $\overline{\tau}_c$ and $\overline{\tau}_e$ are the sample means of the capture and emission times measured, respectively, $s_{\overline{\tau}_c}$ and $s_{\overline{\tau}_e}$ are the sample standard deviations of the mean capture and emission times, respectively, and N_{events} is the number of individual capture times or emission times averaged.

Calibrating the trap

The first step in using traps as probes is to "calibrate" the probe using the simplest region of device operation: the linear region where $V_d \ll V_g - V_{th}$. **Figure 4** shows the average capture and emission times vs. gate voltage with small V_{ds}. Figure 4 is the key to further analysis. Since these data are taken with the entire channel in strong inversion and with V_{ds} small to minimize complicating longitudinal fields, we have simple accurate models for the device in this region. Since for this trap the capture time is very sensitive to the gate voltage in Figure 4, the trap is very sensitive to the changing fields and charge densities near the trap location, as described by Equation (4).

For the trap studied in device A, the emission time was relatively insensitive to the oxide field (see Figure 2), and was not used in further analysis. This trap in device A is probably very near the silicon–oxide interface, so that the trap potential (and thereby the emission time) changes little with changes in oxide field. In sample B, both capture and emission times were sensitive to the gate voltage, and were useful as probes [compare Figure 4 and Figure 9(a), shown later].

It is not necessary at this point to have an accurate and complete physical model for the data in Figure 4. For the present purposes we simply fit the data with a cubic spline function. With some assumptions and approximations about the trap capture and emission mechanisms in FETs, we can start extracting information about the trap location and device operation with little *a priori* knowledge. We now make the simple approximation that in the linear region the capture and emission times are determined by the quasi-Fermi potential difference between the gate and the inversion layer below the trap. Since the emission time is expected to be determined largely by the oxide field, this is more accurate for the emission time. But in strong inversion with small V_{ds}, where the drift field and the depletion capacitance are relatively unimportant, the inversion layer charge density, and thus the capture time, is also determined by this potential difference. This makes it useful to define the functions F_{τ_c} and F_{τ_e}:

$$V_{gs} - V_{ts} = F_{\tau_c}(\tau_c), \tag{4}$$

$$V_{gs} - V_{ts} = F_{\tau_e}(\tau_e), \tag{5}$$

where V_{ts} is the quasi-Fermi potential difference between the source and the inversion layer below the trap. The interpretation of V_{ts} in terms of quasi-Fermi potentials as opposed to the silicon surface potential is discussed below. In defining these functions, we assume that the trapping times are determined completely by the *local* potential difference between the inversion layer and the gate. Conversely, by measuring either the capture or the emission time, we immediately obtain V_{ts} (since V_{gs} is known). This is the key to using these traps as probes of local potential. The functions F_{τ_c} and F_{τ_e} are determined

empirically by fitting cubic spline functions to the average capture and emission times measured in Figure 4. Note that for the data in Figure 4, V_{ds} is small, so V_{ts} is also small and can be neglected in Equations (4) and (5) when obtaining the functions F_{τ_c} and F_{τ_e} from Figure 4. Then, for any gate and drain biases for which the average capture time or emission time can be measured, and for which Equations (4) and (5) are good approximations, we can determine V_{ts}. At large drain voltages ($V_{ds} > V_g - V_{th}$), as discussed below, Equation (4) is no longer valid because the local charge density and capture time are determined by *local* potentials alone.

In summary, the data in Figure 4 (obtained where V_{ts} is negligible) are used to obtain the functions F_{τ_c} and F_{τ_e} in Equations (4) and (5). Then, for other device biases τ_e or τ_c is measured, giving us the trap-to-source potential V_{ts}.

Using the device symmetry

Since the devices studied are macroscopically symmetrical, the source and drain connections can be switched, so that a single trap (if not in the center of the device) can be used to probe both near the source and near the drain. The two possible orientations will be arbitrarily defined as the "forward" and "reverse" orientations. **Figure 5** shows a schematic diagram of device A under both device orientations. These bias connections were made by computer-controlled relays in the experiment. The ability to use a single trap near either the source or the drain is quite valuable, because the results are not complicated by any differences between traps or devices. This symmetry is exploited in much of the analysis below.

Finding the trap location

An important element of these techniques is to find the location of the trap in the device, using the fact that the applied drain voltage (V_{ds}) affects the trap in a manner which depends on its position in the device. Again we use the simple linear region with small V_{ds}. The following technique for trap position determination is generalized from the technique outlined previously [12]. If the trap is near the drain, applying a small drain voltage decreases both the charge density and the gate oxide potential near the trap location. Thus, both the capture and emission times are affected. If the trap is near the source, a small drain voltage has almost no such effect. We define a potential ratio

$$X = V_{ts}/V_{ds}, \tag{6}$$

so that X is the fraction of the source drain potential that appears between the source and the trap. For small drain voltage and higher gate voltage, the quasi-Fermi potential varies linearly with position between the source and the drain. For these conditions X is a good measure of the physical location of the trap in the device,

$$X \simeq L_{ts}/L_{ds}, \tag{7}$$

where L_{ts} is the horizontal distance from the source to the silicon oxide interface below the trap, and L_{ds} is the device channel length. The four combinations which use the capture and emission times and the forward and reverse orientations should yield the same trap location if the approximations are valid. The number of trapping events averaged and the error in the calibration functions (Figure 4) limit the accuracy of V_{ts} obtained from Equation (4). Since the accuracy of X is determined by the fractional error in V_{ts}, greater statistical accuracy is obtained by increasing V_{ds}, as long as the linear channel approximation and the assumptions leading to Equation (4) remain valid. In the measurements described below, drain biases of 0.10 V and 0.20 V were used in the measurements at higher gate voltage, and 0.05 V was used for the lower gate voltages.

Figure 6 shows the ratio V_{ts}/V_{ds} (or X) as a function of gate voltage, and shows that this ratio varies with gate voltage. The curves in Figure 6 are discussed subsequently. Since the trap position should not depend on gate voltage, we must determine the cause of this gate-voltage dependence. The explanation involves a short-channel phenomenon important for devices of these dimensions. For the limit of small V_{ds}, the linear channel approximation is often used where the quasi-Fermi

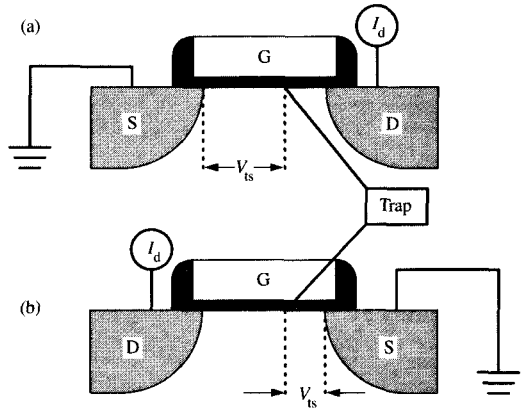

Figure 5

Schematic diagram of device A, showing the trap location and the changing source and drain definitions for the two device orientations: (a) forward; (b) reverse.

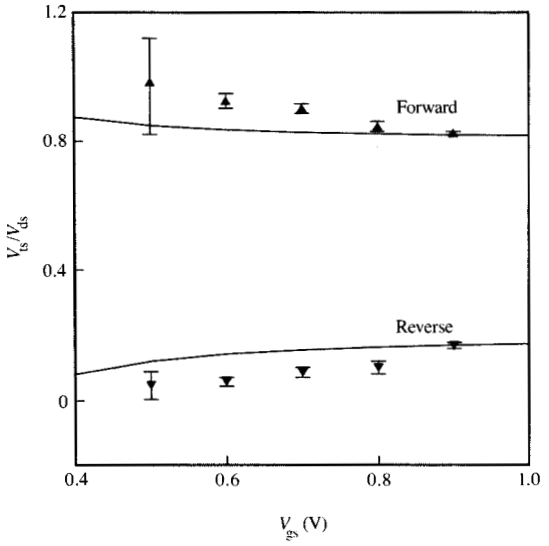

Figure 6

Trap-to-source potential/drain-to-source potential vs. gate voltage for device A, for both forward and reverse orientations, in the linear region of device operation. The solid lines are results from a two-dimensional computer device model.

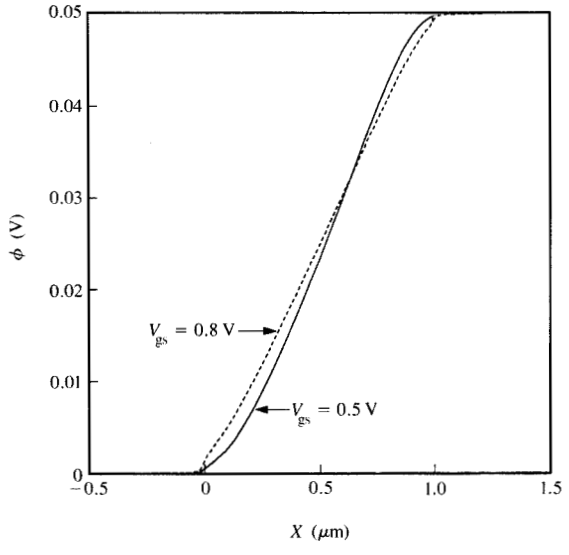

Figure 7

Quasi-Fermi potential for electrons at the silicon–oxide interface vs. distance from the source metallurgical junction with V_{ds} = 0.05 V, for two different gate voltages. These data are from a two-dimensional finite-element computer model.

potential for electrons (ϕ_n) varies linearly between the source and the drain. High-performance VLSI devices are constantly pushed to shorter device lengths to increase speed. The linear channel approximation is not accurate for these short-channel devices, so this approximation must be examined.

Figure 7 shows the results of computer modeling a 0.9-μm device (similar to device A) with two different gate voltages, and V_{ds} = 0.05 V, using a simple, two-dimensional drift-diffusion version of HFIELDS [23]. For larger gate voltage, the curve approaches a straight line in the channel of the device, which is the linear channel approximation. For gate voltages near threshold, however, the effects of the source–drain diffusions and space-charge regions become important. Qualitatively, at lower gate voltages the sheet resistance of the inversion layer is high, and the increased doping density (as well as charge sharing [24]) near the source and drain decrease the sheet resistance near the source and drain of the device. This results in the "S" shape of the curves in Figure 7. The slight asymmetry about the middle of the device is due to the drain voltage modeled (0.05 V), which is large enough to cause a significant reduction in the charge density and sheet resistance near the drain when $V_{th} - V_{gs} = 0.1$ V. In summary, the linear channel approximation is accurate in short devices only at higher gate voltages.

As a result, the higher-gate-voltage data give the most accurate physical trap location. Thus, the best estimate for the trap location in device A is $L_{ts}/L_{ds} = 0.8$ in the forward direction, and, consistently, 0.2 in the reverse direction (from Figure 6).

Since these distances are calculated using the linear channel approximation at high gate voltage, L_{ds} refers to the high-gate-voltage electrical channel length as opposed to the metallurgical channel length from the source to the drain junctions. The solid lines are from the results of computer modeling V_{ts}/V_{ds}. A V_{ds} of 0.05 V was used in the simulation. Note that modeling of these data does not require including the effect of a trap on the device, but merely extracting the device potential at the hypothesized trap location (X = 0.8, 0.2). Note that even the model curves show a slight asymmetry between the forward and reverse directions, especially at low gate voltage. This reflects the asymmetry noted in Figure 7, because the drain voltage (0.05 V) is large enough to create asymmetry in the inversion layer sheet resistance. Also, note that both the data and the model in Figure 6 tend toward 1.0 and 0.0 at low gate voltages, for the forward and reverse orientations, respectively. This reflects the "S" shape observed in Figure 7 due to short-channel effects. To simplify, the inversion layer below the trap is electrically "shorted" to the nearest contact by the effect of the source–drain diffusions at low gate voltage.

Using the trap as a voltage probe

At this point, the trap is calibrated, the trap location is determined, and we can proceed to use this trap to probe the device in the more complicated regions of device operation. We can again use Figure 4 and Equation (4) or (5) to calculate V_{ts} for different bias conditions. Since the emission time is determined mainly by the oxide field, Equation (5) probably remains accurate. Equation (4) becomes less accurate when the horizontal electric field is large enough to have a significant effect on the charge density, and thus the capture time. However, since the emission time was too insensitive in device A, V_{ts} as determined from Equation (4) was used for **Figure 8**. This yields a potential V_{ts} which is qualitatively correct but may have some systematic error at large drain voltages.

Figure 8 shows the ratio V_{ts}/V_{ds} as a function of drain voltage for constant gate voltage for device A in both device orientations. For small V_{ds}, the values reduce to the previously noted physical locations L_{ts}/L_{ds} for the two device orientations. In both orientations, V_{ts}/V_{ds} decreases as V_{ds} increases. Qualitatively, as the drain voltage increases, the charge density near the drain is decreased, creating a higher resistance between the probe and the drain, so that the probe potential approaches the source potential. This is seen in Figure 8 in the reverse orientation data: As V_{ds} increases, V_{ts}/V_{ds} approaches 0.0. In the forward orientation, the trap is near the drain, and, as the drain voltage increases, a high-resistance pinch-off region appears in the small region between the trap and the drain, until most of the potential V_{ds} drops across the small region between the trap and the drain. This device was again modeled using HFIELDS for these bias conditions, and the quasi-Fermi potentials extracted at the two probe locations are shown in Figure 8. The qualitative features of the data are reproduced in the computer modeling results, and the errors are probably due to errors in the model doping profiles, as well as the errors in the approximations needed for Equation (4) to be valid.

In device B, from the 1/4-μm technology, the trapping events were observable throughout virtually the entire operating region of the device. In contrast to the behavior of device A, both the capture and emission times were strongly dependent on the gate voltage in the linear region. This allows us to see the difference between using the capture time and emission times as probes into the device, when Equation (4) becomes inaccurate. **Figures 9(a), (b)** show the emission time and the capture time with the drain voltage fixed at a small value (linear region) and with the gate voltage fixed (into saturation). In **Figures 9(c), (d)** the capture time is plotted as a function of emission time, again for the linear and saturation regions. In the linear region [Figures 9(a), (c)]

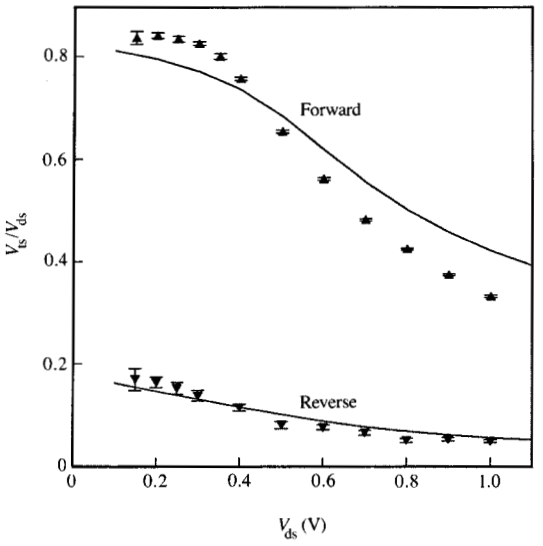

Figure 8

V_{ts}/V_{ds} vs. V_{ds} for forward and reverse device orientations. The gate voltage is a constant 0.9 V. The lines are results from a computer device model.

both region equations (4) and (5) are expected to be accurate. Combining Equations (4) and (5), we obtain the relationship between capture time and emission time,

$$\tau_c = F_{\tau_c}^{-1}\,[F_{\tau_e}(\tau_e)], \tag{8}$$

where $F_{\tau_c}^{-1}$ is the inverse of function F_{τ_c}. Figure 9(c) shows the simple form of the relationship between capture time and emission time for this trap. At the larger drain voltages [Figures 9(b), (d)], however, this relationship changes because Equations (4) and (5) are no longer valid. Specifically, we expect that Equation (4) becomes inaccurate when the trap is near the drain, because the capture time cannot be determined by the surface potentials near the trap alone. This is because the capture time is also sensitive to the charge density, and the relationship between the charge density and surface potential changes near the drain when the device enters saturation. We can qualitatively understand the data in Figures 9(b), (d) as follows: As the drain voltage increases from small values, both the inversion layer charge density near the trap and the oxide field decrease, as in the linear region. However, for larger drain voltages, the charge density (and thus the capture time) ceases to decrease, because electrons are continually supplied from the source. Thus, the capture time becomes constant (independent of drain voltage), while the emission time,

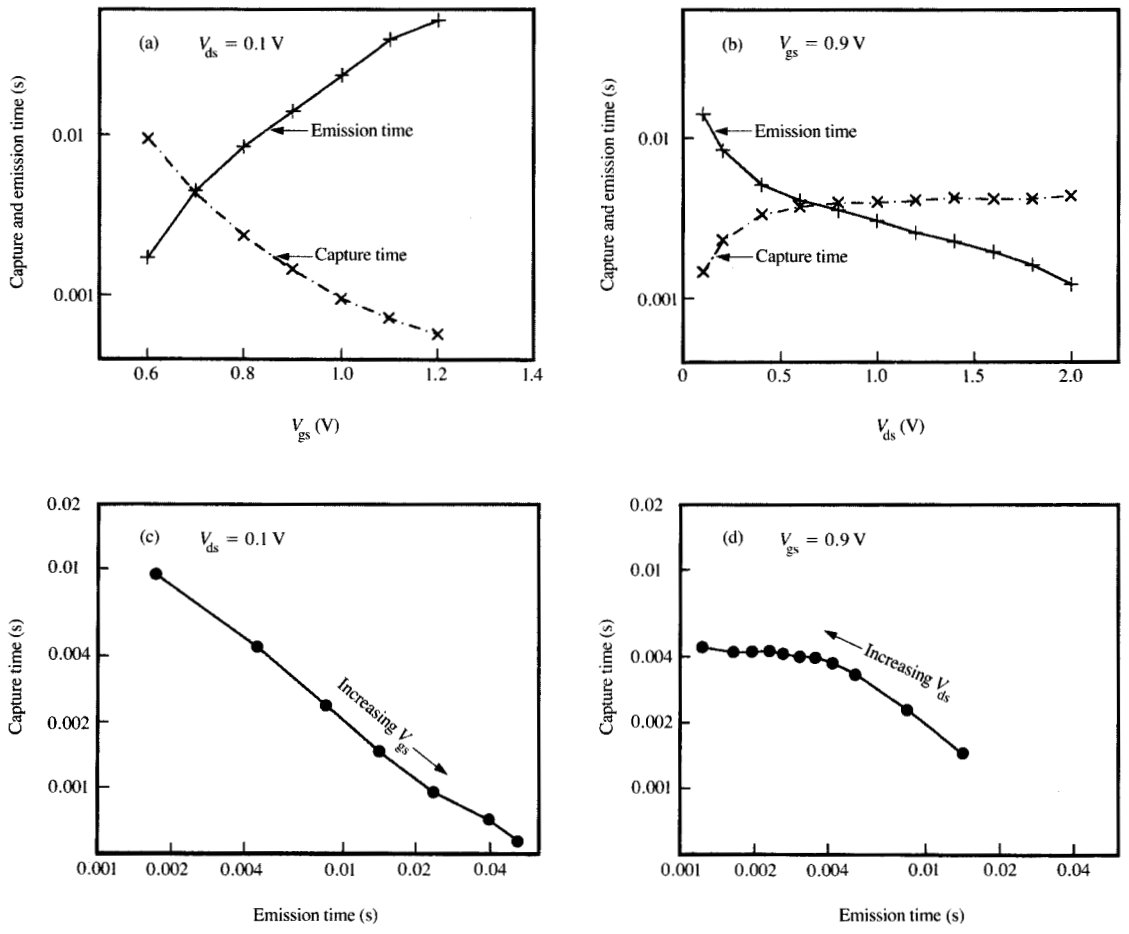

Figure 9

Capture time and emission times for the trap in device B. (a) Capture and emission time vs. gate voltage at small drain voltage. (b) Capture and emission time vs. drain voltage at fixed gate voltage. (c), (d) Capture time vs. emission time for the data from (a), (b), respectively.

mainly dependent on the oxide field, continues to decrease. For this trap we see that the emission time is best used as a probe into the oxide field or the potential across the gate oxide, while the capture time is also sensitive to the charge density in the inversion layer.

To summarize, both the average capture time and the average emission time yield useful information. The two measurements are used to develop the trapping model and verify consistency of the results at low drain biases. At higher drain biases, the two times allow us to extract information about both the local inversion layer charge density and the oxide field.

In most of this work V_{ts} is interpreted as a measure of the quasi-Fermi potential difference between the source contact and the silicon just below the trap. This interpretation simplifies the extraction of the trap location, because the quasi-Fermi potential varies approximately linearly from source to drain in the linear region (see Figure 7). In regions far from equilibrium, such as near the drain in saturation, this interpretation is not accurate. This is because the capture time actually depends on both the oxide field and the charge density in the silicon in a trapping-model-dependent fashion, and these variables cannot be determined from the quasi-Fermi level alone far from equilibrium. For a more accurate analysis, more details of the capture-time and emission-time models must be known, and these details may be trap-dependent. As discussed above, the data in Figure 9, for example, can be used to develop a more detailed interpretation for a particular trap. The simple

interpretation of V_{ts} in terms of the quasi-Fermi potential, however, remains a useful trapping-model-independent starting point.

Trap signal amplitude

In addition to measuring the capture and emission times, the data analysis algorithm also extracts the amplitude of the change in device resistance (ΔR) for each trapping event, with a constant drain current bias. Unlike the individual capture and emission times, which are intrinsically random, ΔR varies only because of "background" fluctuations in the device resistance from other noise sources.

We again start by looking at the simple linear region of device operation. **Figure 10** shows the fractional amplitude of the RTS ($\Delta R/R$) for device B as a function of gate voltage with small drain voltage. In strong inversion the depletion capacitance is negligible, so in the number fluctuation model the effect of a single trapped charge in this region is inversely proportional to the number of charges in the inversion layer,

$$\frac{\Delta R}{R} = \frac{1}{N(V_{gs})}, \tag{9}$$

where R is the average device resistance and $N(V_{gs})$ is the average total number of carriers in the inversion layer as a function of gate voltage. If mobility changes are important, Equation (9) will not be correct, but the step amplitude will still be approximately inversely proportional to the number of carriers due to screening effects. In this linear region the current is also proportional to $N(V_{gs})$,

$$I_{ds} = N(V_{gs})\mu(V_{gs})eV_{ds}/L_{ds}^2, \tag{10}$$

where $\mu(V_{gs})$ is the average mobility in the inversion layer, which depends on gate voltage. If the mobility were constant, the product of the fractional trapping resistance change and the drain current would be gate-voltage-independent in the simple model,

$$\frac{\Delta R}{R} \times I_{ds} = \mu(V_{gs})eV_{ds}/L_{ds}^2. \tag{11}$$

To illustrate this, the product of the step amplitude and the drain current is also plotted in Figure 10. In fact, the gate-voltage dependence of this product reflects the well-known decrease in surface mobility with increasing gate voltage (which is very important with thinner oxides). An accurate description would also include small effects due to modulation of external resistance and channel length by the gate voltage. Data of this kind can help test the detailed accuracy of submicron device models.

Figure 11 shows the fractional device resistance change in device A due to a single trapping event as a function of average drain voltage, for two gate voltages and both

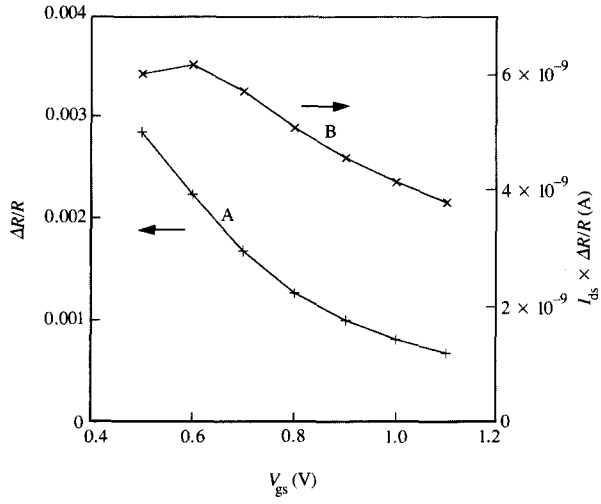

Figure 10

Fractional device resistance change due to trapping for device B as a function of gate voltage with $V_{ds} = 0.05$ V (Curve A, scale on left), and normalized by drain current (Curve B, scale on right).

device orientations. This unique information is useful both in understanding device operation and in studying device degradation due to hot-carrier-induced localized trapped charge and interface states. Note that the location of the trap between the source and the drain is known, which adds to the significance of these data. Many of the features of these data can be understood with simple qualitative arguments but are far from being understood quantitatively. First consider the forward device orientation shown in Figure 11, where the trap is near the drain. As the drain voltage is increased slightly, the charge density near the drain decreases, and the fractional effect of this trap on the device increases. As the drain voltage is increased to $V_{ds} = V_{gs}$, the fractional effect of this trap reaches a maximum. This maximum occurs at higher drain voltage when the gate voltage is larger, and probably occurs when a pinch-off region appears near the trap location. The most sensitive area of a device in saturation is near the pinch-off point. In this region the current is near the surface, and the carrier density is small, so that a single trapped carrier has a large fractional effect. If the trap is near the drain, where the current is no longer confined near the surface, it has little effect, and if the trap is in the strongly inverted region near the source, a single trap has less effect.

In the reverse orientation, the trap is near the source, and several differences are apparent. For small drain

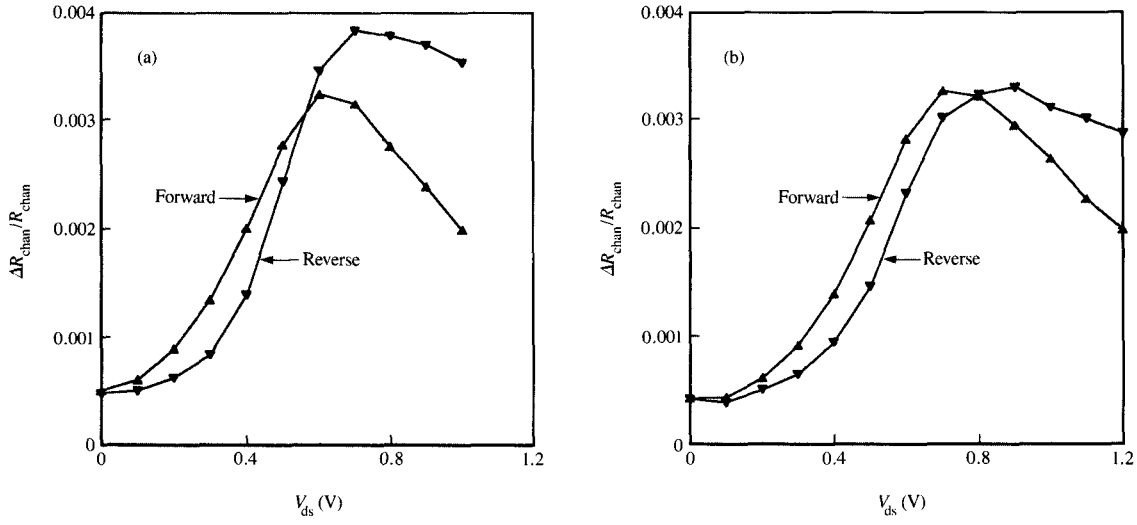

Figure 11

Fractional device resistance change due to trapping as a function of drain voltage for device A, for both forward and reverse device orientations, with gate voltage = (a) 0.09 V and (b) 1.0 V.

voltages, the effect of the trap still increases with drain voltage, but not as much as when the trap is near the drain, because the drain has a smaller charge density. When the drain voltage reaches saturation, however, the effect of the trap near the source continues to rise and becomes larger than the effect of a trap near the drain at higher drain voltages.

These results are consistent with hot-carrier stressing results, where it is well known that trapped charges or interface states have a larger effect on the saturation current when they are nearer to the source than to the drain.

In both orientations, the features in Figure 11 shift to higher drain voltages as the gate voltage is raised. Computer modeling of these results is incomplete, but initial results from a two-dimensional device model show some surprising quantitative differences from the data. This might point out inaccuracies and suggest improvements for VLSI device models.

In device B, a single trap was resolvable throughout almost the entire operating region of the device (**Figure 12**), but the results for this much shorter device are significantly different from those of device A. In device B, L_{ts}/L_{ds} was found, using both the capture time and the emission time, to be 0.15 ± 0.1 for the forward orientation, and 0.85 ± 0.1 for the reverse direction. In contrast to device A, the trap always has a larger effect on the device when the trap is near the drain, even in saturation. Apparently the trap is in the very sensitive region near the pinch-off point in one orientation. In hot-electron degradation, however, it is generally found that damage near the source is more important than damage near the drain, perhaps because this damage is within the source or drain diffusion and not near the pinch-off point. More work is necessary to resolve this issue.

These techniques can be applied to the study of device degradation in different ways. First, high-drain-voltage stressing can create individual electron traps, as shown by Bollu et al. [15]. If a single created trap is resolvable, the techniques described above can be used to determine the location of the trap in the device and to obtain information about the surface potential and charge density near the trap created for different bias conditions. In attempting to reproduce the work of Bollu et al., it was noticed that some of the traps created lasted only a few seconds or minutes, and that in some cases repeated stressing also reduced the number of observable traps in these devices. While the damage to the device certainly increases on the average, in devices of these dimensions the damage is not expected to proceed smoothly and monotonically. In addition, the relatively slow traps near the Fermi level observable by these techniques are probably not representative of all the traps created by stressing.

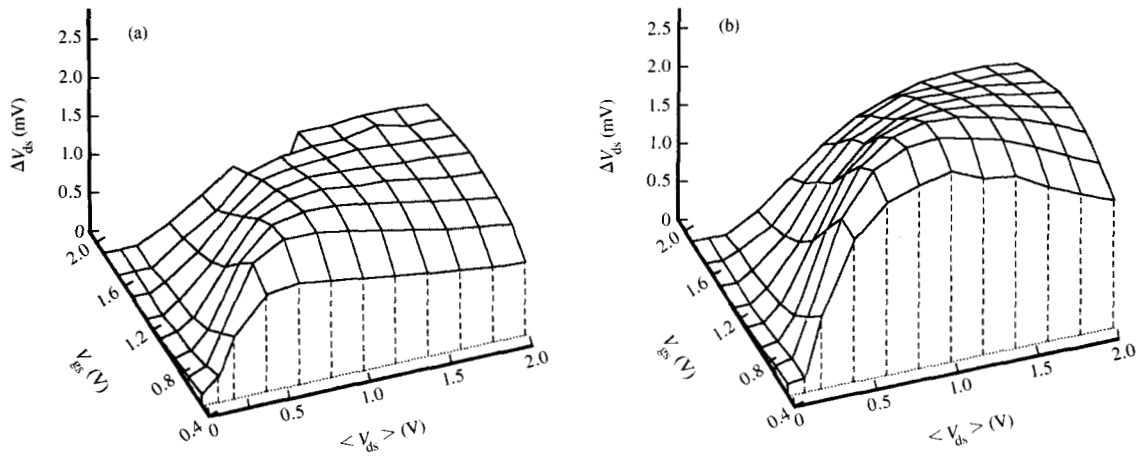

Figure 12

Change in drain voltage (from the mean value $< V_{ds} >$) due to trapping for device B, as a function of both gate voltage and mean drain voltage throughout most of the operating region of the device, for (a) forward and (b) reverse device orientations.

Another technique is to start with a device that has a process-induced trap, then stress the device carefully; if this single trap remains resolvable, information can be obtained about permanent local change in the device (due to fixed oxide charge and fast interface states) at the known location of the trap. Preliminary attempts at this technique show that an original trap may survive moderate hot-carrier stressing if the trap is not located in the most damaged region.

In even smaller devices, it should be possible to watch device degradation processes step by step in real time. Then the effect of every change in the device can be observed during the device stressing, whether it is due to a single charge injected into the oxide, the generation of an interface state, or other mechanisms. In such an experiment, the device would degrade like a random walk in one dimension, with an average drift corresponding to the long-term degradation.

Relationship to 1/*f* noise

There is now considerable evidence that most $1/f$ noise in FETs is due to thermally activated defects such as the traps observed in this work [3, 13, 16, 25]. A single RTS produces noise with a Lorentzian frequency spectrum. In larger devices, the total noise of the device is a superposition of a number of RTSs from a number of defects. A wide distribution of up and down times for these RTSs produces a smooth noise spectrum with a noise power approximately proportional to $1/f$. Many models have been developed for explaining $1/f$ noise in FETs involving carrier trapping [17, 26–28]. Some consider only the change in the number of channel carriers (number fluctuations) and others attempt to include the effects of mobility changes associated with the trapping (i.e., scattering). Although observations of individual traps can directly test many of the assumptions in these models, these experiments have not yet resolved several issues. Observations of individual traps produce detailed information, but only about a relatively small number of traps, previously in limited-bias regions of the device. A complete $1/f$ noise model should account for the dependence of the number of active traps on the bias conditions, as well as the noise magnitude and characteristic frequency of the traps. Since the spatial and energy distributions of oxide traps, as well as the details of charge transport, are likely to be process-dependent, generalizations to differing classes of devices will always be difficult.

Non-Gaussian noise and noise margins

Measurements on small devices have also revealed some unexpected complexities. The noise from interacting or multi-level traps observed by several authors [14, 21, 22, 29] is not explained by any simple parallel kinetics model. In any case where further analysis reveals more information from the noise than is contained in the

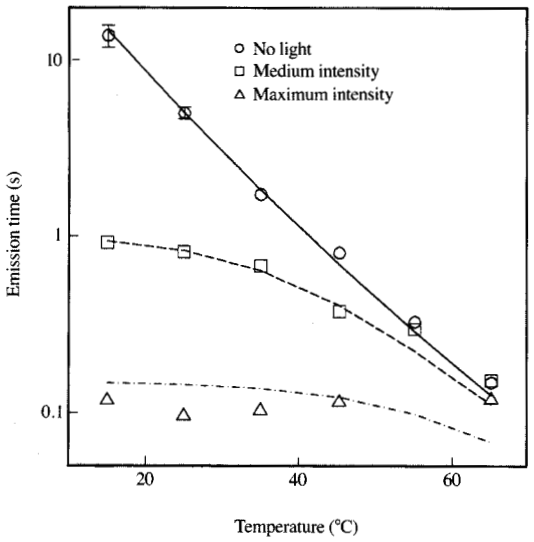

Figure 13

Average trap emission time for device D as a function of temperature for three different 830-nm laser light intensities. Quantitative measurements were not made of the laser light intensities. The curves represent the simple model described in the text. The "medium" laser light intensity used for the model curves was 15% of the "high" intensity.

simple power spectrum, the noise is non-Gaussian. This is true of a simple RTS signal [25], as well as of more complicated signals from interacting traps or multi-state traps [22, 30], although the non-Gaussian effects due to interacting traps are more striking than those of traps which are independent. The large variation in the resistance-change step amplitudes from different traps in similar devices with identical biases has not been explained. The relative roles of number fluctuations and mobility fluctuations have not been resolved because of this variation in amplitudes and because of uncertainties in device dimensions, channel uniformity, and the device models for these small devices. These experimental issues are expected to improve in the near future.

Even in digital circuits, these noise magnitudes may approach significant levels as device dimensions and supply voltages are reduced. Noise sources such as oxide traps may affect noise margins more than a simple analysis would suggest. This is because, unlike more-Gaussian noise sources such as thermal noise and shot noise, a small fraction of the devices will have trapping noise much larger than the mean device noise. This is expected because the number of traps in each device is random. In addition, again unlike thermal noise, the noise is non-Gaussian and appears as steps or bursts, which are more likely to cause a soft error than a Gaussian noise with the same RMS amplitude.

Photoemission from a single trap

In three of approximately 100 devices studied for light sensitivity, an individual trap emission time was found to be dependent on incident light intensity. While the photo-FET method has been used to characterize traps [31, 32], this is the first time photoemission has been observed in a system consisting of a single well-characterized electron trap. As expected, capture time was found to be independent of light intensity. This is additional evidence for the model implicit in this work, which assumes that the RTS observed in submicron FETs is due to charge trapping in oxide interface states. **Figure 13** shows the emission time vs. temperature for three different 830-nm laser light intensities for device C. The lines on this plot are the predictions of a simple model where the emission rate is simply the sum of the known thermally activated rate obtained from no-light measurements [see Equation (2)] and a temperature-independent photoemission rate,

$$\frac{1}{\tau_e} = \frac{1}{\tau_{eT}} + \frac{1}{\tau_{eP}}, \tag{12}$$

where τ_{eT} and τ_{eP} are the characteristic times for thermal emission and photoemission, respectively. The data are consistent with this simple model within the accuracy of the experiment. Using the model of Kirton and Uren [5], the trap emission barrier energy ΔE_{ct} was calculated from the temperature dependence of the capture and emission times, and was found to be 0.6 eV for the trap in device C, at the gate voltage used. Work is underway using a tunable light source to determine whether the energies obtained from thermal activation data are consistent with the threshold for photoemission. The observation of single-trap photoemission allows accurate, detailed measurements to be made on a few traps, and the trap energy and kinetics can be changed and accurately measured as a function of gate voltage and temperature. Techniques such as the photo-FET method, on larger devices, give less precise information on a large number of traps, which is important in determining average distributions of trap photoemission thresholds. Observations on individual traps may also reveal unexpected details not observable in the large-FET experiments. It is not understood why most of the traps studied do not show measurable photoemission rates while some show easily measurable effects.

It may also be possible to determine the oxide field and local surface potential more accurately and easily by determining the photoemission threshold of a trap under

different device bias conditions than by simply measuring the emission time with no light, as was done in this work.

Conclusion

FETs for commercial VLSI application have decreased sufficiently in size that the effects of individual trapped charges are observable. This allows us to study these traps in great detail, and then to use them to understand FET operation and degradation using several methods not possible in larger devices.

Methods were described for deducing the trap location in the device, using the trap to probe the potential near the known trap location under various bias conditions, and using the trapping signal amplitude to quantify the change in the device due to a single trap under different bias conditions.

The initial use of these new measurement techniques will be to compare experimental results with those obtained from computer models of advanced VLSI devices. Even if such models reproduce measured current–voltage device characteristics with acceptable accuracy, comparison with the results of these new internal device measurements will be important in verifying models, choosing among competing models, and, very likely, discovering some areas that are not being modeled accurately.

The direct observation of the effect of individual traps with known location on device characteristics under different bias conditions will contribute to our detailed understanding of device degradation in the smallest VLSI devices of the present and future. These observations also illustrate that it is no longer valid to consider average degradation of average devices when the amplitude of discrete microscopic degradation events becomes significant. Progress is being made in the study of traps and interface states using techniques such as photoemission from single traps, which is of interest to physicists as well as materials scientists.

Finally, similar measurements may help us to predict and avoid "soft" errors caused by trapping events in the noisiest device in a VLSI chip with millions of similar devices.

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Phillip Restle *IBM Research Division, Thomas J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598.* Dr. Restle received the B.A. (honors) degree in physics from Oberlin College, Ohio, in 1979, and the M.S. and Ph.D. degree in physics from the University of Illinois, Urbana, in 1982 and 1986, respectively. His dissertation involved low-frequency noise studies in semiconductors and metals. Dr. Restle received a University of Illinois fellowship in 1983, and an IBM fellowship in physics in 1984. Since joining the Thomas J. Watson Research Center in 1986, he has been engaged in CMOS parametric measurements, device and circuit characterization and modeling, including low temperatures, and studies of low-frequency noise in submicrometer devices and structures. Dr. Restle is a member of the American Physical Society and the Institute of Electrical and Electronics Engineers.

Antonio Gnudi *IBM Research Division, Thomas J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598.* Mr. Gnudi graduated *cum laude* in electrical engineering in 1983 at the University of Bologna, Bologna, Italy. After serving in the Army, he worked in the field of numerical simulation of semiconductor devices at the University of Bologna. Since 1988, he has been visiting the IBM Thomas J. Watson Research Center, where he is engaged in modeling submicrometer devices including higher-order moments of the Boltzmann transport equation.