

A submicron electron-beam tester for VLSI circuits beyond the 4-Mb DRAM

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This paper describes the electron-optical low-voltage column of the submicron electron-beam tester. It can be used to produce an electron probe of 0.12- μm diameter, 2.5-nA probe current, and 1-kV beam voltage. It is shown that in the case of waveform measurements on 1.1- μm interconnection lines, the crosstalk is only $\sim 3\%$. The voltage resolution is sufficient to allow the sense signal of a 4-Mb DRAM (dynamic random access memory) to be measured. Further internal measurements with the electron probe for the chip verification of the 4-Mb DRAM are also shown which demonstrate the flexibility and the benefits of electron-beam testing. On the basis of the measured performance data and its successful use in the circuit analysis of the 4-Mb DRAM, the submicron electron-beam tester appears to be suitable also for VLSI circuits with reduced design rules, e.g., for the 16-Mb DRAM. The improvements required for such future applications are briefly discussed.

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Introduction

Electron-beam testing has proved to be a powerful tool for failure analysis and chip verification. It allows waveform measurements at internal nodes as well as imaging of the functional operation of entire parts of the integrated circuit (IC). The ever-greater reduction in structure and the increase in the operating speed of modern ICs call for a highly accurate electron-beam tester (EBT). Commercially available EBTs, based mainly on modified scanning electron microscopes (SEMs), no longer meet the necessary requirements for measuring advanced ICs. A low-voltage electron-beam tester has been built by ICT GmbH in cooperation with Siemens. A low voltage of approximately 1 kV is required for silicon devices in order to prevent damage and charging.

We report on the electron-optical column of the submicron EBT, on basic experiments performed with this instrument, and on applications for the design verification of our 4-Mb dynamic random-access memory (DRAM) [1]. With regard to the basic principles of electron-beam testing, we refer the reader to the review articles [2-6].

Electron-optical column

Figure 1 illustrates the electron-optical column of the submicron EBT. Part (a) shows a schematic cross section through the column, and part (b) shows the axial distribution of the potential $\Phi(z) = \phi(0, 0, z)$ referred to the cathode and the magnetic flux density $B(z) =$

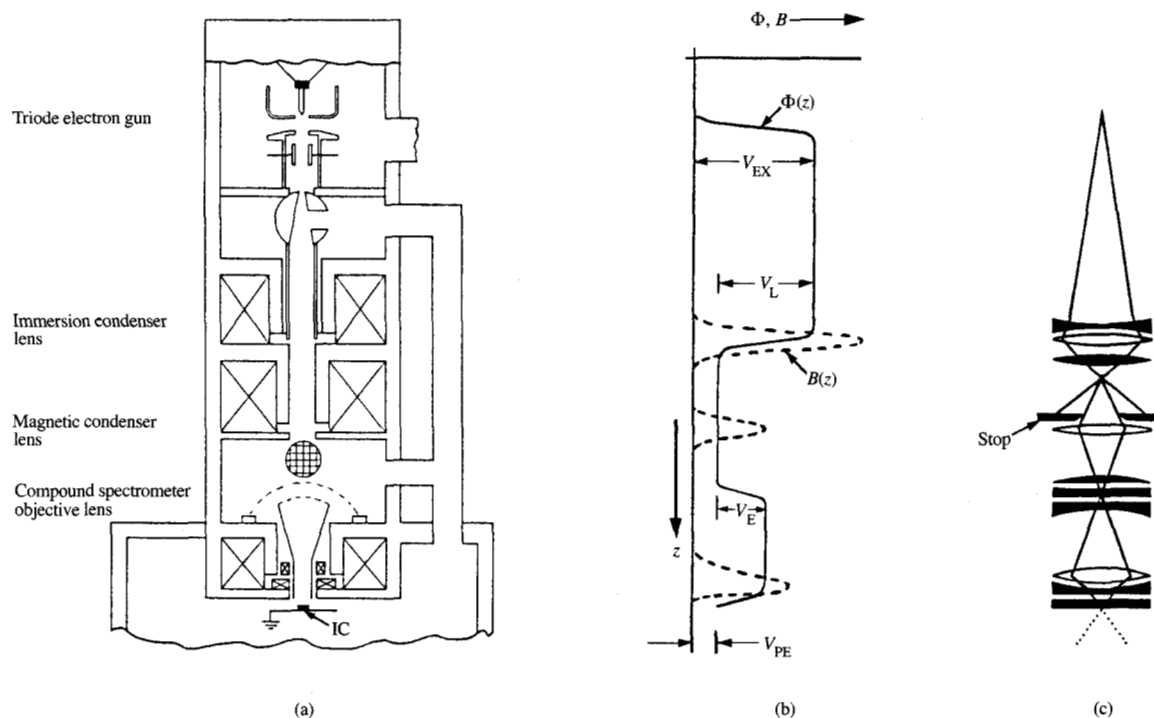


Figure 1

(a) Schematic representation of the electron-optical column of the submicron e-beam tester (ICT 9010). (b) Distributions of the axial (cathode-related) potential $\Phi(z)$ and the axial magnetic flux density $B(z)$ along the optical z-axis. V_{EX} = extraction voltage for the primary electrons in the triode gun, V_L = lens voltage, V_E = extraction voltage for the secondary electrons, and V_{PE} = final beam voltage of the primary electrons. (c) Light-optical counterpart of the electron-optical column. Equivalent lenses of magnetic origin are represented bright, whereas equivalent elements of electrostatic origin (concave and convex lenses and plane parallel plates) have been shaded.

$B_z(0, 0, z)$, which are among the factors affecting the electron-optical performance data (cardinal elements, image aberrations). The kinetic energy of the axial primary electrons is $e\Phi(z)$. The stage is, of course, grounded, and the cathode has the potential $-V_{PE}$ with respect to this ground connection, where V_{PE} is the beam voltage of the primary electrons at the IC. Part (c) of Figure 1 shows the light-optical analog of the column and the principle of primary-electron (PE) focusing, with the equivalent elements of electrostatic origin (concave and convex lenses and plane parallel plates) shown shaded and the equivalent lenses for the magnetic lens fields shown bright.

Theoretically, the maximum beam brightness is proportional to the beam voltage. In the low-voltage range (<2 kV), however, the beam brightness decreases more sharply if a triode electron gun is used. This is ascribed to saturation effects [7] and to the Coulomb interaction of the electrons [8] in the gun. With a tetrode

electron gun, this loss is already smaller [9], but even better is the combination, shown in Figure 1, of a triode gun with a retarding immersion condenser lens [10–12]. Before the immersion condenser lens, the primary electrons (PE) have the energy $eV_{EX} = 5$ keV and are then retarded by eV_L to $eV_{PE} \geq 500$ eV. A brightness of 3.2×10^4 A-cm $^{-2}$ -sr $^{-1}$ for $V_{PE} = 1$ kV has thus been obtained for a (100)-oriented LaB $_6$ cathode with a temperature of 1775 K [10, 11]. This combined electrostatic-magnetic condenser is also characterized by small axial image aberrations (spherical aberration and first-order axial chromatic aberration), which are considerably smaller than with an all-magnetic condenser, which the PEs traverse with a final energy eV_{PE} [13]. This is clearly demonstrated in Figure 1(b), which shows that the PEs traverse the greater part of the magnetic field of the immersion condenser lens with still higher energy; i.e., they have considerable inertia, which means smaller aberrations. Here, however, the axial

image aberrations of the immersion condenser play a minor role, because they are negligible compared with the diameter of the intermediate image of the crossover.

The use of a post-lens spectrometer, e.g. [14], produces a large working distance and thus high axial aberrations and a large probe diameter. In order to obtain a probe diameter of 0.1 μm and a probe current greater than 1 nA, we chose a through-the-lens design. In such a compound spectrometer-objective lens, the spectrometer part in principle also acts on the primary electrons and the objective lens also on the secondary electrons (SEs). Figure 1(c) shows the light-optical counterpart of the spectrometer objective lens. In order to largely eliminate the upper lens group, which is generated by the spectrometer itself, with respect to the primary-electron focusing, we place the intermediate image in or just before this group. The lower lens group represents a retarding combined electrostatic-magnetic lens system distinguished by small image aberrations [12, 13]. That a strong retarding field just in front of the specimen yields low spherical and axial chromatic aberrations had already been recognized by R. F. W. Pease [15, 16].

The SEs are accelerated by an extraction voltage of $V_E = 2$ kV. For a working distance of 2 mm, this means an extraction field strength of 1 kV/mm. The focusing and the angle-independent detection of the SEs, using a semispherical retarding field whose center matches the SE image, is described in detail in [10, 17, 18].

The primary and secondary electron-optical performances of the ICT 9010 submicron electron-beam tester are summarized in Tables 1 and 2, respectively, together with the performances of a modified SEM [19]. The probe diameter of 0.12 μm is sufficient to test ICs with design rules down to as fine as 0.6 μm , which is smaller than the design rules of the 4-Mb DRAM [20]. Using an electron-beam pulse width of 150 ps, waveforms with rise and fall times of 500 ps can be measured with sufficient accuracy. For example, if electron pulses in the ps range are necessary for measurements on GaAs devices, these can also be produced with a relatively simple blanking system similar to a parallel plate deflector [21, 22] or with a laser-triggered photocathode [23]. Deflector blanking is characterized by flexibility with regard to synchronization with the electrical driving of the device under test (DUT), and the pulsed photocathode [23] provides not only very short electron pulses but also a very high beam brightness and thus a short measuring time.

Apart from spatial resolution (PE probe diameter) and temporal resolution (PE pulse width), the two quantities of voltage resolution and crosstalk are also of importance for electron-beam testing. Measurements of these performance quantities are presented in the next section for $V_{PE} = 1$ kV.

Table 1 Comparison of the primary electron-optical performances of two electron-beam testers—a modified SEM (based on a Cambridge Instruments S150 [19]) and a dedicated EBT (ICT 9010).

	<i>Modified SEM</i>	<i>Dedicated EBT</i>
Cathode	W	LaB ₆
Condenser system	Purely magnetic	Immersion lens
Final PE energy (keV)	2.5	1.0
Brightness for final PE energy ($\text{A}\cdot\text{cm}^{-2}\cdot\text{sr}^{-1}$)	1.2×10^4	3.2×10^4
Minimum PE pulse width (ns)	1	0.15
Objective lens	Purely magnetic	Combined electrostatic-magnetic
Working distance (mm)	11	2
Spherical aberration constant (mm)	70	10
Axial chromatic aberration constant (mm)	20	4
Final aperture (rad)	0.02	0.02
PE probe diameter (μm)	0.4	0.12
PE probe current (nA)	5	2.5

Table 2 Comparison of the secondary-electron performances of two types of electron-beam tester—the modified scanning electron microscope and the dedicated electron-beam tester.

	<i>Modified SEM</i>	<i>Dedicated EBT</i>
Type of spectrometer	Planar retarding field	Semispherical retarding field
Location of spectrometer	Post-lens	Through-the-lens
Detector	One Everhart-Thornley	Two Everhart-Thornley
Spectrometer constant	$5 \times 10^{-8} \text{ V}\sqrt{\text{A}}\cdot\text{s}$	$5 \times 10^{-9} \text{ V}\sqrt{\text{A}}\cdot\text{s}$
Crosstalk between 1.5- μm interconnection lines	<40%	<3%

Basic experiments

In order to determine the voltage resolution of the instrument, a triangular signal with different amplitudes was measured on a stub in the chamber. Figure 2 shows the measured signals with voltage swings of 25, 50, 75, and 100 mV. For a noise in the signal of ± 10 mV,

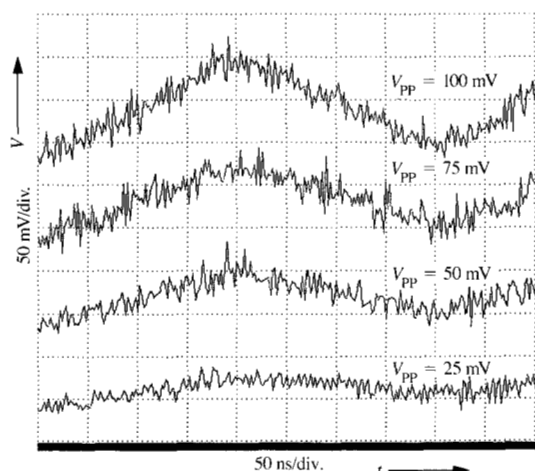


Figure 2

Triangular signals with different peak-to-peak voltages V_{pp} measured on a stub, from which the voltage resolution can be determined. Measurement parameters: probe current 2 nA, electron pulse $\tau_p = 20$ ns, and duty cycle $= 2 \times 10^{-2}$.

voltage changes of 25 mV (requiring twice the measuring time compared with voltage swings of 50, 75, and 100 mV) are still detectable. A voltage change of 50 mV is perfectly measurable. Voltage resolutions of this quality are necessary for measuring the sense signal; see Figure 8, shown later. For the evaluation of the voltage resolution in measurements on 1.1- μm -wide interconnections, reference should be made to the word-line signal WL in Figure 8. It should also be mentioned that the noise detectable in Figure 2 is due in part to the measuring chain (photomultiplier, boxcar integrator, etc.) and not solely to the shot noise of the detected SEs. The measured curves in Figure 2 could be smoothed with a low-pass or a median filter, and it would then be possible to derive a higher voltage resolution from them. Smoothing, however, would filter out not only high noise frequencies, but also high frequencies of the wanted signal and thus its details, which would mean a deterioration in the temporal resolution.

Crosstalk is caused by microfields above the interconnections. The switching of adjacent interconnections changes this local field and thus the trajectories of the SEs leaving the measuring point. This leads ultimately to artifacts in the measured signal, a phenomenon also known as voltage coupling or local-field effect II [24].

The crosstalk was measured on the setup shown in Figure 3. Signals with a range of 5 V were applied with the recorded timing to three interconnections of the address bus in the 4-Mb DRAM. The signal was measured on the center conductor. The measuring point is symbolically indicated. The logic-state mapping image (for basic principle, see [3, 5]) confirms that the injected signal sequences are present in the interconnections. The worst cases were evaluated; these are the following states:

1. The signal being measured is high, and the signals on the adjacent interconnections change from high to low or low to high.
2. The signal being measured is low, and the signals on the adjacent interconnections change from low to high or high to low.

Figure 4 shows the complete signal waveform on the center interconnection and two of its expansions by a factor of 5. Voltage coupling is less than 2% in the first case and $\sim 3.5\%$ in the second case. These values apply to 1.1- μm -wide interconnections. Measurements on submicron structures [25] reveal higher values. These are, however, still acceptable and can be reduced by electron-optical improvements in detecting the secondary electrons. For example, an obvious approach is to use a higher electrostatic field strength for extracting the SEs, as increased field strengths have already been successfully used in photoemission sampling [26, 27].

In the course of our crosstalk measurements, we observed higher crosstalk values in the case of temporarily poor vacuum conditions with contamination of the measuring point. These values, however, were produced by true capacitive coupling between the individual interconnections, with the contamination (caused by line scans of the logic-state mapping) probably acting as a coupling dielectric. The measurement result is also distorted in a manner similar to crosstalk if the PE probe is shifted during the measurement or indeed slips completely off the interconnection. This may happen, for example, due to charging or to the local field of a switching bond wire in the vicinity of the measuring point. Whereas charging can be prevented by a lower beam voltage $V_{PE} < 1$ kV, the deflection of the PE probe by local fields is a major problem for the electron-beam testing of VLSI circuits beyond the 4-Mb DRAM. Such disturbances can, however, in principle be compensated. Some preliminary results look very promising (to be published).

Practical applications: Analysis of a 4-Mb DRAM

The performance of the submicron electron-beam tester has been mentioned or investigated in the previous

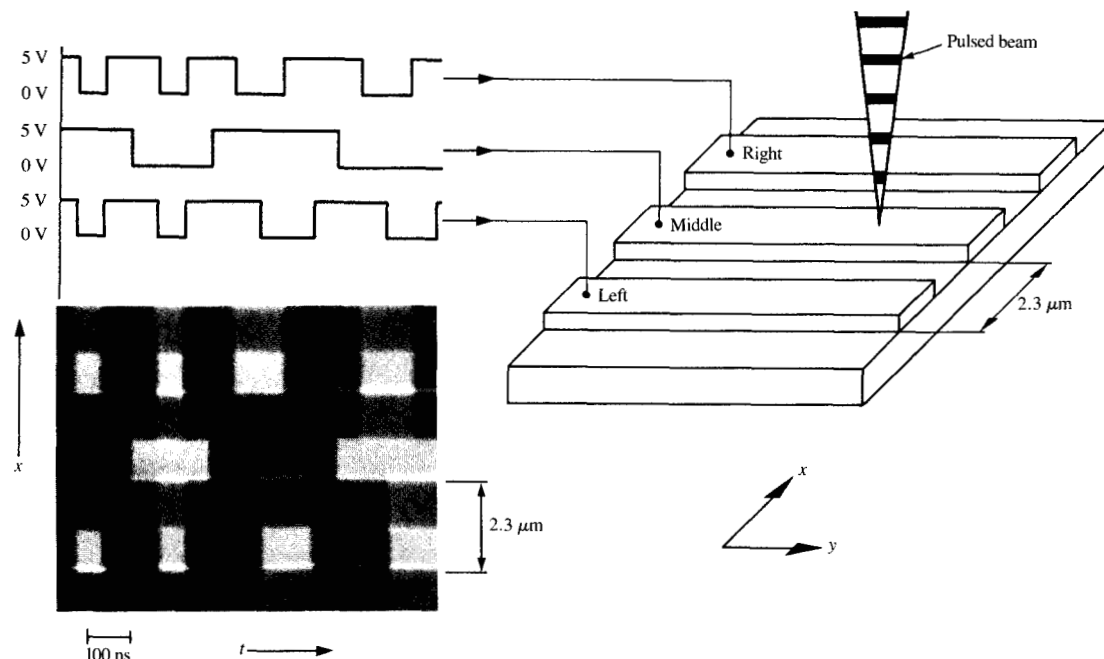


Figure 3

Experimental setup for the determination of the crosstalk (local field effect II) in conjunction with logic-state mapping, which permits control of the signals supplied to the address bus of the 4-Mb DRAM.

chapters, and the limits of the measuring system are therefore known. For each resolution parameter, suitable conditions (measuring point, surrounding effects, probe current, pulse width, etc.) have been chosen, and the measuring setup has been optimized. In principle, however, it is not possible simultaneously to achieve all optimum values with regard to spatial, temporal, and voltage resolution, since these variables are interrelated and in some cases influence one another in opposite directions: The desire for optimum temporal resolution, for example, requires the minimum electron-beam pulse width τ_P and reduces the voltage resolution due to the shortening of the duty cycle; a probe current that has been increased for compensation increases the beam diameter and vice versa. As a rule, a compromise must be struck for the measuring parameters in routine analysis. Disturbances which affect the measuring accuracy, such as switching bond pads and wires, internal current loops, mechanical as well as electrical drift, and loading effects on the probed surface, give rise to greater problems. Such effects mean that the electron beam cannot be precisely positioned on the center of the interconnection line. Resultant measuring errors are

further increased with advancing miniaturization (submicron structures) [25]. The basic values mentioned in the preceding chapters indicate what degree of device integration—measured with reference to the dynamic random access memory as the technology driver of CMOS ICs—can be investigated with the electron-beam tester.

As far as measurement is concerned, the 4-Mb DRAM [1, 20] makes demands that the ICT 9010 electron-beam tester is fully capable of satisfying: minimum interconnection width of upper metallization $1.1 \mu\text{m}$ (pitch $2.3 \mu\text{m}$), fastest signal rising edges $\sim 1 \text{ ns}$, sense signal $\sim 150 \text{ mV}$, cycle time 160 ns ($V_{CC} = 5 \text{ V}$). In addition, the following should be mentioned as practical, economical criteria for the evaluation of the overall system [20]: flexibility of circuit-driving electronics and DUT boards (concept of vacuum chamber); measurements at wafer level, including temperature control and measurement; degree of integration, automation, and CAD linkup; comprehensive, fast change of measuring parameters and measuring methods, etc. In the next section, the last aspect is discussed in more detail.

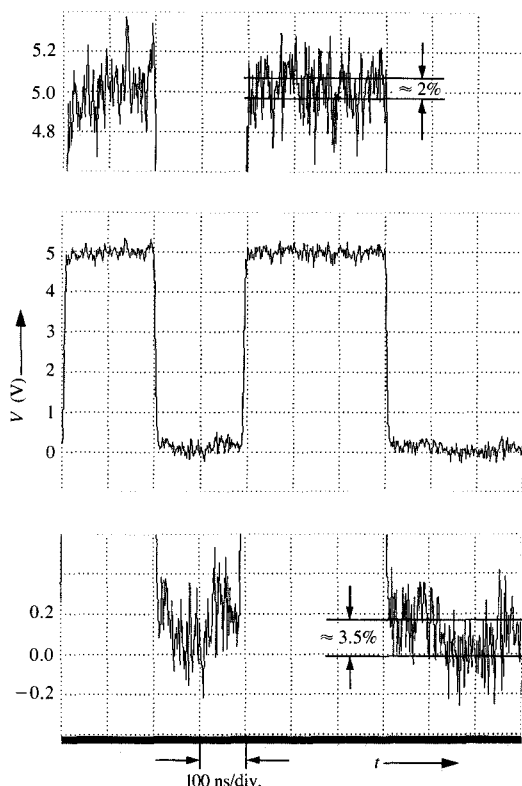


Figure 4

Waveform measurement of the signal on the central line of the setup of Figure 3 together with two detail expansions (upper and lower sections) by a factor of five.

• *Measuring methods (see also Figures 5 to 9)*

The electron-beam tester can be used as follows:

1. As an imaging scanning electron microscope with voltage contrast, for static, stroboscopic, and logic-state mapping (one- and two-dimensional).
2. As a logic analyzer, for timing diagrams.
3. As a (sampling) oscilloscope, for waveform measurements.

A suitable method can be selected, depending on the analysis problem. Furthermore, the ICT 9010 is also a very good inspection instrument (material and topography contrast).

• *Measuring parameters*

A switch can be made from general to detailed measurements without changing the device driving. For a

(relaxed) timing cycle of, e.g., 300 ns (specification: 160 ns with $V_{CC} = 5$ V) and a write and read cycle both for a "0" and a "1," there results an overall sequence (measuring range: T) of 1.2 μ s, which is repeated periodically. Since the trigger signal for synchronizing the measuring chain (boxcar averager) is derived from the device (in the case of laser equipment, the laser's fixed repetition frequency acts as the master), only the trigger signal need be suitably shifted for a detailed investigation of the write operation "1" (compare Figure 8, shown later), e.g., in the time range of 250 ns. Most of the analysis of the 4-Mb DRAM is performed with a comparatively suitable duty cycle $\tau_p/T (= 10^{-2} \dots 10^{-4})$, so that demands for high temporal and/or voltage resolution can be well satisfied. The number of phase points and averages is included proportionally in the measuring time (typical: 15 s up to 2 min, without spectrometer adjustment). The lower limit of measuring delay accuracy depends on the selected measuring range T and the sample points. With the inclusion of all instabilities, a minimum of ± 20 ps has been measured for this limit [20]; counting averages improves the statistics at the expense of the measuring time and reduces the noise amplitude, albeit only as far as the theoretical limit (noise of detected secondary electrons) [28].

The following examples illustrate, in hierarchical order, a typical procedure for the analysis of a 4-Mb DRAM. The demands of the respective measurement methods with respect to the spatial, temporal, and voltage resolution and accuracy, as well as the most important results, are compared in Table 3.

1. *Internal test pads: Figure 5*

As a design for testability, a series of internal control signals were wired via poly bridges to the 4M bus [27]. For the complete suppression of crosstalk, the $4\text{-}\mu\text{m} \times 8\text{-}\mu\text{m}$ pads are surrounded by a guard ring (at V_{SS} potential). Thus, a rough functional check and logic verification is possible at the lowest level of the analysis hierarchy (e.g., on the 4-Mb DRAM, also at wafer level). The PE beam scans the test pads in a line scan and measures the most important 4M signals quasi-simultaneously. The result may be a logic-state mapping [Figure 5(b)] or a timing diagram [Figure 5(c)]. In a short time (see the measuring times given in Figure 5), it is thus possible to characterize the entire internal operation of the memory after measurements on all test-pad structures. Due to the sometimes unsuitable arrangement of the internal test pads at the periphery of the chip, critical signal transit times cannot be measured.

2. *Timing diagram of a partial circuit: Figure 6*

At five circuit nodes of an address buffer (sample and hold circuit), the internal CMOS signals were evaluated

Table 3 Requirements due to spatial, temporal, and voltage resolution for the indicated analysis examples and most important conclusions.

Analysis example	Resolution requirements			Conclusions
	Spatial	Temporal	Voltage	
Internal test pads (Figure 5)	Poor: $4 \times 8\text{-}\mu\text{m}^2$ pads	Poor: Only qualitative	Poor: (a) Logic state mapping: Voltage contrast (b) Timing diagram: High/low-rating ($>2.5\text{ V}/<2.5\text{ V}$)	Rough logic verification: • Existence • Delay • Range of logic states
Timing diagram of special circuit (Figure 6)	High: Internal nodes	Moderate: Only delay information required	Poor: High/low-rating ($>2.5\text{ V}/<2.5\text{ V}$)	Accurate logic verification: (dto.1), but without loss of conducting line delay
SPICE simulation verification (Figure 7)	High: Internal nodes	Moderate/high: • Precise delay evaluation • No true signal rising edges required	Moderate: 50% value of peak-to-peak voltage swing	Chip verification: • CAD model • Transistor parameters Design weaknesses: • Signal delays • Influence of external parameters (temperature, power supply, operating modes)
Sense signal (Figure 8)	High: Internal nodes	High: Sensing includes fastest internal signals	High: • 150-mV nominal potential difference • WL signal boosted up to 10 V and higher	Chip verification: Secure evaluation of sensing operation
Precise timing analysis (Figure 9)	High: Internal nodes	High: Fast internal signals (spike detection)	High: True signal shape and voltage swing	Chip verification, failure analysis: Sophisticated internal analysis

with respect to "high" ($>2.5\text{ V}$) and "low" ($<2.5\text{ V}$) states, and a timing diagram [Figure 6(a)] was recorded [29]. Up to 24 measuring points can be selected and stored in the preceding positions within the image area [Figure 6(b)]. An evaluation of the logic assessment of the time sequence and duration of the high/low states can thus be performed in a single measuring cycle. The result is similar to a measurement with a logic analyzer. In contrast to the internal test pads (see the preceding subsection), these measurements are made at the time-critical internal nodes.

3. SPICE simulation comparison: Figure 7

The switching performance of the memory is calculated in advance in a simulation (SPICE) [29]. Normal and worst-case conditions (overvoltage, undervoltage, temperature) are taken into consideration for various operating modes. For reasons of economy, however, by no means can all cases be simulated, with the result that design weaknesses are often not revealed until the analysis. This calls for waveform measurements—as shown here in the active cycle, $V_{CC} = 5\text{ V}$ —on internal

nodes with, in some cases, minute structure sizes. The evaluation of the signal curves is based on (relative) 50% values, so that the requirements with respect to temporal and voltage resolution as well as voltage swing deviate from possible values. The good agreement between measurement and simulation allows conclusions to be drawn with regard to the simulation model used and to the transistor parameters, which were apparently realistically estimated. It must, however, be remembered that process fluctuations may influence the results. The access time, which can be read from the diagram, has a value less than the specified 80 ns for standard conditions.

4. Measuring the sense signal: Figure 8

The measurement of the sense signal on minute structures imposes extreme demands on the voltage resolution of the measuring system, since the potential difference to be demonstrated is only $\sim 150\text{ mV}$. The folded-bit-line concept used [1] involves a storage cell situated at every other intersection of a word/bit line (WLm/BLn) and connected via a selector transistor to

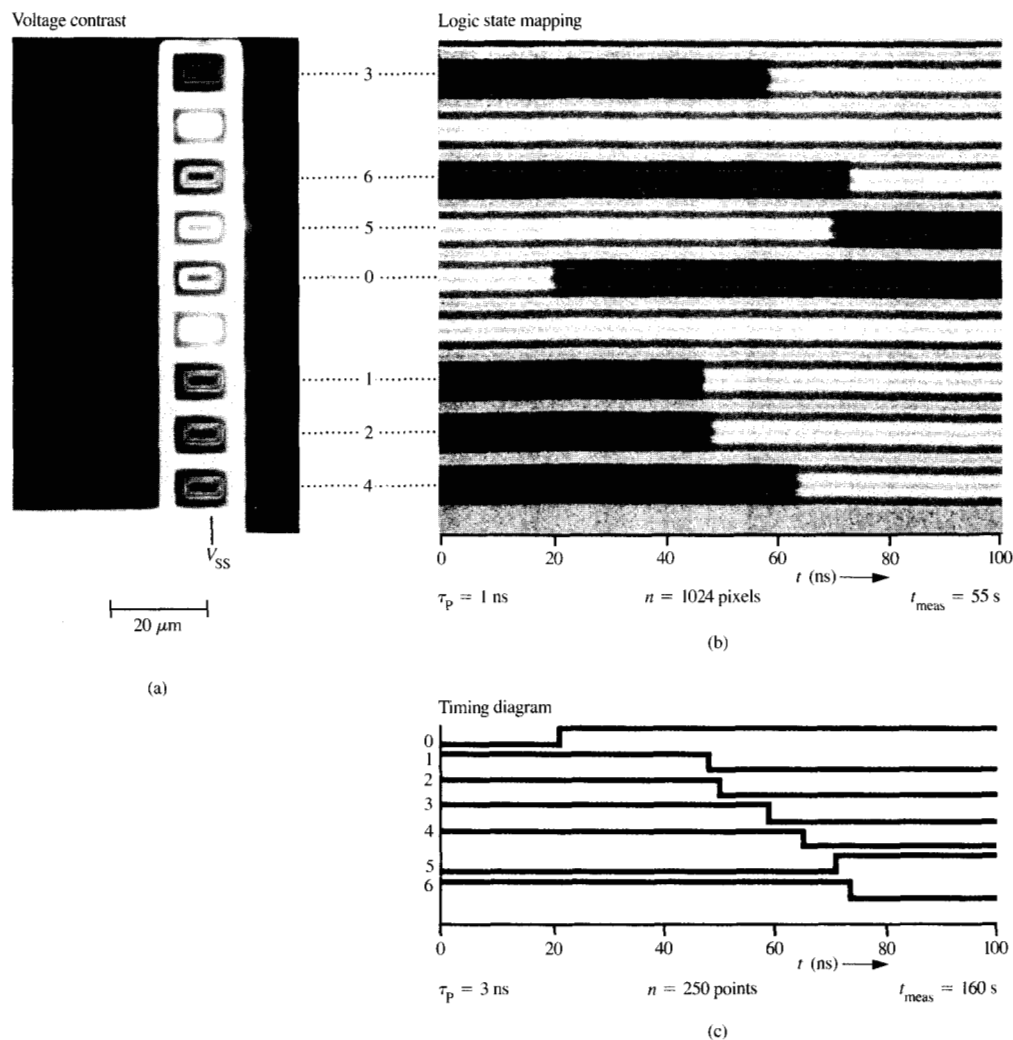


Figure 5

Logic verification of the precharge cycle of the 4-Mb DRAM on internal test pads (a) surrounded by guard rings via logic-state mapping (b) and timing diagram (c). τ_p = primary electron pulse width.

the BLn and to the sense amplifier (SA). The $\overline{\text{BL}}_n$ is also connected to the SA (here $n = 0$). Figure 8(a) shows an overview of the complete read/modify-write cycle (cycle time: 240 ns). Before the read operation (I) (shown here: reading of a "1"), BL0 and $\overline{\text{BL}}_0$ are floating at the bit-line potential $V_{\text{BL}} = 2.5$ V. The read operation (II) is initiated by the boosted WLn (here $m = 0$), which switches through the selector transistor at ~ 5 V, with the result that the small charge stored in the trench capacitor (~ 40 fF) drains onto the bit line BL0. This results—

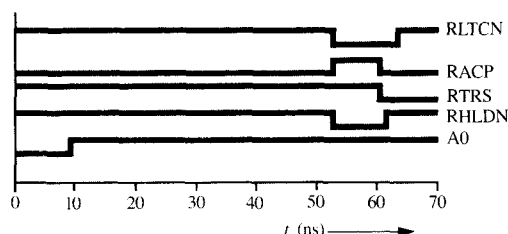
because of the clearly higher BL capacitance of ~ 350 fF—in the low potential difference between BL0 and $\overline{\text{BL}}_0$ of approximately 150 mV. The SA detects and boosts this potential difference during *sensing* (III). The transition from *internal* sensing (within the RAS chain) to *external* sensing (IV) is evident from the brief renewed rise in the $\overline{\text{BL}}_0$ potential: The column-select latch (not shown) connects the internal BL to the external BL and enables the CAS chain. Finally, BL0 and $\overline{\text{BL}}_0$ are boosted to V_{ss} and V_{cc} potential. The start of the *writing operation* of the

read/modify-write cycle selected here (V) is apparent from the toggling of $\overline{BL0}$ and $\overline{BL0}$. After restore and precharge, the cycle is finally completed.

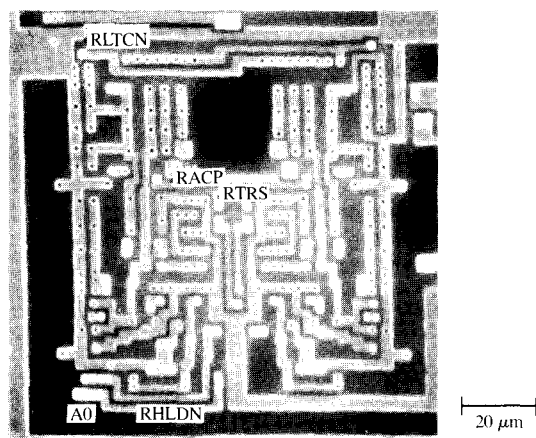
Details of the sensing operation taken from the same long cycle measurement range are shown in Figure 8(b). From this graph it can be seen that the sense signal is about 150 mV. The accuracy of this measurement is ± 100 mV due to the small feature sizes and the high temporal resolution. Nevertheless, the capacitance ratio between cell and BL, which is crucial to the reliable sensing of the contents of the memory, can be adequately valued.

5. High-accuracy timing analysis: Figure 9

Finally, a complex analysis example that imposes equally high demands on temporal, spatial, and voltage resolution is discussed. Analyses of this kind [30] are indispensable for the identification of design weaknesses and lead to appropriate redesign measures. Frequently, it is only the electrical characterization of the silicon on the



(a)



(b)

Figure 8

Timing diagram (a) of input buffer signals of the sample and hold circuit, which can be seen in the SEM micrograph (b).

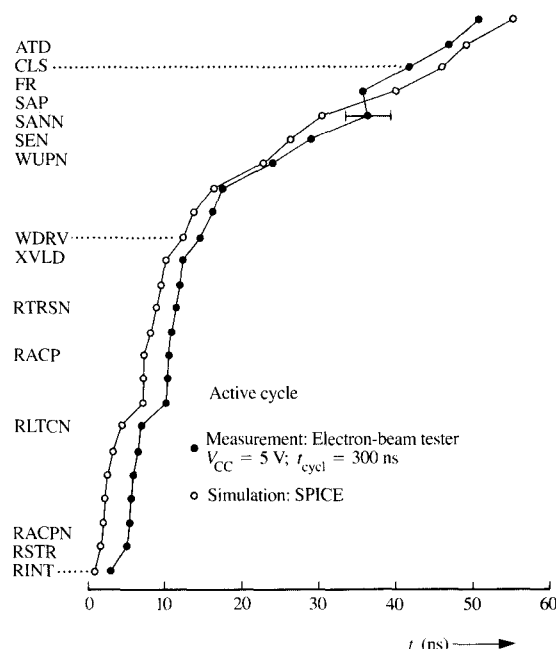


Figure 7

Comparison of measured and simulated signal delays in the 4-Mb DRAM.

function tester that reveals a failure map that is dependent on external parameters (temperature, supply voltage, special timing conditions or function modes, etc.). In the present case, the read-write cycle was studied under critical operating conditions (increased supply voltage $V_{CC} = 6$ V). The logic-state mapping micrographs shown in Figure 9(b) were produced by scanning the electron beam over the line shown in Figure 9(a). "High" potentials (6 V) of the six parallel signals are shown dark and "low" potentials (0 V) bright. Figure 9(c) shows corresponding waveform measurements of two selected signals ("ATDN" and "CINT") in the same time range. The parameter in the three diagrams, positioned one above the other, is the externally impressed reference voltage V_{REF} , which is normally produced internally by the memory. At $V_{REF} = 1.39$ V (normal operation), two ATDN pulses occur, about 5 ns in width. The first one precharges the external bit line. During the second pulse, the CINT signal increases, and thus the column address buffer works correctly for readout. At $V_{REF} = 0.93$ V, this second ATDN pulse is missing, and the rising edge of CINT is considerably delayed. At $V_{REF} = 0.91$ V, some ATDN oscillations occur, and CINT is only a weak pulse

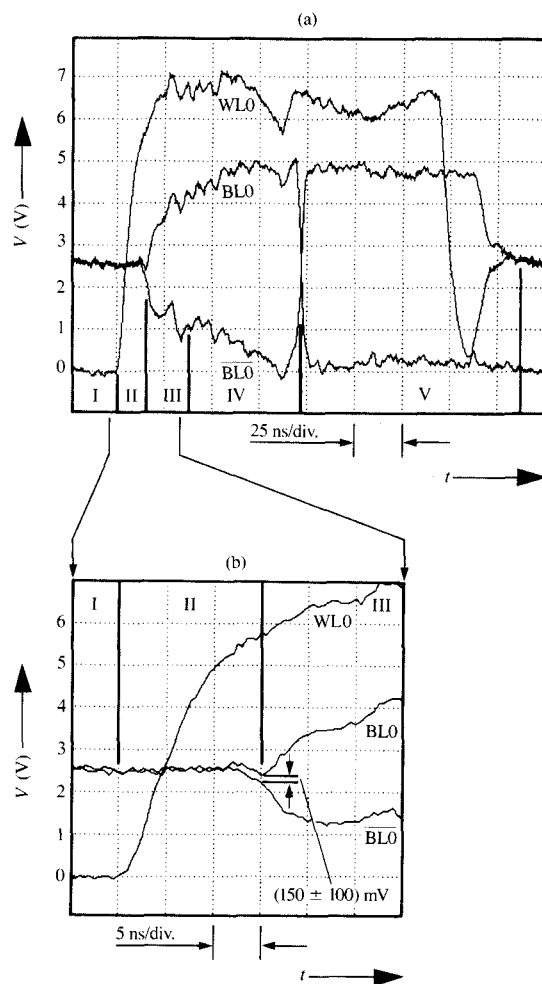


Figure 8

Waveform measurements of a word line signal (WL0) and bit-line signals (BL0 and $\overline{\text{BL0}}$) during the read/modify-write operation of the 4-Mb DRAM. (a) Overview of the complete cycle (cycle time: 240 ns). Different sensing operating modes are indicated by I ... V. (b) From the detail (time scale enlarged by a factor of five), the sense signal of about 150 mV can be evaluated. Measurement parameters: beam voltage $V_{\text{PE}} = 1 \text{ kV}$, probe current $I_{\text{PE}} = 2 \text{ nA}$, electron pulse width $\tau_p = 1 \text{ ns}$, width of word line = $1.1 \mu\text{m}$, size of internal bit-line nodes = $1.5 \mu\text{m}$.

signal. According to this investigation, the expected behavior is guaranteed only for $V_{\text{REF}} \geq 1.39 \text{ V}$; this critical value was understepped due to a V_{SS} overshoot at the end of internal sensing, without V_{REF} being able to respond. The signal behavior precisely recorded in Figure 9(c) could already be characterized qualitatively by logic-state mapping [Figure 9(b)], with the result that this imaging method is again shown to be a significant e-beam testing mode.

Conclusions and outlook

From basic measurements and our experience gained during the chip verification of the 4-Mb DRAM, we expect that the ICT 9010 submicron electron-beam tester can also be used for the 16-Mb DRAM. The spatial resolution is certainly adequate for this purpose, and the crosstalk measuring error due to the local fields can, if necessary, be kept at a sufficiently low level by means of additional electron-optical measures. A greater cause for concern is the observed shift of the electron probe during waveform measurements, which also leads to measuring errors. A correlation was observed between the shift of the probe and switching of bond wires or current drawn by the IC. A compensation of this error seems possible. If a two-level aluminum metallization layer is introduced for the 16-Mb DRAM, fewer signals will be available for electron-beam testing. This leads to specific design requirements for electron-beam testability [31].

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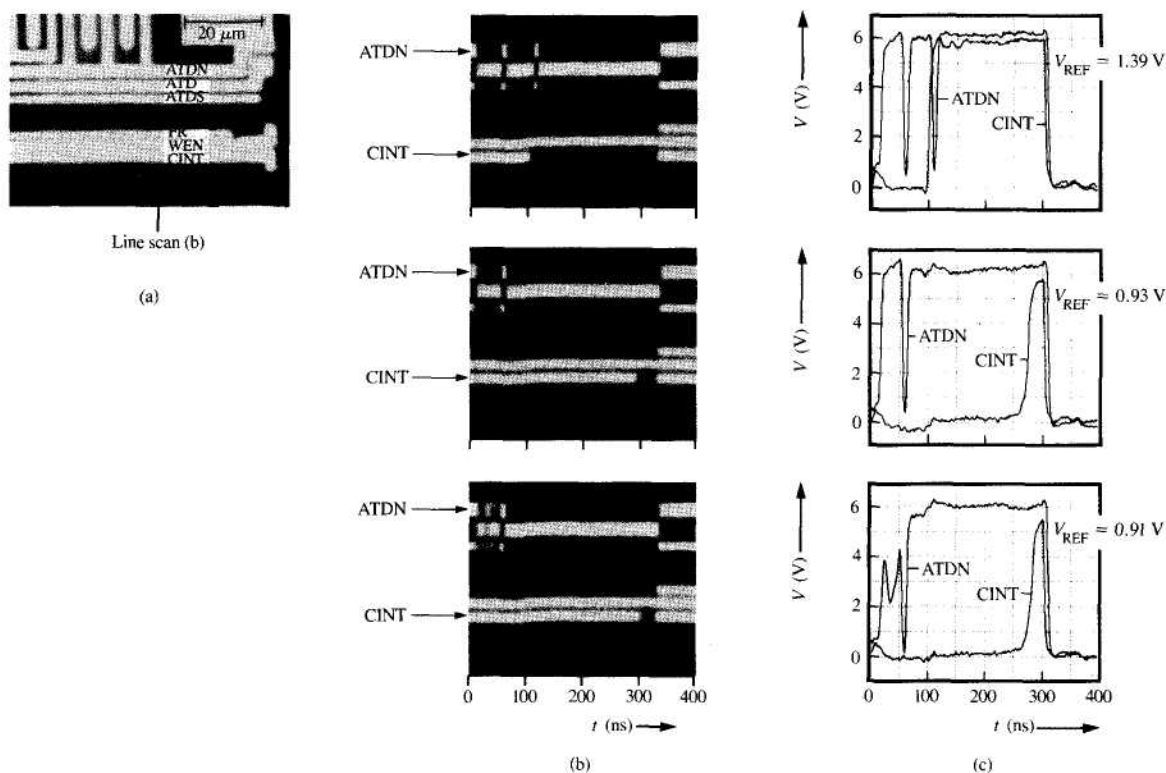


Figure 9

Accurate analysis of internal switching operations in the 4-Mb DRAM. (a) Voltage contrast micrograph in which the line-scan position for the logic-state mapping measurements is indicated. (b) Logic-state mappings and (c) waveform measurement of ATDN and CINT for three different values of the parameter V_{REF} .

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