Preface

Very-large-scale integrated (VLSI) circuits present some very challenging and interesting problems to the testing community. It is the objective of this special issue to describe and discuss some of the ingenious ways in which these problems are investigated and solved. Before introducing the papers in this issue, a few general comments on testing are in order. The ability to test the performance of a particular technology underlies the progress in developing that technology. In the case of VLSI, this principle applies at every level of the integration hierarchy, from testing of individual devices to testing of new chip and system complexes. The challenges of VLSI are posited by the increased speed of the devices, their decreasing dimensions, and the increasing chip complexity (number of transistors per chip and number of interconnect levels). A distinction should be made between testing for design verification—i.e., testing a new design (novel layout and/or fabrication), be it at device, chip, or system level, and testing for fabrication integrity—Is the chip or package fabricated as designed, or do its defects come from imperfect fabrication? This is the distinction between testing at the research and development stage and testing at the manufacturing stage. At some stage of the design verification these two testing modes overlap.

This special Journal issue emphasizes the extremely difficult problems in testing at the chip level, where the complexity of VLSI challenges not only design verification but also the detection of defects in the manufacturing process. The consequence of this increased complexity has been the necessity to design for testability. As the VLSI design rules become ever more aggressive, random manufacturing defects increase concomitantly in number and variety. The role of testing in the manufacturing environment is to reveal these defects economically and as early as possible in the manufacturing process, since the cost of repair in the field will be very much more than the cost of detecting that same defect at the chip level.

The first section of this issue, Device/Circuit Test, deals with the testing of individual devices, typically in the VLSI environment. The first six papers of this section address methods for examining the ac characteristics of VLSI devices by using different noncontact techniques to probe waveforms at internal nodes in integrated circuits (ICs). Here the main challenges of testing are in achieving sufficient voltage, spatial, and temporal resolutions to make these measurements. For instance, the ability to achieve sufficient temporal resolution is an example of a generic testing problem—the "chicken and egg" problem of testing some aspect of an aggressive chip technology with a technology that must in that aspect be at least as aggressive. In testing the switching speeds of individual devices, we would like the tester to produce stimuli which are several times faster than the device speeds. One way of solving this problem, as described in several of the papers of this section, uses directly or indirectly the fast switching speeds that are possible in laser technology. Clearly, mechanical probes are not capable of internal node testing; the probes used here for noncontact testing are optical, and, for even better resolution, electron-beam probes. The first three of the papers discuss different optical probe techniques: electro-optic sampling, optical charge sensing, and photoemission probing. The next three papers examine electron-beam probe techniques, with two papers concentrating on temporal resolution using beam-blanking techniques and laser-pulsed photoelectrons, respectively.

The last two papers of this section report on the dc parametrics of submicron FET devices. In the first, traps in the gate oxide are used as internal probes of the device. In the second, a new method for measuring mobilities is introduced which allows parameter extraction for submicron devices.

Testing at this level of the integration hierarchy is largely for design verification, although it is conceivable that there might be critical circuit nodes where testing at the manufacturing stage could be important. The testing procedures described in this section can also be important in fault analysis; for example, if the chip-level test reveals a fault in some part of a circuit, the device testing tool will allow a complete investigation of the nature of this fault.

The paper in the second section, Package Test, discusses an electron-beam probe method for circuit testing of the interconnects on multi-chip packages.

The third and final section, Chip and System Test, is devoted to testing at the manufacturing level. In this case, test signal patterns must be generated which can uncover a substantial portion (number and type) of the total circuit defects in a reasonable time. The first paper of this section looks at very-high-speed pin testers that allow the application of signal patterns to chip I/O at high frequencies. Next, a paper discusses the special difficulty of pattern generation for fault detection of memories embedded in logic. Fault simulation allows efficient production of test patterns for maximum coverage; however, for complex chips this can cause excessive memory storage and simulation time, and other resource problems. This is discussed in the third paper for the particular case of circuit chips with embedded memory. In general, most of the chip tests are not executed at system speed, and this can lead at the system level to ac-related faults. The next three papers discuss this problem—two look at ac testing at the chip level and the third at the multi-chip module level.

For a VLSI chip to be fully testable at all, let alone tested in reasonable time, the chip must be designed with

testability in mind. The remaining papers in this section examine different issues of design for testability. The first of these discusses the use of boundary-scan techniques, which allow reduced-pin-count testing on chips with high signal–I/O pin count. Next is the first of several papers on built-in self-test (BIST), which is generically a method that uses on-chip circuitry to generate test (usually pseudorandom) patterns and to analyze chip responses (signature analysis), thus avoiding the problems of high-pin-count testing. In this paper, pseudorandom-pattern self-test is discussed for a processor in combination with boundary-scan techniques to allow migration of tests to higher levels of the integration hierarchy. The succeeding papers discuss, respectively, data compression techniques in signature analysis registers that determine, on chip, good or bad responses to test patterns, and the errors that can result from such compression; an algorithm that efficiently determines required pseudorandom test-pattern lengths to test a network; cellular automata arrays as an alternative approach to conventional self-test circuits for pseudorandom number generation and for signature analysis; and automation support for self-test, including design rules checking, testability analysis, and expected good-machine signature generation. The final two papers discuss testing of the local area network (LAN) interface chip; the first describes built-in self-test and boundary-scan functions, and the second looks at the very different problem of analog testing, in particular the phase lock loop circuitry of the chip.

I wish to conclude this preface by thanking all the authors who submitted papers, the many referees who were involved in the reviewing process, and particularly Jean-Marc Halbout and George Chiu, who were involved from an early stage with definition of the issue and helped me throughout the reviewing and acceptance process.

Paul G. May
Guest Editor