Preface

The first five papers in this issue describe the Q-Coder, an adaptive binary arithmetic coder that uses a fixed-precision representation of the code string and a self-generating mechanism for adaptive symbol-probability estimation. Developed by researchers at the IBM T. J. Watson Research Center in Yorktown Heights, New York, and the IBM Almaden Research Center in San Jose, California, the Q-Coder is expected to find particular application in the compression of bilevel images for transmission and storage.

The first paper, an introduction to the basic principles of the Q-Coder by W. B. Pennebaker, J. L. Mitchell, G. G. Langdon, Jr., and R. B. Arps, briefly describes the concepts of arithmetic coding in historical context, then summarizes the Q-Coder coding conventions, the optimization of hardware and software coding structures, and the interval-renormalization procedure used in probability estimation.

In the second paper, Mitchell and Pennebaker describe in detail the means by which hardware and software implementations of the Q-Coder can both be optimized while remaining compatible, and the solutions to problems associated with fixed-precision implementation.

In the third paper, the same authors present a theoretical analysis and a model describing the process of adaptive probability estimation using interval renormalizations during the coding procedure, and the implementation of the process as a finite-state machine. Experimental studies verify the model and provide performance data.

Implementation from a software perspective is covered in the fourth paper, which describes implementations for both hardware and software paths, presents detailed flowcharts of the software implementation, and provides results for a software-optimized model against a small data set.

The final paper, by R. B. Arps, T. K. Truong, D. J. Lu, R. C. Pasco, and T. D. Friedman, recapitulates the principles of the Q-Coder from a hardware designer's point of view, describes the design of a versatile VLSI chip capable of implementing a variety of data-compression systems based on adaptive binary arithmetic coding architecture, and describes a Q-Coder implementation of the chip.

The *Journal* wishes to give special acknowledgment to J. J. Rissanen and G. G. Langdon, Jr. Dr. Langdon is, as already noted, a coauthor of one of the papers, and both names appear frequently in the references and footnotes of all five papers in recognition of the insight they have brought to many particulars of the work described. In addition, however, their fundamental contributions to IBM research in the field, and to the development of arithmetic coding generally, form much of the context within which the present work was done.