Electrical design of signal lines for multilayer printed circuit boards

by C. S. Chang

Key aspects of the electrical design of signal lines for multilayer printed circuit boards used in computers are examined. Illustrative calculations are carried out for several signal-line configurations, and associated means are presented for selecting design trade-offs regarding cross talk and skin-effect-induced delay.

Introduction

In multilayer printed circuit boards (PCBs) used in computers, some of the conducting layers are used to provide electrical ground and power-supply voltages, and others to provide interconnections among integrated circuit chips [1–4]. A signal layer usually contains parallel signal lines; two adjacent layers of orthogonal lines constitute a signal-plane pair. It is assumed that signal lines may or may not have adjacent neighbors. If two or more parallel signal lines are in close proximity, the presence of a signal on one line will cause noise to appear in adjacent lines [5–10]. At the near (source) end of the signal lines, such noise may be saturated or unsaturated, depending on signal rise time and the length over which the lines are coupled. At the far end, the noise generally increases linearly with length and inversely with rise time. Another source of noise, denoted as delta-I noise [10, 11] is due to changes in current through various parasitic inductances which may be present (e.g., those associated with chip-carrier leads). Although they are only briefly covered in this paper, such parasitic inductances must generally be taken into account in PCB design.

Transmission-line characteristics of a signal line

A typical signal line and nearby voltage plane form a pair of parallel conductors having a loop inductance per unit length L (in pH/mm) and a signal-to-reference capacitance per unit length C (in pF/mm). The pair must be treated as a transmission line for fast-rise-time signal propagation [5, 6, 12, 13]. The corresponding propagation time constant τ and the characteristic impedance Z_0 can be expressed as

$$\tau = \sqrt{LC} = 3.33\sqrt{\epsilon_r}, \quad \text{(ps/mm)} \tag{1}$$

$$Z_0 = \sqrt{L/C}. \quad (\Omega) \tag{2}$$

Note that the signal propagation time constant τ is proportional to the square root of the relative dielectric constant ϵ_r. In vacuum, a signal propagates 1 mm in 3.33 ps. In the glass–epoxy dielectric cited in [1], assuming $\epsilon_r = 4$, 6.67 ps are required. Some of the signal paths within one CPU cycle may span many logic-gate stages at close

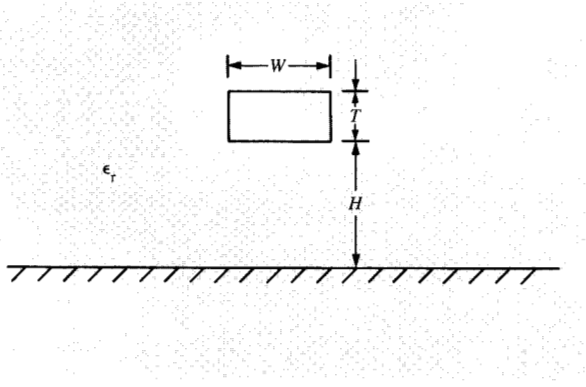


Figure 1

Cross section, in a homogeneous medium, of a stripline of width W and thickness T, located at a height H from a voltage-reference plane.

Table 1 Illustrative effects of number of layers in dielectric laminate and signal-line H/W ratio on characteristic impedance of stripline structure, assuming $\epsilon_r = 4$.

No. of layers in dielectric laminate	H/W	Z_0 (Ω)
2	1.4	60.4
3	2.1	71.1
4	2.8	79.1
5	3.5	85.6
6	4.2	91.1
7	4.9	95.9
8	5.6	100.2

proximity. Some of them may contain only two logic-gate stages separated by a significant distance. For the signal paths of the latter type, if the time of flight across a PCB signal line is 60% of the total signal-path delay, a reduction in ϵ_r from 4.0 to 2.5 would reduce the total signal-path delay by 12.5%.

Characteristic impedance of a signal line

Signal-line width may range from 20 to 200 μm. Because of process considerations, the minimum line-to-line spacing is usually 1 to 2 times the line width. Line thickness is about 0.3 to 0.6 times line width.

To examine associated geometrical considerations in signal-line impedance design [5, 6, 14], we next consider a stripline having thickness T and width W, shown in **Figure 1**. The stripline is assumed to be surrounded by a homogeneous medium at a height H above a voltage-reference plane. The medium is assumed to have a relative dielectric constant ϵ_r. The signal-line-to-reference-plane capacitance per unit length C is unchanged if H, W, and T are scaled by the same factor. By using the line width as a normalization parameter, C can be expressed as

$$C = \epsilon_r f(H/W,\ T/W). \tag{3}$$

From (1) and (2),

$$\sqrt{\epsilon_r} Z_0 = 3.33/(C/\epsilon_r). \tag{4}$$

The capacitance in Equation (3) can be calculated numerically, and Z_0 can then be obtained from Equation (4). The numerical results [15] for $T/W = 0.5$ can be approximated as follows:

$$\sqrt{\epsilon_r} Z_0 = 377 \times (H/W) \div [1 + 2.62(H/W)^{3/4}]. \tag{5}$$

The error is less than 1% when $H/W < 4.5$ [16]. The inverse of the right-hand side of Equation (5) contains the factor

$$f(W/H) = (W/H) + 2.62 \times (W/H)^{1/4}. \tag{6}$$

The first term represents the parallel-plate contribution, and the second term gives the approximate fringe-field contribution to the signal-line capacitance and impedance. Note that the fringe-field contribution becomes the dominant term when $H/W > 0.28$.

Because of yield and reliability considerations, the glass–epoxy dielectric cited above is formed using two or more laminated layers of epoxy-impregnated glass cloth, each 40 to 100 μm thick. Assuming that a 100-μm-wide signal line can be fabricated with acceptable yield, and the cloth has a thickness of 70 μm, the expected behavior of Z_0 as a function of the number of layers in the dielectric laminate is shown in **Table 1**. Note that the increase by a factor of 4 in laminate thickness would result in a 1.66× increase in Z_0. A 100-Ω signal-line impedance would require use of an eight-ply laminate, and would result in a relatively thick PCB. In addition, a thick laminate would require a large spacing between signal lines to contain the coupled noise (discussed later). The alternatives would be reduction of signal-line width, if possible, or use of a cloth having a lower dielectric constant.

To reduce Z_0 below 60 Ω, it would be necessary to reduce the thickness of the cloth or increase the signal-line width at the expense of wiring density.

Note that Equation (5) is useful only for $T/W = 0.5$. At other T/W values, use may be made of an approximate effective line width, viz.,

$$W(\text{effective}) = W \times (1 + T/W) \div 1.5. \tag{7}$$

For a typical PCB structure having $T/W = 0.3$ to 0.6, and $H/W = 0.5$ to 5, the error in computing Z_0 is found to be less than 3% when use is made of that expression for W(effective).*

It follows from Equation (5) that the ratio of the fractional variation of Z_0 to that of H/W is

* K. T. Ho, IBM Systems Technology Division, Endicott, New York, private communication.

$$(\delta Z_0/Z_0)/[\delta(H/W)/(H/W)]$$
$$= [1 + 0.655 \times (\mathrm{H/W})^{3/4}]$$
$$\div [1 + 2.62 \times (H/W)^{3/4}]. \quad (8)$$

Illustratively, we assume that the effective signal-line width, W(effective), has an 8% process variation, and the epoxy-impregnated glass cloth thickness has a 6% variation. The root-sum-square of the above two variations yields a 10% variation for H/W. If the design objective is $H/W = 4$, Z_0 should display a 3.4% variation. If it is $H/W = 1$, Z_0 should display a 4.6% variation. Of course, variability in ϵ_r will lead to additional variation in Z_0.

Microstrip and triplate structures

In some PCBs, signal lines are placed on the upper surface of the dielectric medium, as illustrated in **Figure 2**. For such a "microstrip" line [14] most of the associated electromagnetic wave is contained in the underlying dielectric medium. However, a significant fraction of the wave energy resides in the air dielectric. The combined traveling wave in the inhomogeneous medium is not a pure transverse electromagnetic (TEM) wave [5]. Use is made of a quasi-TEM wave approximation, and transmission-line treatment is applied as previously. Laboratory measurements indicate that the propagation time constant lies between that of the air and the underlying dielectric medium.

Since the permeability μ of the dielectric medium is equal to that of air, the value of L of the signal line in Figure 2 is identical to that of the signal line in Figure 1. The value of C can be obtained by solving the electrostatic field problem [15]. Numerical calculation results indicate that the fringe-field contribution can be closely approximated by $1.37 \times (W/H)^{1/6}$, viz.,

$$C = 4 \times \epsilon_0 \times [(W/H) + 1.37 \times (W/H)^{1/6}]. \quad (9)$$

This approximation contains an error of <1% if $0.1 < (W/H) < 10$. From Equations (6) and (9), we obtain an effective ϵ_r of

$$\epsilon_r(\mathrm{eff}) = 4 \times [(W/H) + 1.37 \times (W/H)^{1/6}]$$
$$\div [(W/H) + 2.62 \times (W/H)^{1/4}]. \quad (10)$$

Equation (6) contains an error of <1% of opposite polarity to that in Equation (9) when $0.1 < (W/H) < 4.5$, yielding a ±2% error in Equation (10). Typically, for $H/W = 0.5$ to 5, Equation (10) gives an ϵ_r(eff) of from 2.54 to 2.77.

Alternatively, the signal line may be sandwiched between two reference planes, forming a shielded stripline, as shown in **Figure 3** [5, 6, 14]. The latter is referred to here as a triplate structure to emphasize the presence of the second reference plane. Its presence increases C and reduces Z_0. The parallel-plate contribution in an expression which is the counterpart to Equation (6) increases by a factor of $1 + H_1/H_2$. Its magnitude is 1.5 if $H_2 = 2H_1$, and 2.0 if

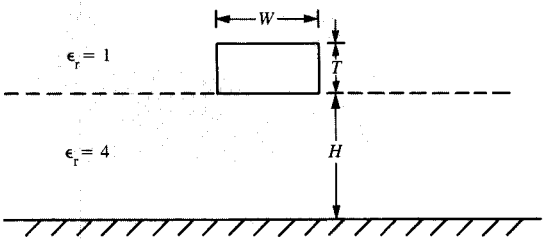


Figure 2

Cross section of a microstrip line.

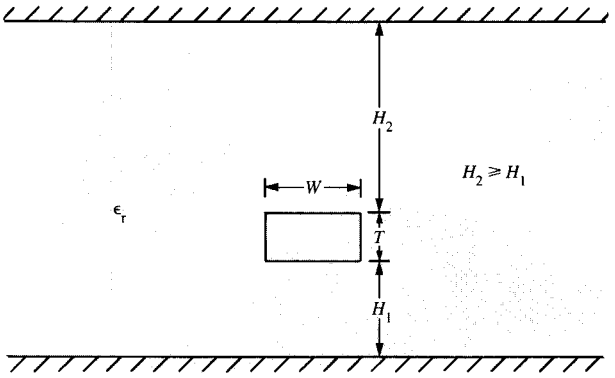


Figure 3

Cross section of a shielded stripline (triplate) structure.

$H_2 = H_1$. Numerical calculation indicates that the fringe-field contribution causes only a slight change if $H_2 = 2H_1$, and only a 7% increase if $H_2 = H_1$ [16]. Therefore, in the triplate structure, the fringe-field contribution becomes the dominant term when $H_1/W > 0.48$ and 0.64 for $H_2 = 2H_1$ and $H_2 = H_1$, respectively. For $T/W = 0.5$, the signal-line impedances can be approximated by the following formulas:

$$\sqrt{\epsilon_r} Z_0(H_2 = 2H_1) = 377 \times (H_1/W)$$
$$\div [1.5 + 2.62(H_1/W)^{3/4}], \quad (11)$$
$$\sqrt{\epsilon_r} Z_0(H_2 = H_1) = 377 \times (H_1/W)$$
$$\div [2 + 2.8(H_1/W)^{3/4}]. \quad (12)$$

At other T/W ratios, use may be made instead of W(effective). The error in Z_0 is typically found to be less than 3% if $T/W = 0.3$ to 0.6 and $H_1/W = 0.5$ to 5.* If $H_1/W = 0.5$, the presence of the second reference plane at $H_2 = 2H_1$ or H_1 causes a reduction in Z_0 of 16% or 30%, respectively. If $H_1/W = 3.0$, the reduction becomes 7% or 17%, respectively.

Effect of dc and skin-effect resistances

As semiconductor chip technology has advanced, the number of circuits per chip has increased considerably, resulting in a sizable increase in the required number of on-chip signal I/O leads and PCB signal lines [17]. To achieve this by increasing the number of PCB signal layers might require an increase in board thickness, leading to process challenges. In addition, the thickness might become incompatible with the PCB edge connectors which are used. Also, if use is made of plated through-holes, as, e.g., cited in [1], the associated increase which might be required in their length-to-diameter aspect ratio might cause difficulties in hole drilling and plating. Alternatively, signal-line widths and spacings might be reduced, resulting in other process-related challenges and an increase in signal-line resistance. Such an increase has different effects on the packaging of different logic circuit families [18].

Another consideration is that an increase in chip circuit density has reduced internal circuit delay time and off-chip driver-circuit rise times. This has resulted in a corresponding increase in PCB operating-frequency requirements, leading to the need to consider the skin effect [5, 13, 19–21].

The skin depth δ is given by

$$\delta = 1/\sqrt{\pi f \sigma \mu}, \tag{13}$$

where f is the frequency and σ is the conductivity. For copper, for which $1/\sigma = 0.0172\ \Omega\text{-}\mu\text{m}$, δ is calculated to be 2.09 μm at 1 GHz.

The current density decreases exponentially to about 5% of its surface value at three times the skin depth. If the signal-line thickness exceeds 6δ, the series resistance is roughly inversely proportional to the skin depth, i.e., linearly proportional to the square root of frequency.

If a signal line and its reference conductor have a circular cross section, the current density is highest at adjacent surfaces (proximity effect). As a result, the resistance can increase by 15.5% when the axial separation is four times the conductor radius [19].

For a signal line of rectangular cross section over a flat reference plane, the associated frequency-dependent resistance can be obtained from numerical calculation [21]. Lossy transmission-line simulation can then be used for more detailed calculations [22–24]. For a first-order approximation of the associated signal rise-time degradation, we calculate the skin-effect resistance per unit length, R_s, as follows:

$$R_s \approx 1/[\sigma \times (\text{perimeter}) \times (\text{skin depth})]$$
$$= (1/\sigma)\sqrt{\pi f \sigma \mu}/2(W + T). \tag{14}$$

Although the proximity effect has not been taken into account, nor has the resistance of the reference plane, this approximation is sufficient for establishing initial design guidelines.

If the dc resistance R_{dc} and the skin-effect resistance are taken into consideration, the transmission-line propagation constant can be approximated as [16]

$$\Gamma \approx s\tau + (R_{dc}/2Z_0) + \sqrt{s}(R_1/2Z_0\sqrt{\pi}), \tag{15}$$

where $\tau \equiv \sqrt{LC}$, $Z_0 \equiv \sqrt{L/C}$, and $R_1 \equiv R_s/\sqrt{f}$ (R_1 is independent of frequency).

The use of Equation (15) is limited to the frequency range for which

$$\omega L = \omega \tau Z_0 \gg \sqrt{2R_s}. \tag{16}$$

If $Z_0 = 80\ \Omega$ and $\epsilon_r = 4$, $\omega\tau Z_0 = 3350 \times (f/10^9)\ \Omega$/m. For a 100×50-μm copper wire, $R_{dc} = 3.45\ \Omega$/m, and $R_s \approx 27.5 \times (f/10^9)^{1/2}\ \Omega$/m. Equation (16) is generally satisfied at $f > 10$ MHz. If the width and thickness of the signal line are each reduced by a factor of 10, R_{dc} and R_s will increase by factors of 100 and 10, respectively; the equation can then generally be satisfied at above 1 GHz.

In order to illustrate the signal attenuation due to R_{dc} and the rise-time degradation due to R_s, we assume that (1) the voltage waveform at the input end of the transmission line (at $y = 0$) is a V_0-volt ramp, with a 0-to-100% rise time of T_r, and (2) the end of the transmission line (at $y = D$) is terminated by another identical transmission line of sufficient length to ensure that there is no signal reflection.

The voltage waveform at $y = D$ is [16]

$$V_D(t) = V_0\{\exp(-R_{dc}D/2Z_0)\} \times [u(t - \tau D)p(t - \tau D) - u(t - \tau D - T_r)p(t - \tau D - T_r)], \tag{17}$$

where

$$p(t) \equiv (t/T_r)[(1 + b^2/2t)\,\text{erfc}(b/2\sqrt{t}) - \{b/\sqrt{\pi t}\}\exp(-b^2/4t)] \tag{18}$$

and

$$b = R_1 D/2Z_0\sqrt{\pi}. \tag{19}$$

The exponential term in Equation (17) represents the signal magnitude attenuation due to R_{dc}, which may require an appropriate change in off-chip driver current. The additional delta-I noise associated with the resulting increase in line current is usually small compared to $V_0[1 - \exp(R_{dc}D/2Z_0)]$. This is illustrative of design trade-offs which must be taken into account in considering line-width reductions.

The term in the square brackets of Equation (17) represents the signal rise-time degradation due to R_s, which may be expressed as an additional delay (in ns) through use

of the parameter Φ defined as follows:

$$\Phi \equiv 2.5b = 0.705R_1 D/Z_0, \tag{20}$$

where $R_1 = R_s/\sqrt{f}$, with f expressed in GHz.

For a one-meter-long, 100 × 50-μm signal line in an 80-Ω impedance design, the substitution of Equation (14) into Equation (20) gives a value of $\Phi \approx 0.24$.

The square-bracket term of Equation (17), assuming that $T_r = 0.5$ ns, is plotted in **Figure 4** for various values of Φ, which is linearly proportional to the line length D. For a lossless transmission line and a voltage ramp of 0.5-ns rise time, the signal would cross the 80% threshold at $t - \tau D = 0.4$ ns. Because of the skin effect, this occurs at 0.61 ns for $\Phi = 0.5$, and at 8.17 ns for $\Phi = 2.5$. The additional delay would be reduced to 0.14 and 3.30 ns, respectively, if the receiver circuit threshold voltage were set at a 70% level. The results are shown in **Figure 5**. Note that both the abscissa, Φ^2/T_r, and the ordinate, $\delta(\text{delay})/T_r$, are normalized by the rise time T_r.

At the upper right, $\delta(\text{delay}) \approx 1.2\Phi^2$ for an 80% threshold level and $\approx 0.5\Phi^2$ for a 70% threshold level. It should be emphasized here that the signal attenuation due to dc resistance has been compensated by increasing the output current of the off-chip driver circuits.

In order to minimize the additional delay due to the skin-effect rise-time degradation, it is desirable to set a limit of $\Phi < 0.3$. This is equivalent to setting a maximum critical signal-line length of

$$D_{Cr} < 0.426 Z_0/R_1 . \tag{21}$$

For a copper conductor having $W = 100$ μm, $T = 50$ μm, it follows that $R_1 = 27.5\,\Omega\text{-ns}^{1/2}/\text{m}$. For a PCB design in which $Z_0 = 80$ Ω, Equation (21) indicates that $D_{Cr} < 1.24$ m. On the other hand, if the PCB were to be designed with $W = 25$ μm, $T = 12.5$ μm, it would follow that for a 50-Ω signal line, D_{Cr} would be <0.194 m.

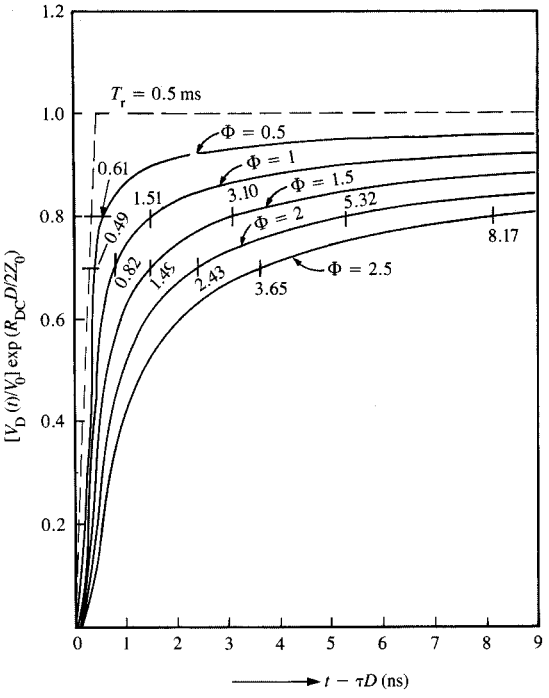


Figure 4

Signal rise-time degradation due to skin-effect loss.

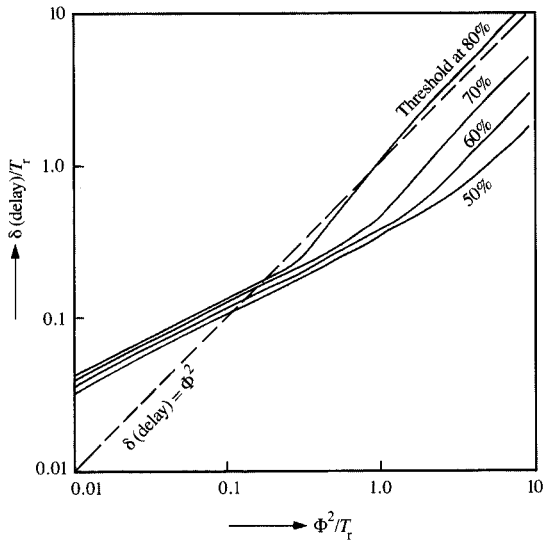


Figure 5

Additional delay due to rise-time degradation.

Matched-load impedances of parallel signal lines

Figure 6 shows a vertical cross section, in a homogeneous medium, of a triplate structure having three parallel signal lines sandwiched between two voltage-reference planes. It is assumed that the signal lines have the same width W and thickness T, and are located at the same height H_1 above the lower reference plane; and that $H_2 \geq H_1$. For a stripline structure, $H_2 = \infty$. The signal lines are assumed to be spaced at a distance of S from each other. In this section, we discuss an example for which $T = 0.5\,W$, $H_1 = 2.0\,W$, $H_2 = \infty$, and $S = 1.0\,W$ and $4.0\,W$, and we compare resulting electrical parameters with the extreme case of infinite line separation, $S = \infty$.

Numerical calculation results for the elements in the associated 3 × 3 capacitance and inductance matrices [15]

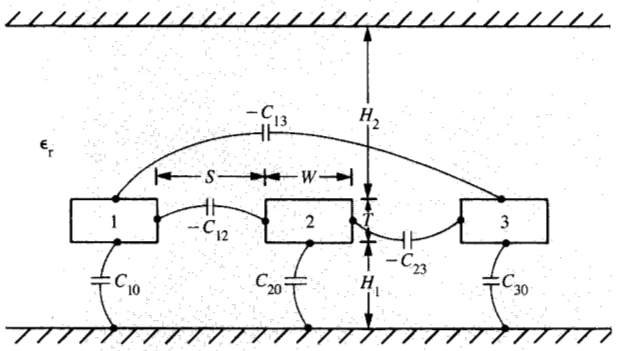


Figure 6

Vertical cross section of three parallel signal lines in a homogeneous medium.

Table 2 Electrical parameters for triple-line example in a homogeneous medium for which $\epsilon_r = 1.0$.

Parameter \ Spacing	$S = \infty$	$S = 4W_0$	$S = W_0$
C_{11} (pF/m)	23.82	24.28	29.34
$-C_{12}$ (pF/m)	0	3.00	11.40
$-C_{13}$ (pF/m)	0	0.57	1.35
C_{22} (pF/m)	23.82	24.67	34.27
C_{2F} (pF/m)	23.82	23.91	24.98
L_{11} (nH/m)	466.14	465.34	453.25
L_{12} (nH/m)	0	58.88	181.19
L_{13} (nH/m)	0	18.26	91.20
L_{22} (nH/m)	466.14	464.71	444.84
Z_{02F} (Ω)	139.90	139.41	133.45
$\sqrt{L_{11}/C_{11}}$ (Ω)	139.90	138.44	124.28
Z_{01} (Ω)	139.90	138.40	123.00
$\sqrt{L_{22}/C_{22}}$ (Ω)	139.90	137.25	113.93
Z_{02} (Ω)	139.90	137.20	112.80
b_{21}	0	0.0623	0.190
b_{21} (approx.)	0	0.0621	0.183
b_{31}	0	0.0157	0.0622
b_{31} (approx.)	0	0.0157	0.0618
b_{12}	0	0.0626	0.207
b_{12} (approx.)	0	0.0626	0.199

Notes: 1. $C_{21} = C_{23} = C_{32} = C_{12}$.
2. $L_{21} = L_{23} = L_{32} = L_{12}$.
3. $C_{33} = C_{11}$.
4. $L_{33} = L_{11}$.
5. $Z_{03} = Z_{01}$.
6. $Z_{02F} = \sqrt{L_{22}/C_{2F}}$.

which must be considered are shown in **Table 2**. It follows from stored energy considerations [25] that the matrices are positive-definite symmetrical matrices, and the off-diagonal elements of the capacitance matrix are all negative. In calculating the inductance [15], it is assumed that all of the current flux is confined to the conductor surface; i.e., the internal inductance is not included. When the adjacent signal lines are brought into closer proximity, the surface current density redistributes itself to reach its minimum-energy state, reducing the self-inductance slightly.

The term C_{22} is the sum of C_{20}, $-C_{12}$, and $-C_{23}$, and represents the capacitance between line 2 and a combined voltage reference formed from line 1, line 3, and the original reference plane. It increases drastically as the spacing between adjacent lines is decreased from ∞ to W.

If lines 1 and 3 are left floating, the capacitance between line 2 and the reference plane becomes the parallel combination of three branches: (1) C_{20}, (2) series capacitance of C_{10} and $-C_{12}$, and (3) series capacitance of C_{30} and $-C_{23}$. The result is defined as C_{2F}, and is included in Table 2. The capacitance C_{2F} can be regarded as the capacitance between line 2 and the reference plane if lines 1 and 3 are replaced by a dielectric material having an infinite dielectric constant. Since the high-dielectric regions would only occupy relatively small areas, the increase in C_{2F} would be very small compared to the increase in C_{22}. The self-inductance L_{22} is calculated with the adjacent lines floating, as is C_{2F}. Hence, it follows that $Z_{02F} \equiv \sqrt{L_{22}/C_{2F}}$ is the open-circuited impedance of the center signal line. The calculated results are shown in Table 2. Note that the open-circuited impedance is only slightly less than that of a single isolated line. In practice, the near end of the two adjacent lines would not be floating, but would most likely be connected to other signal-line sections before being terminated at driver or receiver circuits.

For lossless coupled transmission lines, the characteristic impedance can be represented as the $n \times n$ matrix [24, 26]

$$Z_0 = Y_0^{-1} = (LC)^{-1/2}L = (LC)^{1/2}C^{-1}, \tag{22}$$

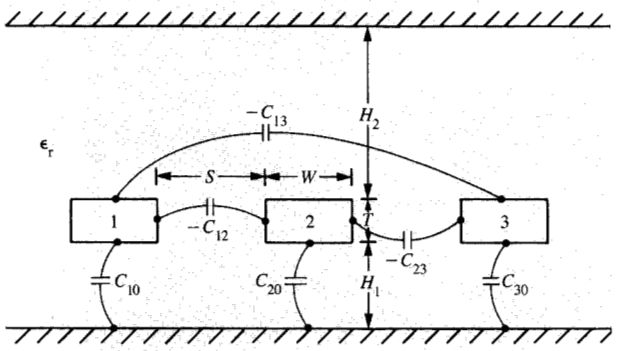
where $(LC)^{1/2} = P\tau P^{-1}$, P is the $n \times n$ eigenvector matrix of the LC product, and τ is the positive square root of the corresponding eigenvalues.

For the example shown in Table 2, the three eigenvalues are identical because of the assumed presence of a homogeneous medium. The characteristic impedance and admittance matrices become

$$Z_0 = (1/\tau)L = \tau C^{-1}, \tag{23}$$

$$Y_0 = Z_0^{-1} = \tau L^{-1} = (1/\tau)C. \tag{24}$$

Note that Z_0 is the open-circuited input impedance matrix of a three-port network, which represents an infinitely long section of three coupled transmission lines. Y_0 is the short-circuited input admittance matrix of such a three-port network.



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Z_{01} (Ω)	139.90	138.40	123.00
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4. $L_{33} = L_{11}$.
5. $Z_{03} = Z_{01}$.
6. $Z_{02F} = \sqrt{L_{22}/C_{2F}}$.

which must be considered are shown in **Table 2**. It follows from stored energy considerations [25] that the matrices are positive-definite symmetrical matrices, and the off-diagonal elements of the capacitance matrix are all negative. In calculating the inductance [15], it is assumed that all of the current flux is confined to the conductor surface; i.e., the internal inductance is not included. When the adjacent signal lines are brought into closer proximity, the surface current density redistributes itself to reach its minimum-energy state, reducing the self-inductance slightly.

The term C_{22} is the sum of C_{20}, $-C_{12}$, and $-C_{23}$, and represents the capacitance between line 2 and a combined voltage reference formed from line 1, line 3, and the original reference plane. It increases drastically as the spacing between adjacent lines is decreased from ∞ to W.

If lines 1 and 3 are left floating, the capacitance between line 2 and the reference plane becomes the parallel combination of three branches: (1) C_{20}, (2) series capacitance of C_{10} and $-C_{12}$, and (3) series capacitance of C_{30} and $-C_{23}$. The result is defined as C_{2F}, and is included in Table 2. The capacitance C_{2F} can be regarded as the capacitance between line 2 and the reference plane if lines 1 and 3 are replaced by a dielectric material having an infinite dielectric constant. Since the high-dielectric regions would only occupy relatively small areas, the increase in C_{2F} would be very small compared to the increase in C_{22}. The self-inductance L_{22} is calculated with the adjacent lines floating, as is C_{2F}. Hence, it follows that $Z_{02F} \equiv \sqrt{L_{22}/C_{2F}}$ is the open-circuited impedance of the center signal line. The calculated results are shown in Table 2. Note that the open-circuited impedance is only slightly less than that of a single isolated line. In practice, the near end of the two adjacent lines would not be floating, but would most likely be connected to other signal-line sections before being terminated at driver or receiver circuits.

For lossless coupled transmission lines, the characteristic impedance can be represented as the $n \times n$ matrix [24, 26]

$$Z_0 = Y_0^{-1} = (LC)^{-1/2}L = (LC)^{1/2}C^{-1}, \tag{22}$$

where $(LC)^{1/2} = P\tau P^{-1}$, P is the $n \times n$ eigenvector matrix of the LC product, and τ is the positive square root of the corresponding eigenvalues.

For the example shown in Table 2, the three eigenvalues are identical because of the assumed presence of a homogeneous medium. The characteristic impedance and admittance matrices become

$$Z_0 = (1/\tau)L = \tau C^{-1}, \tag{23}$$

$$Y_0 = Z_0^{-1} = \tau L^{-1} = (1/\tau)C. \tag{24}$$

Note that Z_0 is the open-circuited input impedance matrix of a three-port network, which represents an infinitely long section of three coupled transmission lines. Y_0 is the short-circuited input admittance matrix of such a three-port network.

To obtain the matched-load impedance of the three lines, we might consider measuring the input impedance of one line, using, for example, a time-domain reflectometer, terminating this line in its measured input impedance, proceeding to do the same for each remaining line, and then iteratively repeating the entire procedure until it converges. The set of impedances thus obtained, $\{Z_{01}, Z_{02}, Z_{03}\}$, is defined as the matched-load impedance. The results of such an iterative simulation are shown in Table 2. The difference between Z_{02} and $\sqrt{L_{22}/C_{2F}}$ is small for $S = 4W$, but becomes unacceptably large for $S = W$. On the other hand, $\sqrt{L_{11}/C_{11}}$ and $\sqrt{L_{22}/C_{22}}$ can be used as first-order approximations for Z_{01} and Z_{02}, respectively.

The ratio of the open-circuited impedance for line 2, $\sqrt{L_{22}/C_{2F}}$, and the first-order approximation for its matched-load impedance, $\sqrt{L_{22}/C_{22}}$, is $\sqrt{C_{22}/C_{2F}}$. One can easily measure the two capacitances, C_{22} and C_{2F}, and obtain an assessment of the difference between the open-circuited and matched-load impedances. A significant difference indicates an impedance mismatch at the boundary of the sparsely and closely placed wiring regions.

Cross talk among adjacent parallel signal lines

Three long parallel signal lines over a voltage reference plane are shown in **Figure 7**. Line 1 is assumed to be connected to an active signal source, and the near ends of lines 2 and 3 are assumed to be terminated by their corresponding matched-load impedances. Because of their assumed long length, the terminations at their far ends are irrelevant. These lines can be treated as a three-port resistor network. At their input ends, lines 2 and 3 will display finite voltages, designated as cross talk, or coupled noises, due to the presence of the signal on line 1. The ratios of the coupled noises on lines 2 and 3 to the active signal voltage on line 1 are defined as the backward (i.e., backward to the near end) -coupling coefficients b_{21} and b_{31}. (The voltages on lines 2 and 3 are then $b_{21}V_{01}$ and $b_{31}V_{01}$, respectively, when the voltage on line 1 is V_{01}.)

If we assume that line 1 has a source impedance equal to its matched-load impedance Z_{01}, and a Thevenin's equivalent source voltage of $2V_{01}$, the voltage on its input end should be V_{01}. Similarly, if line 3 is the only active line with a Thevenin's equivalent voltage of $2V_{03}$ and a source impedance of Z_{03}, the voltages on the input ends of lines 1, 2, and 3 should be $b_{13}V_{03}$, $b_{23}V_{03}$, and V_{03}, respectively. From linear superposition, if lines 1 and 3 are active with Thevenin's equivalent source voltages $2V_{01} = 2V_{03} = 2V_0$, the voltages on the input ends of lines 1, 2, and 3 should be $(1 + b_{13})V_0$, $(b_{21} + b_{23})V_0$, and $(1 + b_{31})V_0$, respectively. If lines 1 and 3 are assumed to be active, the voltage on line 1 will not be equal to V_0. The backward-coupling coefficients obtained from simulations are included in Table 2.

When all signal lines are terminated by their corresponding matched-load impedances, the backward-coupled noise appears as near-end cross talk; it has the following closed-form approximation [9]:

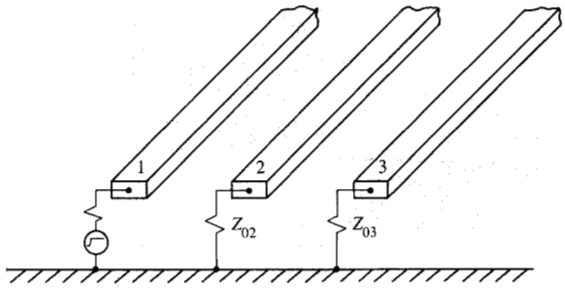

Figure 7

Near-end termination of three long parallel signal lines.

$$V_{21}(\text{near end}) \approx b_{21}[V_0(t) - V_0(t - 2\tau D)], \tag{25}$$

$$b_{21}(\text{approx.}) = 0.25(-C_{21}/C_{22} + L_{21}/L_{11}), \tag{26}$$

where $V_0(t)$ is the voltage on the input end of line 1; the product τD is the delay time across the coupled-line section of length D. The second term on the right-hand side of Equation (26) is the inductive coupling coefficient; it is independent of the relative dielectric constant. The first term on the right-hand side of Equation (26) is the capacitive coupling coefficient; it is independent of the relative dielectric constant only in a homogeneous medium. Both terms are functions of geometrical parameters. The results of these calculations are also included in Table 2. The approximation contains an error of <4% even when the coupling coefficient exceeds 0.2. Equation (25) indicates that if the 0-to-100% rise time T_r of $V_0(t)$ is shorter than twice the delay time across the length of the coupled-line section, i.e., $2\tau D$, the noise reaches its maximum magnitude, designated as the saturated backward-coupled noise, and has a pulse width of $2\tau D$. On the other hand, if the length of the parallel section is shorter, so that $2\tau D < T_r$, the magnitude of the coupled noise should be less and should have a pulse width of T_r. Therefore, we should be able to reduce the magnitude of the coupled noise by reducing the length of the parallel sections. This is usually accomplished by establishing a design guideline and using a computer-aided design system to ensure that it is strictly adhered to.

If the spacing between adjacent lines decreases, $-C_{12}$ increases more rapidly than C_{22}, yielding an increase in coupled noise and a decrease in matched-load impedances, as illustrated in Table 2.

Although in a homogeneous medium the backward-coupling coefficient b_{21} is independent of ϵ_r, it is sensitive to

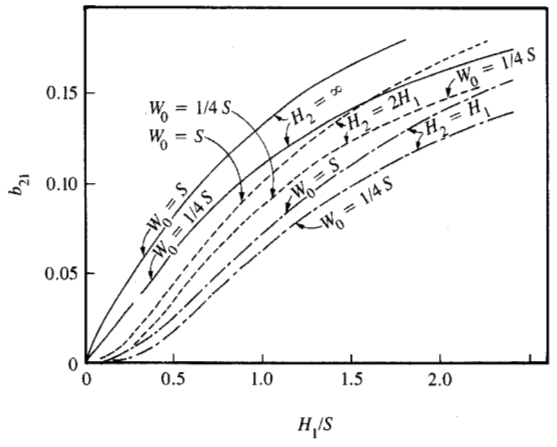

Figure 8

Backward coupling to the central signal line in a homogeneous medium if only one adjacent line is active.

Table 3 Wiring density comparisons for a 60-Ω design, assuming the presence of a homogeneous medium, and that $b_{21} \leq 0.1$.

ϵ_r	*Parameters*	$H_2 = \infty$	$H_2 = 2H_1$	$H_2 = H_1$
2.5	H_1/W_0	0.82	1.04	1.39
	H_1/S	0.68	0.99	1.34
	$\frac{S}{W_0} = \frac{H_1/W_0}{H_1/S}$	1.21	1.05	1.04
	$S + W_0$	$2.21W_0$	$2.05W_0$	$2.04W_0$
4.0	H_1/W_0	1.37	1.72	2.24
	H_1/S	0.74	1.03	1.37
	$\frac{S}{W_0} = \frac{H_1/W_0}{H_1/S}$	1.85	1.67	1.64
	$S + W_0$	$2.85W_0$	$2.67W_0$	$2.64W_0$

geometrical parameters. We assume a signal-line thickness T of half of the minimum manufacturable line width W_0. Through numerical calculations, we show that the relevant geometrical parameters in Figure 6 have the following order of importance: (1) H_1/S, (2) H_2/H_1, and (3) W_0/S. Note that we have used the line-to-line spacing S as a normalization parameter.

Furthermore, we assume that the three signal lines in Figure 6 have an edge-to-edge spacing $S = W_0$ to $4W_0$. The 3 by 3 capacitance and inductance matrices are then calculated [15], and the matched-load impedances $\{Z_{01}, Z_{02}, Z_{03}\}$, as defined before, are simulated, as are the backward-coupling coefficients b_{21}, b_{31}, and b_{12}.

The two solid curves in **Figure 8** show the backward-coupling coefficient b_{21} versus the H_1/S ratio, with $W_0/S = 1.0$ and 0.25 as parameter for the stripline structure. Note that when W_0/S is kept at 1.0, and H_1 is reduced by a factor of four so that H_1/S is reduced from 1.6 to 0.4, b_{21} is reduced from 0.171 to 0.070. On the other hand, when both S and H_1 are increased by a factor of four, so that H_1/S = constant and W_0/S is reduced by a factor of four from 1.0 to 0.25, b_{21} is reduced from 0.171 to 0.146. The reduction is about 0.02–0.03 throughout the range of H_1/S in practical applications. When a second reference plane is introduced to form the triplate structure, similar numerical calculations are carried out for $H_2/H_1 = 2.0$ and 1.0, and shown in Figure 8. A few observations are summarized as follows:

1. b_{21} is heavily influenced by the H_1/S ratio, but is weakly dependent on the W_0/S ratio.
2. The introduction of the second reference plane to form the triplate structure reduces the coupling coefficient from that of the stripline structure by about 0.025–0.035 if $H_2 = 2H_1$, and by 0.04–0.06 if $H_2 = H_1$.
3. We may use linear interpolation with reasonable accuracy for W_0/S between 0.25 and 1.0, and for values of H_1/H_2 which lie between 0.0 and 1.0. Note that $H_1/H_2 = 0$ for the stripline structure.

Typically, the total saturated coupled noise should not exceed 200 mV per volt of active signal swing. If a signal line has two parallel adajcent active lines, the total coupled noise will double. Therefore, it is important that $b_{21} < 0.1$. From Figure 8, we find that when $S = W_0$, the acceptable design is $H_1 < 0.65S$, $0.98S$, or $1.33S$ for $H_2 = \infty$, $2H_1$, or H_1, respectively. From Equations (5), (11), and (12), we find that the corresponding single signal-line impedances are $Z_0 = 42$, 46, and 46.5 Ω if $\epsilon_r = 4$, and 53, 58, and 59 Ω if $\epsilon_r = 2.5$.

Let us compare the wiring density of the stripline and triplate structures for a 60-Ω design with a restriction on coupled noise equivalent to $b_{21} \leq 0.1$. The results are shown in **Table 3** for $\epsilon_r = 2.5$ and 4.0. Note that, with $\epsilon_r = 4$, the acceptable center-to-center pitch between adjacent signal lines is reduced from $2.85W_0$ to $2.67W_0$ when a second reference plane is introduced to convert a stripline into a triplate structure with $H_2 = 2H_1$. On the other hand, the reduction of ϵ_r from 4.0 to 2.5 for the stripline structure will reduce the pitch from $2.85W_0$ to $2.21W_0$. In other words, under the same signal-line impedance and coupled-noise restriction, the low-dielectric medium displays wiring-density advantages. On the other hand, the introduction of a second reference plane to form the triplate structures offers only minor density advantages. When there are two signal layers sandwiched between the reference planes, other design considerations become important.

Effect of line spacing on matched-load impedances

The presence of adjacent signal lines causes signal cross talk, and always reduces their matched-load impedance. **Figure 9** shows the percentage reduction of the matched-load impedance Z_{02} of the central one of three parallel signal lines. The ordinate is defined as

$$\delta Z_{02}\ (\%) \equiv 100\% \times (Z_{02} - Z_0) \div Z_0\,, \qquad (27)$$

where Z_0 is the characteristic impedance of a single signal line having given W, T, H_1, and H_2 values.

To compensate for the reduction in impedance, H_1 can be increased so that Z_0 lies halfway between its value for an isolated line and Z_{02}. The line spacing may need to be increased to contain the coupled noise. The change in Z_{02} is strongly influenced by H_1/S, and mildly influenced by W_0/S and the introduction of a second voltage-reference plane. In Figure 9, linear interpolation may be used with reasonable accuracy for values of W_0/S between 0.25 and 1.0 and values of H_1/H_2 between 0 and 1.0.

In the previous section, we pointed out that for $W_0 = S$ the backward-coupling coefficient b_{21} is less than 0.1 when $H_1 < 0.65S$, $0.98S$, and $1.33S$ for $H_2 = \infty$, $2H_1$, and H_1, respectively. From Figure 9 we find that the corresponding reduction in matched-load impedance is 7.5%, 7.2%, and 7.1%, respectively. Thus, when a pulse traveling on a signal line in the absence of neighboring lines on both sides arrives at the point where both neighboring lines are present, it experiences an impedance discontinuity, which causes a 3.7–3.9% reduction of the active voltage on the central signal line. The output current of the off-chip driver circuit may need to be increased by about 3.8% to achieve the required voltage swing.

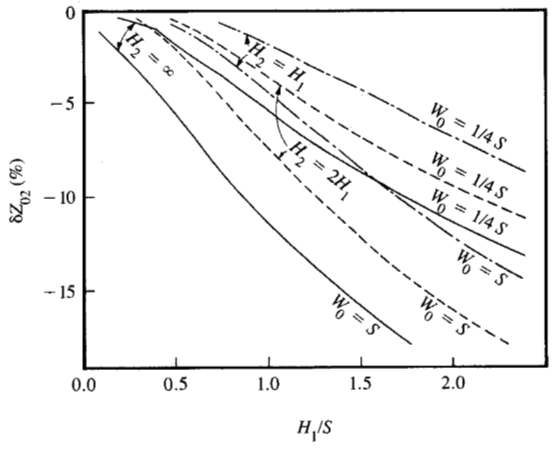

Figure 9

Percentage reduction of matched-load impedance of central signal line, in a homogeneous medium.

Effects of orthogonal lines on impedance and coupled noise

We assume that the signal lines of interest run in the y-direction. With the introduction of x-direction signal lines of the corresponding plane pair, the environment for energy propagation along the y-direction signal lines is changed, as summarized in the following:

- The vertical cross section of the PCB normal to the y-direction is a function of y; i.e., the y-direction transmission line is not uniform along the propagation direction. If the spacing between the x-direction lines on the adjacent signal layer is much less than a quarter wavelength (e.g., 1/20 of the wavelength), we may assume an average effect on the y-direction signal-line characteristics. For $\epsilon_r = 4$, a 1.0-mm center-to-center pitch between adjacent x-direction signal lines should not reach 1/20 of one wavelength until 7.5 GHz. Therefore, in the low-GHz range, we may continue using the uniform transmission-line treatment.
- The dielectric medium becomes inhomogeneous. The x-direction signal lines act as a dielectric medium with infinite relative dielectric constant [9]. This causes an increase in the signal propagation time. The impact is greater on the common-mode (or sum-mode) signal, and less on the difference-mode signal. This can be visualized, since energy of the difference-mode propagation is concentrated in the region between the y-direction parallel signal lines [5], where the influence of the medium with infinite relative dielectric constant is minimal.

Alternatively, the presence of the orthogonal lines can be regarded as follows:

- The alternating current along a y-direction signal line will induce eddy current along the circumference of the cross section of the x-direction signal lines on the adjacent layer. These eddy-current loops on the yz-plane will reduce the self and mutual inductances among the y-direction signal lines. Since the cross-sectional area of these x-direction signal lines occupies only a small percentage of the total space surrounding the signal lines, the reduction in the inductances is usually negligible, as has been demonstrated by numerical calculation and measurement [27–28].
- For capacitance calculation, the orthogonal lines are treated as part of the voltage reference. Numerical computation and hardware measurements indicate that there are significant increases in the self-capacitance, i.e., the main diagonal elements in the capacitance matrix, and moderate decreases in the mutual capacitances [28–30].

Considered qualitatively, because there is a significant increase in self-capacitance but a negligible reduction in inductance, the signal-line impedance, Equation (2), will decrease, and the signal propagation time, Equation (1), will increase, both at half the rate of that of the self-capacitance [28]. Because the backward-coupling coefficient is the sum of the capacitive and inductive coupling, as indicated in Equation (26), the inductive-coupling component is negligibly changed. But the combination of moderate reduction in the mutual capacitance and significant increase in the self-capacitance reduces the capacitive coupling, and thus also the backward-coupling coefficient.

The increase in propagation time of the common-mode signal is greater than that of the difference-mode signal; hence the difference-mode signal arrives at the receiving end first, so that the quiet line on the receiving end will experience an out-of-phase coupled noise [9]. The total forward-coupling energy is proportional to the propagation time difference between these two modes of propagation [23, 24]. Hence, the stronger the orthogonal-line effect, the worse the forward-coupled noise.

In the triplate structure, where the signal-plane pair is sandwiched between two voltage-reference planes, the orthogonal lines disturb the electromagnetic field in the region midway to the more distant voltage plane. This adds a small perturbation term to the W/H_2 parallel-plate contribution. The orthogonal-line effect is usually small.

The stripline structure contains only one voltage-reference plane. The signal lines closer to the voltage plane experience only a small effect due to the orthgonal lines, which are further away from the voltage plane. However, if the signal lines of interest are on the layer which is further away from the reference plane, a significant portion of their field to the reference plane is disturbed. Thus, it follows that

- Use of a wider line width may be needed to compensate for the larger value of H_1 to obtain the same impedance as that on the signal layer closer to the reference plane. Hence, the line-to-line spacing may need to be increased in proportion to the increase in H_1 to limit the coupled noise, thus reducing the wiring density on the outer signal layer.
- The signal lines on the outer signal layer, however, will experience a large impedance discontinuity at the boundary between sparsely and closely placed signal-line regions of the inner signal layer.
- For microstrip lines, the difference mode on the outer lines contains some electromagnetic energy in the air dielectric medium, yielding a greater difference in propagation delay between the common and difference modes, which further increases the forward-coupled noise.

Concluding remarks

The key aspects of PCB signal-line design for computer applications have been examined. The characteristic impedance of a single signal line in a stripline or triplate structure in a homogeneous medium has been treated by using imaginary parallel-plate and fringe-field contributions. The presence of signals in adjacent parallel lines can induce cross talk in a given line and reduce its matched-load impedance. The skin effect can degrade signal rise times and introduce delay which is proportional to the square of line length. Because of inadequate treatment in the literature, emphasis has been placed on examining the effects of matched-load impedance, the presence of orthogonal lines, and skin-effect-induced delay.

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